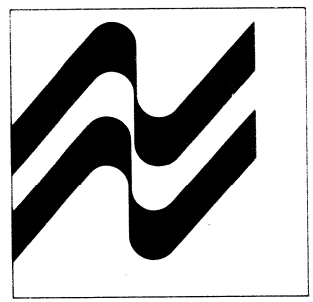
DATA CONVERSION/ ACQUISITION

DATABOOK

NATIONAL SEMICONDUCTOR



DATA CONVERSION/ ACQUISITION

DATABOOK

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Introduction

National Semiconductor brings to the marketplace a unique combination of qualifications to supply the components required by data acquisition and conversion—technologies include BI-FET™, linear bipolar, CMOS, thin film, laser trimming, I^2L, hybrid, and other state-of-the-art processes combined with high volume production capability.

The products in this databook include devices in the direct analog signal path before (and after) the digital processor.

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Section 1

Selection Guides

1

Section Contents

Analog Switches/Multiplexers Selection Guide

R_{ON} (Ω)	V_A/I (V)	Part Number	Logic Input	V_S (V) Typ	t_{ON}/t_{OFF} Typ
QUAD SPST					
200	± 10	LF11201	TTL	± 15	90/500 ns
200	± 10	LF11202	TTL	± 15	90/500 ns
200	± 10	LF11331	TTL	± 15	90/500 ns
200	± 10	LF11332	TTL	± 15	90/500 ns
200	± 10	LF11333	TTL	± 15	90/500 ns
250	± 10	LF13201	TTL	± 15	90/500 ns
250	± 10	LF13202	TTL	± 15	90/500 ns
250	± 10	LF13331	TTL	± 15	90/500 ns
250	± 10	LF13332	TTL	± 15	90/500 ns
250	± 10	LF13333	TTL	± 15	90/500 ns
280	± 7.5	CD4066	CMOS	± 7.5	50/50 ns
850	± 7.5	CD4016	CMOS	± 7.5	20/20 ns
TRIPLE SPDT					
280	± 7.5	CD4053	CMOS	± 7.5	150/150 ns
4-CHANNEL DIFFERENTIAL					
280	± 7.5	CD4052	CMOS	± 7.5	150/150 ns
350	12, −15	LF11509	TTL	± 15	1/0.2 μs
270	± 7.5	CD4529B	CMOS	_ 7.5	50/50 ns
8-CHANNEL					
250-400	± 5	AM3705	TTL	− 15, 5	300/600 ns
350	12, −15	LF11508	TTL	± 15	1/0.2 μs
270	± 7.5	CD4529B	CMOS	± 7.5	50/50 ns
280	± 7.5	CD4501	CMOS	± 7.5	150/150 ns

Notes:

R_{ON} max @ $T_A = 25°C$

V_A/I = maximum voltage or current to be safely switched

A/D Converter/DVM Selection Guide

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time (Typ)	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range (Note 1) M	I	C	Package	Comments
A/D CONVERTER											
ADC0800	8	±2 LSB	35 μs	10V	TTL, TRI-STATE®	+5, −12	•		•	18-Pin DIP	
ADC0801	8	±1/4 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP	Differential Input
ADC0802	8	±1/2 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP	Differential Input
ADC0803	8	±1/2 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP	Differential Input
ADC0804	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP	Differential Input
ADC0808	8	±1/2 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	28-Pin DIP	Includes 8-Channel MUX
ADC0809	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5		•	•	28-Pin DIP	Includes 8-Channel MUX
ADC0816	8	±1/2 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	40-Pin DIP	Includes 16-Channel MUX
ADC0817	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5		•	•	40-Pin DIP	Includes 16-Channel MUX
ADB1200 LF13300	12	±1/2 LSB	Q6 ms	±11V	TTL, TRI-STATE	+5, −15 ±15			•	28-Pin DIP 18-Pin DIP	Dual Slope
ADC1210	12	±1/2 LSB	26 μs	10.2V	CMOS	+5 to ±15	•	•		24-Pin DIP	
ADC1211	12 (10)	±1 LSB	30 μs	10.2V	CMOS	+5 to ±15	•	•		24-Pin DIP	
ADC3511	3 1/2-Digit	0.05%	200 ms	2V	TTL, TRI-STATE	+5			•	24-Pin DIP	Integrating μP Compatible
ADC3711	3 3/4-Digit	0.05%	400 ms	2V	TTL, TRI-STATE	+5			•	24-Pin DIP	Integrating μP Compatible
LM131	V-F	0.01%	N/A	V_{CC}-2V	N/A	+5 to +40	•	•	•	8-Pin DIP or TO-99 Can	Voltage-to-Frequency Converter 100 kHz Max
DIGITAL VOLTMETER											
ADD3501	3 1/2-Digit	0.05%	200 ms	V_{CC}-2V	7-Segment LED Drive	+5			•	28-Pin DIP	3 1/2-Digit LED DVM
ADD3701	3 3/4-Digit	0.05%	400 ms	V_{CC}-2V	7-Segment LED Drive	+5			•	28-Pin DIP	3 3/4-Digit LED DVM

Note 1: Temperature ranges are: "M" is −55°C to +125°C ambient; "I" is −40°C to +85°C or −25°C to +85°C; "C" is 0°C to 70°C.

D/A Converter Selection Guide

Part No.	Resolution (Bits)	Linearity @25°C (Max)	Internal Reference	Output Op Amp	Settling Time (+1/2 LSB)	Supplies (V)	Temperature Range (Note 1) M	I	C	Package	Comments
DAC0800	8	0.19			135 ns	±5 to ±15	•		•	16-Pin DIP	High Speed Multiplying
DAC0801	8	0.39			150 ns	±5 to ±15	•		•	16-Pin DIP	High Speed Multiplying
DAC0802	8	0.1			135 ns	±5 to ±15	•		•	16-Pin DIP	High Speed Multiplying
DAC0806	8	0.78			150 ns typ	±5 to ±15			•	16-Pin DIP	Multiplying
DAC0807	8	0.39			150 ns typ	±5 to ±15			•	16-Pin DIP	Multiplying
DAC0808	8	0.19			150 ns typ	±5 to ±15	•		•	16-Pin DIP	Multiplying
DAC0830	8	0.05			1μs typ	5 to 15	•	•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC0831	8	0.10			1μs typ	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC0832	8	0.20			1μs typ	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1000	10	0.05			500 ns typ	5 to 15	•	•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1001	10	0.1			500 ns typ	5 to 15		•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1002	10	0.2			500 ns typ	5 to 15		•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1006	10	0.05			500 ns typ	5 to 15	•	•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1007	10	0.1			500 ns typ	5 to 15		•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1008	10	0.2			500 ns typ	5 to 15		•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1020	10	0.05			500 ns typ	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1021	10	0.1			500 ns typ	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1022	10	0.2			500 ns typ	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1200	12	0.012	•	•	1.5-2.5 μs	±15, 5	•	•		24-Pin DIP	Current or Voltage Mode
DAC1201	12	0.049	•	•	1.5-2.5 μs	±15, 5	•	•		24-Pin DIP	Current or Voltage Mode
DAC1208	12	0.012			1 μs typ	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1209	12	0.024			1 μs typ	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying

Note 1: Ambient temperature range for "M" is −55°C to +125°C, "I" is −25°C to +85°C or −40°C to +85°C, "C" is 0°C to +70°C.

D/A Converter Selection Guide

Part No.	Resolution (Bits)	Linearity @25°C (Max)	Internal Reference	Output Op Amp	Settling Time (± 1/2 LSB)	Supplies (V)	Temperature Range (Note 1) M	I	C	Package	Comments
DAC1210	12	0.05			1 μs typ	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1218	12	0.012			1 μs typ	5 to 15		•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1219	12	0.024			1 μs typ	5 to 15			•	18-Pin DIP	4-Quadrant Multiplying
DAC1220	12	0.05			500 ns typ	5 to 15	•	•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1221	12	0.1			500 ns typ	5 to 15	•	•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1222	12	0.2			500 ns typ	5 to 15	•	•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1230	12	0.012			1μs typ	5 to 15	•	•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1231	12	0.024			1μs typ	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1232	12	0.05			1μs typ	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
*DAC1264	12	0.006	•		400 ns	± 15	•		•	24-Pin DIP	Hi-Speed
*DAC1265	12	0.012	•		400 ns	± 15	•		•	24-Pin DIP	Hi-Speed
DAC1280	12	0.024	•	•	300 ns/2.5 μs	± 15, 5	•		•	24-Pin DIP	Current or Voltage Mode
DAC1285	12	0.012	•	•	300 ns/2.5 μs	± 15, 5	•		•	24-Pin DIP	Current or Voltage Mode

Sample and Hold Selection Guide

	LF198	LF398	LH0023	LH0023C	LH0043	LH0043C	LH0053	LH0053C
Accuracy (% Max) Gain/Offset Error	0.02	0.02	0.01	0.02	0.1	0.3	0.2	0.3
Offset Voltage (mV Max)	5	10	20	20	40	40	10	15
Droop Rate (mV/sec, 25°C)								
C_S = 1000 pF	30	30	100	100	10	10	30	30
C_S = 10000 pF	3	3	10	10	1	1	3	3
Acquisition Time (μs, 25°C)								
C_S = 1000 pF	4	4	10	10	10	10	4	4
C_S = 10000 pF	20	20	50	50	50	50		
Aperture Time (ns, 25°C)	25	25	150	150	20	20	25	25
Temperature Range (°C)	−55 to +125	0 to +70	−55 to +125	−25 to +85	−55 to +125	−25 to +85	−55 to +125	+25 to +85
Comment	General Purpose	General Purpose	Low Drift	Low Drift	Medium Speed	Medium Speed	High Speed	High Speed

Note 1: Ambient temperature range for "M" is −55°C to +125°C, "I" is −25°C to +85°C or −40°C to +85°C, "C" is 0°C to +70°C.

* To be announced

Data Conversion/Acquisition Circuits Cross Reference Guide

National Part Number	Function	National Direct Replacement	National Functional Replacement
ANALOG DEVICES			
AD537JD	V/F Converter		LM331H, N
AD537KD			LM331AH, N
AD537SD			LM131AH
AD559KD	8-Bit D/A Converter	DAC0808LCJ	
AD559SD		DAC0808LD	
AD561JD	10-Bit D/A Converter, Low Cost		DAC1006LCD
AD561KD			DAC1006LCD
AD561SD			DAC1006LD
AD561TD			DAC1006LD
AD562AD/BIN	12-Bit D/A Converter		DAC1200HCD
AD562KD/BIN			DAC1200HCD
AD562SD/BIN			DAC1200HD
AD563AD/BIN	12-Bit D/A Converter	*DAC1265LCD	
AD563KD/BIN		*DAC1265LCD	
AD563SD/BIN		*DAC1265LD	
AD565JD/BIN		*DAC1265LCD	
AD565JN/BIN	Complete High Speed 12-Bit D/A Converter	*DAC1265LCN	
AD565KD/BIN		*DAC1264LCD	
AD565KN/BIN		*DAC1264LCD	
AD565SD/BIN		*DAC1264LD	
AD565TD/BIN		*DAC1264LD	
AD570JD	Low Cost, Complete 8-Bit A/D Converter		ADC0801LCD
AD570SD			ADC0801LD
AD571JD	10-Bit A/D Converter w/Reference		*ADC1001
AD571KD			*ADC1001
AD571SD			*ADC1001
AD572AD	12-Bit A/D Successive Approximation, Reference		ADC1210HCD
AD572BD			ADC1210HCD
AD572SD			ADC1210HCD
AD574JD	Fast Complete 12-Bit A/D Converter w/Microprocessor Interface		ADC1210HCD
AD574KD			ADC1210HCD
AD574LD			ADC1210HCD
AD574SD			ADC1210HCD
AD574TD			ADC1210HCD
AD574UD			ADC1210HCD
AD580JH	Low Drift Voltage Reference		LM336H
AD580KH			LM336H
AD580LH			LM336H
AD580MH			LM336AH
AD580SH			LM136H
AD580TH			LM136H

* To be announced.

Data Conversion/Acquisition Circuits Cross Reference Guide (Continued)

National Part Number	Function	National Direct Replacement	National Functional Replacement
ANALOG DEVICES (Continued)			
AD580UH			LM136AH
AD581JH	High Precision 10V Reference		LH0070CH
AD581KH			LH0070CH
AD581LH			LH0070CH
AD581SH			LH0070H
AD581TH			LH0070H
AD581UH			LH0070H
AD582KD	Sample/Hold Amplifier, Low Cost		LF398H, N
AD582KH			LF398H
AD582SD			LF198H
AD582SH			LF198H
AD583KD	Sample/Hold Gated Op Amp		LF398H, N
AD1408-7D	8-Bit Monolithic Multiplying D/A Converter	DAC0807LCJ	
AD1408-8D		DAC0808LCJ	
AD1408-9D			DAC0802LCJ
AD1508-8D		DAC0808LD	
AD1508-9D			DAC0802LD
AD7501JD	8-Channel Analog Multiplexer		LF11508D
AD7501JN			LF13508D
AD7501KD			LF11508D
AD7501SD			LF11508D
AD7502JD	Dual 4-Channel Analog Multiplexer		LF11509D
AD7502JN			LF13509D
AD7502KD			LF11509D
AD7502KN			LF13509ND
AD7502SD			LF11509D
AD7510DIJD	4 Independent SPST Analog Switches		LF11331D
AD7510DIJN			LF13331N
AD7510DIKD			LF11331D
AD7510DIKN			LF13331N
AD7510DISD			LF11331D
AD7516JN	Quad SPST Analog Switches		CD4066BCN
AN7516KN			CD4066BCN
AD7516SD			CD4066BMJ
AD7516TD			CD4066BMJ
AD7520JD	10-Bit Multiplying D/A Converter	DAC1022LCD	
AD7520JN		DAC1022LCN	
AD7520KD		DAC1021LCD	
AD7520KN		DAC1021LCN	
AD7520LD		DAC1020LCD	

Data Conversion/Acquisition Circuits Cross Reference Guide (Continued)

National Part Number	Function	National Direct Replacement	National Functional Replacement
ANALOG DEVICES (Continued)			
AD7520LN		DAC1020LCN	
AD7520SD		DAC1022LD	
AD7520TD		DAC1021LD	
AD7520UD		DAC1020LD	
AD7521JD	12-Bit Multiplying D/A Converter	DAC1222LCD	
AD7521JN		DAC1222LCN	
AD7521KD		DAC1221LCD	
AD7521KN		DAC1222LCN	
AD7521LD		DAC1220LCD	
AD7521LN		DAC1220LCN	
AD7521SD		DAC1222LD	
AD7521TD		DAC1221LD	
AD7521UD		DAC1221LD	
AD7522JD	10-Bit Buffered Multiplying D/A Converter		DAC1008LCD
AD7522JN			DAC1008LCN
AD7522KD			DAC1007LCD
AD7522KN			DAC1007LCN
AD7522LD			DAC1006LCD
AD7522LN			DAC1006LCN
AD7522SD			DAC1008LD
AD7522TD			DAC1007LD
AD7522UD			DAC1006LD
AD7523JN	8-Bit Multiplying D/A Converter, CMOS		DAC0808LCN
AD7523KN			DAC0808LCN
AD7523LN			DAC0808LCN
AD7524AD	8-Bit Buffered Multiplying D/A Converter		DAC0832LCD
AD7524BD			DAC0831LCD
AD7524CD			DAC0830LCD
AD7524JN			DAC0832LCN
AD7524KN			DAC0831LCN
AD7524LN			DAC0830LCN
AD7524SD			DAC0830LD
AD7524TD			DAC0830LD
AD7524UD			DAC0830LD
AD7530JD	10-Bit Multiplying D/A Converter, CMOS	DAC1022LCD	
AD7530JN		DAC1022LCN	
AD7530KD		DAC1021LCD	
AD7530KN		DAC1021LCN	
AD7530LD		DAC1020LCD	
AD7530LN		DAC1020LCN	

Data Conversion/Acquisition Circuits Cross Reference Guide (Continued)

National Part Number	Function	National Direct Replacement	National Functional Replacement
ANALOG DEVICES (Continued)			
AD7531JD	12-Bit Multiplying D/A Converter	DAC1222LCD	
AD7531JN		DAC1222LCN	
AD7531KD		DAC1221LCD	
AD7531KN		DAC1221LCN	
AD7531LD		DAC1220LCD	
AD7531LN		DAC1220LCN	
AD7533AD	10-Bit Multiplying D/A Converter, Low Cost	DAC1022LCD	
AD7533BD		DAC1021LCD	
AD7533CD		DAC1020LCD	
AD7533JN		DAC1022LCN	
AD7533KN		DAC1021LCN	
AD7533LN		DAC1020LCN	
AD7533SD		DAC1022LD	
AD7533TD		DAC1021LD	
AD7533UD		DAC1020LD	
AD7541AD	12-Bit Multiplying D/A Converter		DAC1219LCD
AD7541BD			DAC1218LCD
AD7541JN			DAC1219LCN
AD7541KN			DAC1218LCN
AD7541SD			DAC1219LD
AD7541TD			DAC1218LD
AD7570JD	10-Bit A/D Converter		*ADC1001LCD
AD7570LD			*ADC1001LCD
BURR-BROWN			
ADC80AG-10	10-Bit A/D, Low Cost		ADC1211HCD
ADC80AG-12	12-Bit A/D, Low Cost		ADC1210HCD
ADC80AGZ-10	10-Bit A/D, Low Cost		ADC1211HCD
ADC08AGZ-12	12-Bit A/D, Low Cost		ADC1210HCD
ADC82AG	8-Bit A/D, Low Cost, High Speed		ADC0801LCD
ADC82AM			ADC0801LCD
ADC85C-10	10-Bit A/D, Low Drift, High Speed		*ADC1001LCD
ADC85-10			*ADC1001LCD
ADC85C-12	12-Bit A/D, Low Drift, High Speed		ADC1210HCD
ADC85-12			ADC1210HCD
DAC80-CBI-I	12-Bit D/A, Low Cost	DAC1280HCD	
DAC80-CBI-V		DAC1280HCD	
DAC82KG	8-Bit D/A, Low Cost		DAC0800LCJ
DAC82BM			DAC0800LCJ
DAC82SM			DAC0800LD

* To be announced.

Data Conversion/Acquisition Circuits Cross Reference Guide (Continued)

National Part Number	Function	National Direct Replacement	National Functional Replacement
BURR-BROWN (Continued)			
DAC85-CBI-I	12-Bit D/A, Low Drift		DAC1285HCD
DAC85-CBI-V			DAC1285HCD
DAC85LD-CBI-I			DAC1285HCD
DAC85LD-CBI-V			DAC1285HCD
DAC87CBI	Wide Temperature Range 12-Bit D/A	DAC1285HD	
DAC87CBV		DAC1285HD	
DAC862BG-BIN	12-Bit D/A Converter		*DAC1264LCD
DAC862KG-BIN			*DAC1265LCD
DAC863BG-BIN	12-Bit D/A Converter with Reference	*DAC1264LCD	
DAC863KG-BIN		*DAC1265LCD	
DAC90-BG	8-Bit D/A, Monolithic		DAC0800LCJ
DAC90-SG			DAC0800LD
MP20	8080-SC/MP-Compatible 8-Bit A/D		ADC0816CCN
MP21	Universal μP-Compatible 12-Bit A/D		ADC0816CCN
MP-10	8-Bit D/A μP-Compatible 8080, S.C.		DAC1006LCD
MP-11	8-Bit D/A μP-Compatible 6800, 6502		DAC1006LCD
MPC8S	8-Channel MUX, CMOS		LF13508D
MPC4D	4-Channel Diff., MUX, CMOS		LF13509D
SHC80KP	S/H, Low Cost Complete		LF398H
SHC80BM			LF398H
SHC85	S/H, High Speed Complete		LF398H
SHC298AM	S/H, Low Cost Monolithic	LF398H	
VFC32KP	V/F, Low Cost Monolithic		LM331H
VFC32BM			LM331H
VFC32SM			LM131H
VFC42BP	Low Cost, Complete Hybrid		LM331AH
VFC52BP			LM331AH
MOTOROLA			
MC1405L	A/D Converter Subsystem		LF13300D
MC1408L6	8-Bit Multiplying D/A Converter	DAC0806LCJ	
MC1408L7		DAC0807LCJ	
MC1408L8		DAC0808LCJ	
MC1408P6		DAC0806LCN	
MC1408P7		DAC0807LCN	
MC1408P8		DAC0808LCN	
MC1508L8		DAC0808LD	
MC3408L	8-Bit Multiplying D/A Converter	DAC0806LCJ	
MC3410L	10-Bit Multiplying D/A Converter		DAC1020LCD
MC3410P			DAC1020LCN
MC3410CL			DAC1021LCD

*To be announced.

Data Conversion/Acquisition Circuits
Cross Reference Guide (Continued)

National Part Number	Function	National Direct Replacement	National Functional Replacement
MOTOROLA (Continued)			
MC3410CP			DAC1021LCN
MC3510L			DAC1020LD
PMI			
DAC-03ADX1(X2)	8 and 10-Bit Low Cost D/A Converter		DAC1020LCD
DAC-03BDX1(X2)			DAC1021LCD
DAC-03CDX1(X2)			DAC1022LCD
DAC-03DDX1(X2)			DAC1022LCD
DAC-08AQ	8-Bit High Speed Multiplying D/A Converter	DAC0802LD	
DAC-08Q		DAC0800LD	
DAC-08EQ		DAC0800LCJ	
DAC-08HQ		DAC0802LCJ	
DAC-08CQ		DAC0801LCJ	
DAC-100AA	8 or 10-Bit D/A Converter w/Reference		DAC1020LD
DAC-100AB			DAC1021LD
DAC-100AC			DAC1022LD
DAC-100BB			DAC1020LCD
DAC-100BC			DAC1021LCD
DAC-100CC			DAC1022LCD
DAC-100DD			DAC1022LCD
DAC-12AV	12-Bit High Speed D/A Converter		*DAC1265LD
DAC-12BV			*DAC1265LD
DAC-12EV			*DAC1265LCD
DAC-12FV			*DAC1265LCD
DAC-12GV			*DAC1265LCD
DAC-12HV			*DAC1265LCD
SSS1408A-6Q		DAC0806LCJ	
SSS1408A-7Q		DAC0807LCJ	
SSS1408A-8Q		DAC0808LCJ	
SSS1508A-8Q	8-Bit Multiplying D/A Converter	DAC0808LD	
MUX-88AQ	Protected 8-Channel BI-FET™ Analog Multiplexer		LF11508D
MUX-88BQ			LF11508D
MUX-88EQ			LF13508D
MUX-88FQ			LF13508D
REF-01AJ	10V Precision Voltage Reference		LH0070H
REF-01J			LH0070H
REF-01EJ			LH0070CH
REF-01HJ			LH0070CH
REF-01CJ			LH0070CH
REF-01DJ			LH0070CH

* To be announced.

Data Conversion/Acquisition Circuits Cross Reference Guide (Continued)

National Part Number	Function	National Direct Replacement	National Functional Replacement
PMI (Continued)			
REF-02AJ	5V Precision Voltage Reference/Thermometer		LM135H
REF-02J			LM135H
REF-02EJ			LM335H
REF-02HJ			LM335H
REF-02CJ			LM335H
REF-02DJ			LM335H
TEXAS INSTRUMENTS			
TL501N	3 1/2-Digit A/D Processor (0.1)		ADC3511CCN
TL505N	3-Digit A/D Converter		ADC3511CCN
TL487N	5-Step Analog Level Detector		LM3915N
TL489N	5-Step Analog Level Detector		LM3914N
TL490N	10-Step Linear Scale Indicator (O.C.)		LM3914N
TL491N	10-Step Linear Scale Indicator (E.P.U.)		LM3914N
TL507P	7-Bit A/D Converter		ADC0804LCN
ADC0816J			ADC0816LD
ADC0816CJ			ADC0816CCJ
ADC0816CN			ADC0816CCN
ADC0817CN			ADC0817CCN

Voltage Reference Selection Guide

Reverse Breakdown Voltage V_R at I_R	Device	Voltage Tolerance Max, $T_A = 25°C$	Voltage Temperature Drift-ppm/°C Max or mV Max Change Over Temperature Range		Current Range, I_R	Output Dynamic Impedance (Max)
			Drift (Max)	Temperature Range		
1.22	LM113	±5%	100 ppm typ	−55°C to +125°C	500 μA to 20 mA	0.8Ω
1.22	LM313	±5%	100 ppm typ	0°C to +70°C	500 μA to 20 mA	0.8Ω
1.22	LM113-1	±1%	50 ppm typ	−55°C to +125°C	500 μA to 20 mA	0.8Ω
1.22	LM113-2	±2%	50 ppm typ	−55°C to +125°C	500 μA to 20 mA	0.8Ω
1.235	LM185	±1%	20 ppm typ	−55°C to +125°C	1 mA to 20 mA	0.2Ω
1.235	LM285	±1%	20 ppm typ	−25°C to +85°C	1 mA to 20 mA	0.2Ω
1.235	LM385B	±1%	20 ppm typ	0°C to ±70°C	1 mA to 20 mA	0.2Ω
1.235	LM385	−2.5, +2	20 ppm typ	0°C to +70°C	1 mA to 20 mA	0.4Ω
2.49	LM136	±2%	18 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
2.49	LM136A	±1%	18 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
2.49	LM236	±2%	9 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
2.49	LM236A	±1%	9 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
2.49	LM336	±4%	6 mV	0°C to +70°C	400 μA to 10 mA	1Ω
2.49	LM336B	±2%	6 mV	0°C to +70°C	400 μA to 10 mA	1Ω
5.0	LM136-5.0	±2%	36 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
5.0	LM136A-5.0	±1%	36 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
5.0	LM236-5.0	±2%	18 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
5.0	LM236A-5.0	±1%	18 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
5.0	LM336-5.0	±4%	12 mV	0°C to +70°C	400 μA to 10 mA	1Ω
5.0	LM336B-5.0	±2%	12 mV	0°C to +70°C	400 μA to 10 mA	1Ω
6.90	LM129A	+3%, −2%	10 ppm	−55°C to +125°C	0.6 mA to 15 mA	1Ω
6.90	LM129B	+3%, −2%	20 ppm	−55°C to +125°C	0.6 mA to 15 mA	1Ω
6.90	LM129C	+3%, −2%	50 ppm	−55°C to +125°C	0.6 mA to 15 mA	1Ω
6.90	LM329B	±5%	20 ppm	0°C to +70°C	0.6 mA to 15 mA	2Ω
6.90	LM329C	±5%	50 ppm	0°C to +70°C	0.6 mA to 15 mA	2Ω
6.90	LM329D	±5%	100 ppm	0°C to +70°C	0.6 mA to 15 mA	2Ω
6.95	LM199A	+1%, −2%	0.5 ppm	−55°C to +125°C	0.5 mA to 10 mA	1Ω
6.95	LM199A	+1%, −2%	10 ppm	85°C to 125°C	0.5 mA to 10 mA	1Ω
6.95	LM199	+1%, −2%	1 ppm	−55°C to +85°C	0.5 mA to 10 mA	1Ω
6.95	LM199	+1%, −2%	15 ppm	85°C to 125°C	0.5 mA to 10 mA	1Ω
6.95	LM299A	+1%, −2%	0.5 ppm	−25°C to +85°C	0.5 mA to 10 mA	1Ω
6.95	LM299	+1%, −2%	1 ppm	−25°C to +85°C	0.5 mA to 10 mA	1Ω
6.95	LM399A	±5%	1 ppm	0°C to +70°C	0.5 mA to 10 mA	1.5Ω
6.95	LM399	±5%	2 ppm	0°C to +70°C	0.5 mA to 10 mA	1.5Ω
6.95	LM3999	±5%	5 ppm	0°C to +70°C	0.6 mA to 10 mA	2.2Ω
10.00	LH0070-0	0.1%	20 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.00	LH0070-1	0.1%	10 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.00	LH0070-2	0.05%	4 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.24	LH0071-0	0.1%	20 mV	−25°C to +85°C	0 mA to 20 mA	1Ω

Voltage Reference Selection Guide (Continued)

Reverse Breakdown Voltage V_R at I_R	Device	Voltage Tolerance Max, $T_A = 25°C$	Voltage Temperature Drift-ppm/°C Max or mV Max Change Over Temperature Range		Current Range, I_R	Output Dynamic Impedance (Max)
			Drift (Max)	Temperature Range		
10.24	LH0071-1	0.1%	10 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.24	LH0071-2	0.05%	4 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
Adjustable— 5V, 6V, 10V, 12V, 15V	LH0075	±0.5%	0.003%/°C typ	−55°C to +125°C	1 mA to 200 mA	1Ω
Adjustable— 5V, 6V, 10V, 12V, 15V	LH0075C	±1%	0.003%/°C typ	0°C to +70°C	1 mA to 200 mA	1Ω
Adjustable— −5V, −6V, −10V, −12V, −15V	LH0076	±0.5%	0.003%/°C typ	−55°C to +125°C	1 mA to 200 mA	1Ω
Adjustable— −5V, −6V, −10V, −12V, −15V	LH0076C	±1%	0.003%/°C typ	0°C to +70°C	1 mA to 200 mA	1Ω

Reverse Breakdown Voltage V_R at I_R	Device	Voltage Tolerance Max, $T_A = 25°C$	Voltage Temperature Drift-ppm/°C Max or mV Max Change Over Temperature Range		Current Range, I_R	Output Dynamic Impedance (Max)
			Drift (Max)	Temperature Range		
LOW CURRENT ZENER DIODES						
1.8	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
2.0	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
2.2	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
2.4	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
2.7	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
3.0	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
3.3	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
3.6	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
3.9	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
4.3	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
4.7	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
5.1	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω
5.6	LM103	±10%	−5 mV/°C typ	−55°C to +125°C	10 μA to 10 mA	25Ω

Section 2

Active Filters

2

Section Contents

AF99 Tunable Bandpass Filter/Oscillator

General Description

The AF99 is a low frequency bandpass filter that is tunable with a single resistor. Additionally, with a few external components, the AF99 can be used as an oscillator. Therefore, one device can be used as a complete tone generating and receiving system. The filter bandwidth is selected by one of two external jumpers to be 2.5 Hz or 5.0 Hz. The frequency adjustment range is from 60 Hz to 270 Hz. These features make the device ideal for tone signaling, tone activated industrial control systems, tone activated communication systems, two-wire sensing and control, alarms, and the like. An internal biasing amplifier is included to facilitate using the device on dual supplies or single ended supply applications. The supply current drain is low to allow for remote or battery operated systems.

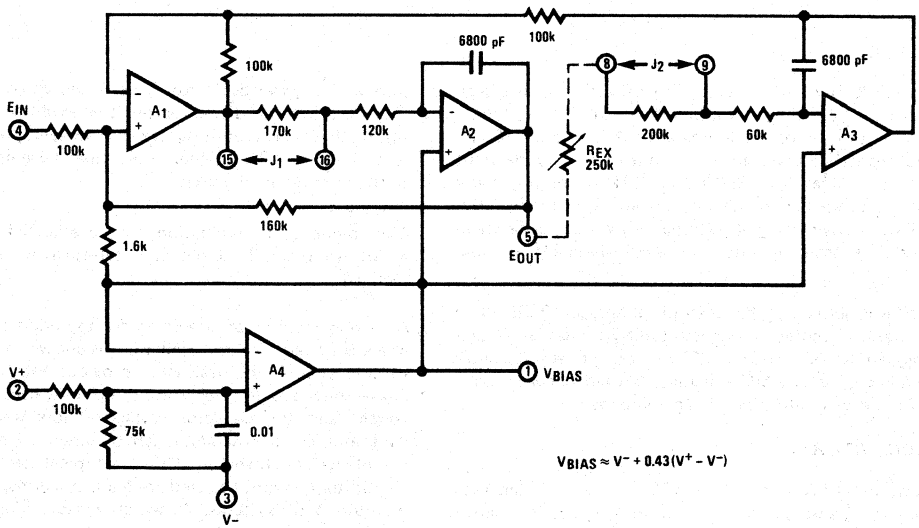
Features

- Adjustable center frequency
- Bandwidth options 2.5 Hz or 5 Hz
- Bandwidth independent of frequency setting
- Fixed voltage gain independent of settings
- Single or split supply operation
- Low current drain
- Low cost

Applications

- Tone control systems
- Alarm systems
- Tone activated squelch
- Remote sensing and control systems
- Two-wire signaling
- Doppler shift burglar alarms

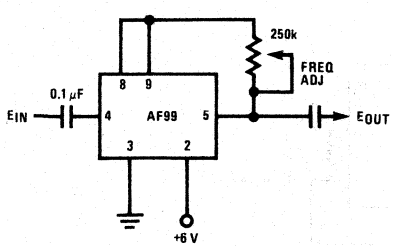
Schematic Diagram



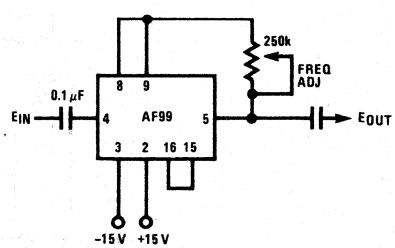
$V_{BIAS} \approx V^- + 0.43(V^+ - V^-)$

Schematic Diagram

Typical Applications



80 Hz TO 130 Hz TUNABLE BANDPASS FILTER
BANDWIDTH = 2.5 Hz, SINGLE SUPPLY



125 Hz TO 270 Hz TUNABLE BANDPASS FILTER
BANDWIDTH = 5 Hz, DUAL SUPPLIES

Absolute Maximum Ratings

Supply Voltage Between Pins 2 and 3	32 V
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−55°C to +125°C
Short Circuit Duration, Any Pin	continuous
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Specifications

These specifications apply at +25°C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Tuning Range	See Connection table	60		270	Hz
Voltage Gain	R_L = 10 kΩ R_S = 50 Ω		4		dB
Input Impedance			100		kΩ
Bandwidth	J_1 – IN J_1 – OUT	4.0 2.0	5.0 2.5	6.0 3.0	Hz Hz
Power Supply	pin 2 to pin 3	6		32	V
Power Supply Current	V+ = +15 V V− = −15 V		1.5 1.5	3.0 3.0	mA mA

General Information

FILTER

The AF99 is a bi-quad type active filter which has been internally connected as a bandpass filter with "fixed" bandwidth options. By jumpering pin 15 and pin 16, the total resistance between the output of A_1 and the input of A_2 is reduced from 290 kΩ to 120 kΩ. This nominally will change the bandwidth from 2.5 Hz to 5 Hz. Obviously, by placing an external resistor or pot between these pins, the bandwidth can be adjusted between these limits.

Similarly, jumper J_2 between pin 8 and pin 9 will allow for various center frequency tuning ranges. Although designed for use with a 250 kΩ pot to adjust center frequency, up to 1 MΩ pot may be used between pin 5 and pin 8. A ten-turn pot is recommended.

OSCILLATOR

From the schematic of the AF99, it can be seen that from the input, pin 4, to the output, pin 5, is negative feedback. However, by inserting an additional amplifier, connected in the inverting mode, the AF99 can be made into a sine wave oscillator. This is shown in figure 1. The back-to-back diodes across the external amplifier insure that signal limiting takes place and the output is a sine wave. This signal could then be amplified or buffered to drive long lines.

The frequency of oscillation can be adjusted by using a pot from pin 8 to pin 5. A ten-turn pot is recommended.

A second method of providing for the additional 180° phase shift required for oscillation is shown in figure 2. In this circuit, the transistor provides the additional phase shift due to the relationship between the base voltage and the collector voltage at low frequencies. Additionally, the oscillator can be gated on or off by use of the switch shown. This is a typical example of a circuit that might be used in burglar alarms, or plant monitoring of systems. A switch closure identifies an alarm condition and the frequency indicates where the alarm occurs.

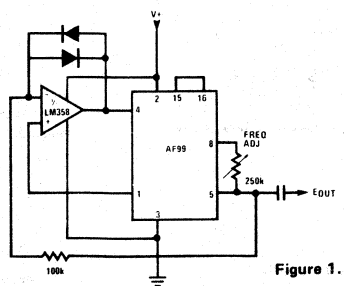


Figure 1. Oscillator with Signal Limiting (E_{OUT} = 0.8 Vrms, 6V ≤ V_{CC} ≤ 32 V)

Connections Table

J_1	J_2	Tuning Range (Hz)	Bandwidth (Hz)
0	0	60 - 80	2.5
0	1	80 - 130	2.5
1	0	100 - 130	5.0
1	1	125 - 270	5.0

Typical Applications

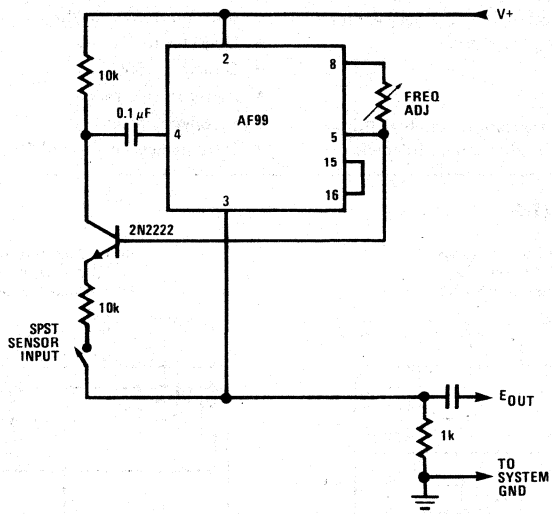


Figure 2. 2-Wire Tone Encoder

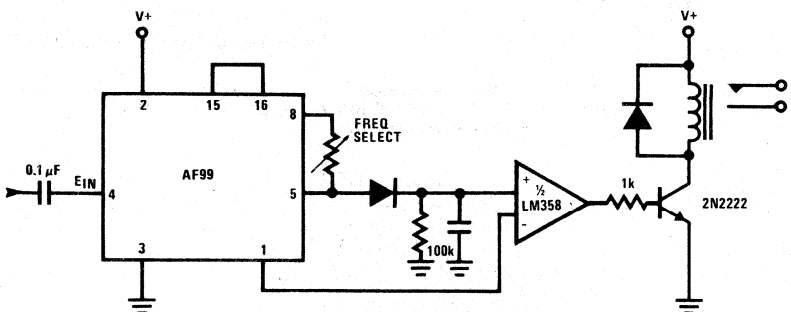


Figure 3. Tone Decoder with Relay Output

National Semiconductor

AF100 Universal Active Filter

General Description

The AF100 state variable active filter is a general second order lumped RC network. Only four external resistors program the AF100 for specific second order functions. Lowpass, highpass, and bandpass functions are available simultaneously at separate outputs. Notch and allpass functions are available by summing the outputs in the uncommitted output summing amplifier. Higher order systems are realized by cascading AF100 active filters with appropriate programming resistors.

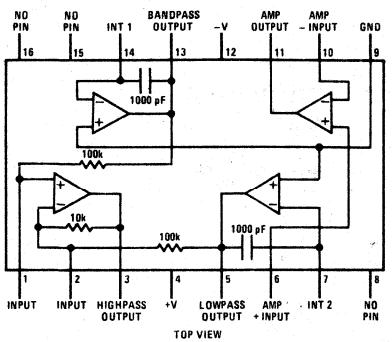
Any of the classical filter configurations, such as Butterworth, Bessel, Cauer, and Chebyshev can be formed.

Features

- Military or commercial specifications
- Independent Q, frequency, gain adjustments
- Low sensitivity to external component variation
- Separate lowpass, highpass, bandpass outputs
- Inputs may be differential, inverting, or non-inverting
- Allpass and notch outputs may be formed using uncommitted amplifier
- Operates to 10 kHz
- Q range to 500
- Power supply range ±5V to ±18V
- Frequency accuracy ±1% unadjusted
- Q frequency product $\leq$ 50,000

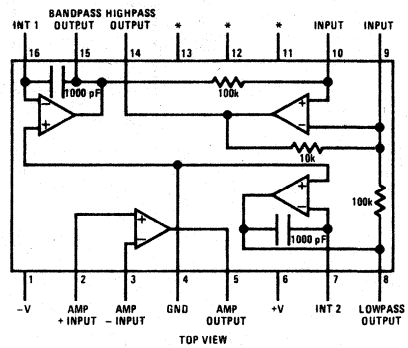
Connection Diagrams

Ceramic Dual-In-Line Package
AF100-1CJ, AF100-2CJ
NS Package Number HY13A



TOP VIEW

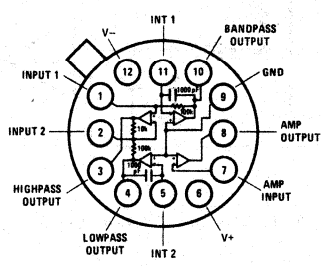
Plastic Dual-In-Line Package
AF100-1CN, AF100-2CN
NS Package Number N16A



TOP VIEW

*Note: Internally connected. Do not use.

Metal Can Package
AF100-1CG, AF100-1G, AF100-2CG, AG100-2G
NS Package Number H12A



TOP VIEW

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	900 mW/Package (500 mW/Amp)
Differential Input Voltage	±36V
Output Short Circuit Duration (Note 1)	Infinite
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Temperature	
AF100-1CJ, AF100-2CJ, AF100-1CG, AF100-2CG, AF100-1CN, AF100-2CN	−25°C to +85°C
AF100-1G, AF100-2G	−55°C to +125°C
Storage Temperature	
AF100-1G, AF100-2G	−65°C to +125°C
AF100-1CG, AF100-2CG, AF100-1CJ, AF100-2CJ, AF100-1CN, AF100-2CN	−25°C to +100°C

Electrical Characteristics (Complete Active Filter) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_C \times Q \leq 50{,}000$			10k	Hz
Q Range	$f_C \times Q \leq 50{,}000$			500	Hz/Hz
f_O Accuracy					
AF100-1, AF100-1C	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±2.5	%
AF100-2, AF100-2C	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±1.0	%
f_O Temperature Coefficient			±50	±150	ppm/°C
Q Accuracy	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±7.5	%
Q Temperature Coefficient			±300	±750	ppm/°C
Power Supply Current	$V_S = ±15V$		2.5	4.5	mA

Electrical Characteristics (Internal Op Amp) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance			2.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2k$, $V_{OUT} = ±10V$	25	160		V/mV
Output Voltage Swing	$R_L = 10\ k\Omega$	±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range		±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		dB
Output Short Circuit Current			25		mA
Slew Rate (Unity Gain)			0.6		V/μs
Small Signal Bandwidth			1		MHz
Phase Margin			60		Degrees

Note 1: Any of the amplifiers can be shorted to ground indefinitely, however more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: Specifications apply for $V_S = ±15V$, over −25°C to +85°C for the AF100-1C and AF100-2C and over −55°C to +125°C for the AF100-1 and AF100-2, unless otherwise specified.

Note 3: Specifications apply for $V_S = ±15V$, $T_A = 25°C$.

Applications Information

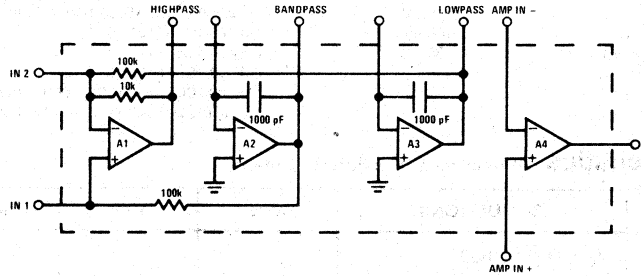


FIGURE 1. AF100 Schematic

CIRCUIT DESCRIPTION AND OPERATION

A schematic of the AF100 is shown in *Figure 1.* Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input. Amplifier A4 is an uncommitted amplifier.

By adding external resistors the circuit can be used to generate the second order system

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_0 = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_0}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(highpass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer function becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(bandpass)}$$

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(lowpass)}$$

Using proper input and output connections the circuit can also be used to generate the transfer functions for a notch and allpass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals 1, and a_3 equals ω_Z^2. The transfer function becomes:

$$T(s) = \frac{s^2 + \omega_Z^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(notch)}$$

In the allpass transfer function $a_1 = 1$, $a_2 = -\omega_0/Q$ and $a_3 = \omega_0^2$. The transfer function becomes:

$$T(s) = \frac{s^2 - \frac{\omega_0}{Q} s + \omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(allpass)}$$

COMMON CONFIGURATIONS

The specific transfer functions for some of the most useful circuit configurations using the AF100 are illustrated in *Figures 2 through 8.* Also included are the gain equations for each transfer function in the frequency band of interest, the Q equation, center frequency equation and the Q determining resistor equation.

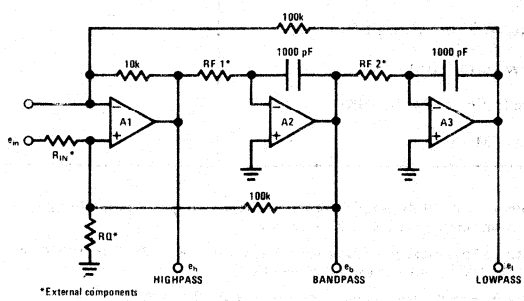


FIGURE 2. Non-inverting Input ($Q > Q_{MIN}$, See Q Tuning Section)

Applications Information (Continued)

a) Non-inverting input *(Figure 2)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\frac{1.1}{1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\frac{1.1}{1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2\left[\frac{1.1}{1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\left[\frac{1.1}{1+\frac{10^5}{RQ}+\frac{10^5}{R_{IN}}}\right]\omega_1 + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{11}{\left(1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{1.1}{\left(1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{\left(1+\frac{10^5}{RQ}+\frac{10^5}{R_{IN}}\right)}{\left(1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}\right)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left(\frac{1+\frac{10^5}{R_{IN}}+\frac{10^5}{RQ}}{1.1}\right)\sqrt{0.1\left(\frac{\omega_2}{\omega_1}\right)}$$

$$RQ = \frac{10^5}{\left(\frac{1.1Q}{\sqrt{0.1\frac{\omega_2}{\omega_1}}}\right) - 1 - \frac{10^5}{R_{IN}}}$$

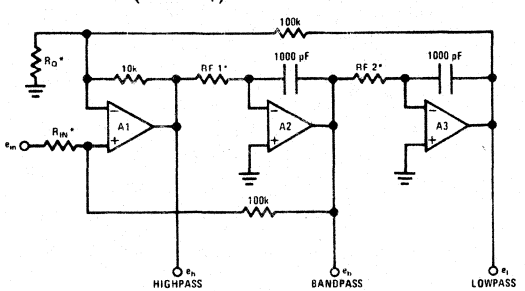


FIGURE 3. Non-Inverting Input (Q < Q_{MIN}, See Q Tuning Section)

b) Non-inverting input *(Figure 3)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\frac{1.1+\frac{10^4}{RQ}}{1+\frac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\frac{1.1+\frac{10^4}{RQ}}{1+\frac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2\left[\frac{1.1+\frac{10^4}{RQ}}{1+\frac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1+\frac{10^4}{RQ}}{1+\frac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{1.1+\frac{10^4}{RQ}}{0.1\left(1+\frac{R_{IN}}{10^5}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{1.1+\frac{10^4}{RQ}}{1+\frac{R_{IN}}{10^5}}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{1+\frac{10^5}{R_{IN}}}{1+\frac{R_{IN}}{10^5}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1+\frac{10^5}{R_{IN}}}{1.1+\frac{10^4}{RQ}}\right]\sqrt{0.1\frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^4}{\left(1+\frac{10^5}{R_{IN}}\right)\left(\frac{\sqrt{0.1\frac{\omega_2}{\omega_1}}}{Q}\right) - 1.1}$$

Applications Information (Continued)

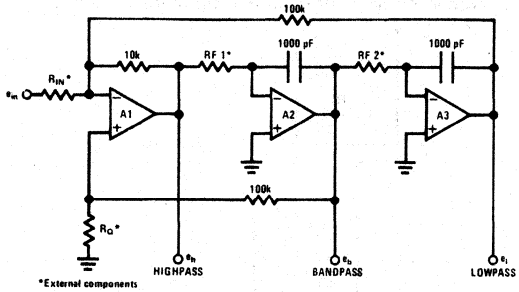


FIGURE 4. Inverting Input

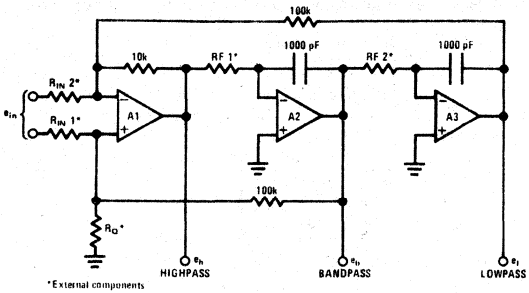


FIGURE 5. Differential Input

c) Inverting input *(Figure 4)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{-s^2 \dfrac{10^4}{R_{IN}}}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{s\,\omega_1 \dfrac{10^4}{R_{IN}}}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{-\omega_1\,\omega_2 \dfrac{10^4}{R_{IN}}}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \dfrac{10^4}{R_{IN}}}{1 + \dfrac{10^5}{R_Q}} \right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s \to 0} = -\frac{10^5}{R_{IN}} \quad \text{(lowpass)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = -\frac{10^4}{R_{IN}} \quad \text{(highpass)}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_0} = \frac{\dfrac{10^4}{R_{IN}}\left(1 + \dfrac{10^5}{RQ}\right)}{1.1 + \dfrac{10^4}{R_{IN}}} \quad \text{(bandpass)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \dfrac{10^5}{RQ}}{1.1 + \dfrac{10^4}{R_{IN}}} \right] \sqrt{0.1 \frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\dfrac{Q}{\sqrt{0.1 \dfrac{\omega_2}{\omega_1}}} \left(1.1 + \dfrac{10^4}{R_{IN}}\right) - 1}$$

d) Differential input *(Figure 5)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \dfrac{10^4}{R_{IN2}}}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1 \dfrac{10^4}{R_{IN2}}}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2 \dfrac{10^4}{R_{IN2}}}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \dfrac{10^4}{R_{IN2}}}{1 + \dfrac{10^5}{RQ} + \dfrac{10^5}{R_{IN1}}} \right] + 0.1\,\omega_1\omega_2$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \dfrac{10^5}{RQ} + \dfrac{10^5}{R_{IN1}}}{1.1 + \dfrac{10^4}{R_{IN2}}} \right] \sqrt{0.1 \frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\dfrac{Q}{\sqrt{0.1 \dfrac{\omega_2}{\omega_1}}} \left(1.1 + \dfrac{10^4}{R_{IN2}}\right) - 1 - \dfrac{10^5}{R_{IN1}}}$$

Applications Information (Continued)

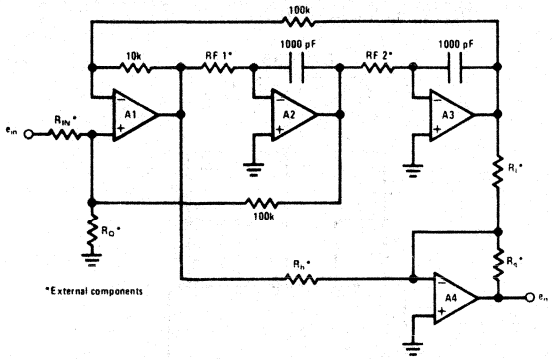


FIGURE 6. Output Notch Using All Four Amplifiers

e) Output notch *(Figure 6)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{(s^2 + \omega_Z{}^2)\left[\frac{1.1}{1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}}\right]\frac{R_g}{R_h}}{s^2 + s\,\omega_1\left[\frac{1.1}{1 + \frac{10^5}{RQ} + \frac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\omega_Z = \omega_0\sqrt{\frac{10\,R_h}{R_Q}}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to 0} = \frac{11}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}\right)}\frac{R_g}{R_Q}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to \infty} = \frac{1.1}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}\right)}\frac{R_g}{R_h}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega = \omega_Z} = 0$$

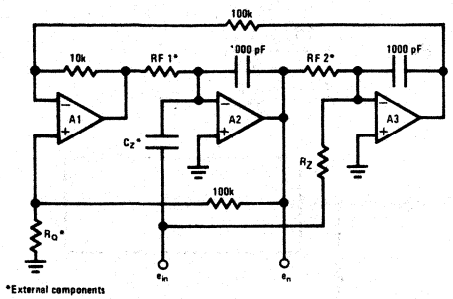


FIGURE 7. Input Notch Using Three Amplifiers

j) Input notch *(Figure 7)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = -\frac{\frac{C_Z}{10^{-9}}\left[s^2 + \omega_Z{}^2\right]}{s^2 + s\,\omega_1\left[\frac{1.1\,RQ}{10^5 + RQ}\right] + \omega_0{}^2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_Z = \omega_0\sqrt{\frac{RF2 \times 10^{-9}}{R_Z\,C_Z}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to 0} = -\frac{R_{F2}}{R_Z}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to \infty} = -\frac{C_Z}{10^{-9}}$$

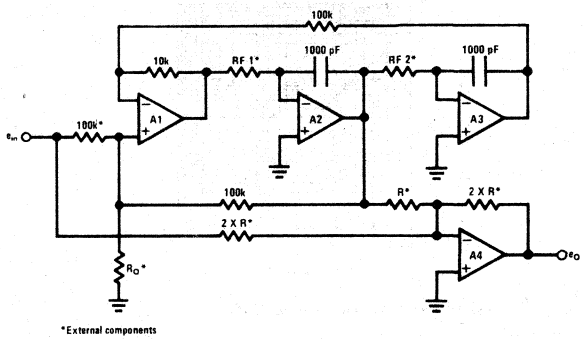


FIGURE 8. Allpass

g) Allpass *(Figure 8)* transfer function equations are:

$$\frac{e_o}{e_{IN}} = -\left[\frac{s^2 - s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{RQ}}\right] + \omega_0{}^2}{s^2 + s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{RQ}}\right] + \omega_0{}^2}\right]$$

$$Q = \frac{2 + \frac{10^5}{RQ}}{1.1}\sqrt{0.1\,\frac{\omega_2}{\omega_1}}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

Time delay at $\omega_0 = \frac{2Q}{\omega_0}$ seconds

FREQUENCY TUNING

To tune the AF100 two resistors are required for frequencies between 200 Hz and 10 kHz. For lower frequencies "T" tuning or addition of external capacitors

Applications Information (Continued)

is required. Using external capacitors allows the user to go as low in frequency as he desires. "T" tuning and external capacitors can be used together.

Two resistor tuning for 200 Hz to 10 kHz

$$R_f = \frac{50.33 \times 10^6}{f_o}\ \Omega$$

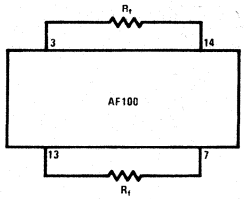
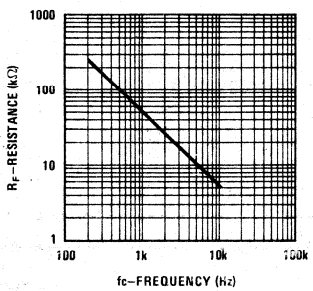


FIGURE 9. Resistive Tuning

GRAPH A. Resistive Tuning



"T" resistive tuning for $f_O < 200$ Hz

$$R_s = \frac{R_t^2}{R_f - 2R_t} \qquad R_t < \frac{R_F}{2}$$

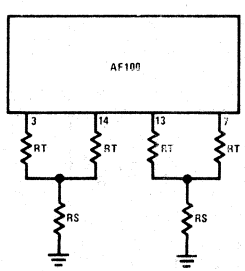
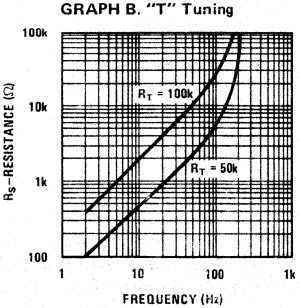


FIGURE 10. T Tuning

GRAPH B. "T" Tuning



RC tuning for $f_O < 200$ Hz

$$R_f = \frac{0.05033}{f_o\,(C + 1 \times 10^{-9})}$$

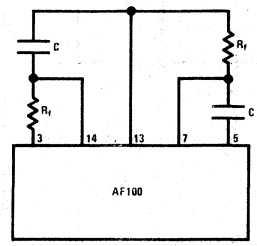
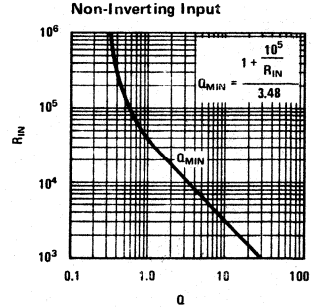


FIGURE 11. Low Frequency RC Tuning

Q TUNING

To tune the Q of an AF100 requires one resistor from pins 1 or 2 to ground. The value of the Q tuning resistor depends on the input connection and input resistance as well as the value of the Q. The Q of the unit is inversely proportional to resistance to ground at pin 1 and directly proportional to resistance to ground from pin 2.

GRAPH C. Q_{MIN}, Non-Inverting Input



For $Q > Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}}$$

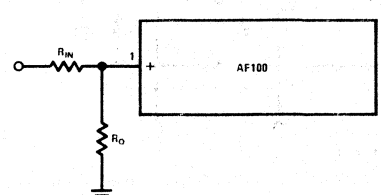
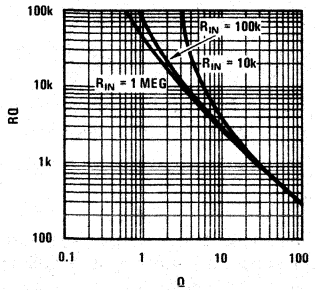


FIGURE 12. Q Tuning for $Q > Q_{MIN}$, Non-Inverting Input

Applications Information (Continued)

GRAPH D. Q > Q_{MIN}, Non-Inverting Input



For $Q < Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^4}{\left(1 + \frac{10^5}{R_{IN}}\right)} - 1.1$$
$$0.3162 \quad Q$$

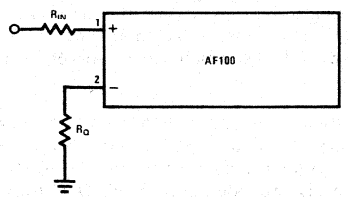
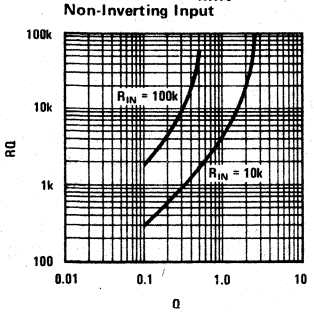


FIGURE 13. Q Tuning for $Q < Q_{MIN}$, Non-Inverting Input

GRAPH E. $Q < Q_{MIN}$, Non-Inverting Input



For any Q in inverting mode:

$$RQ = \frac{10^5}{3.16Q \cdot \left(1.1 + \frac{10^4}{R_{IN}}\right) - 1}$$

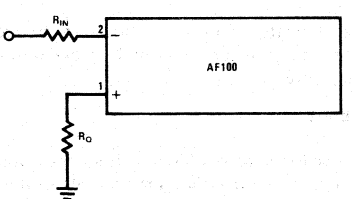
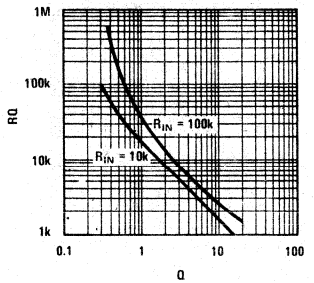


FIGURE 14. Q Tuning Inverting Input

GRAPH F. Q Tuning, Inverting Input



NOTCH TUNING

Two methods to generate notches are the RC input and lowpass/highpass summing. The RC input method requires adding a capacitor and resistor connected to the two integrator inputs. The capacitor connects to "Int 1" and the resistor connects to "Int 2." The output summing requires two resistors connected to the lowpass and highpass output.

For input RC notch tuning:

$$R_Z = \frac{R_F \times 10^{-9}}{C_Z} \left(\frac{f_O}{f_Z}\right)^2$$

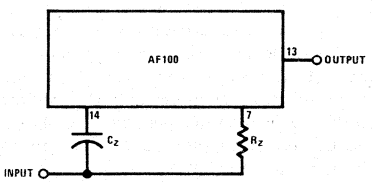
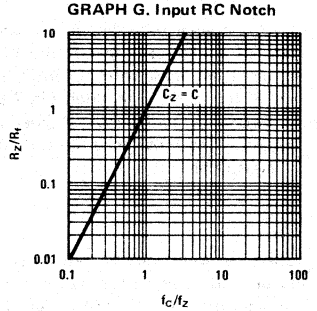


FIGURE 15. Input RC Notch

GRAPH G. Input RC Notch



For output notch tuning:

$$R_{HP} = \left(\frac{f_Z}{f_O}\right)^2 \frac{R_{LP}}{10}$$

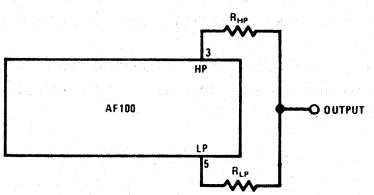
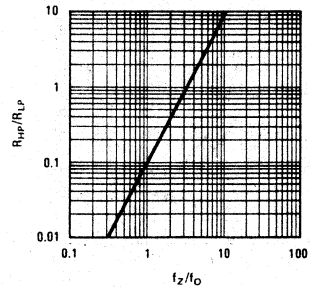


FIGURE 16. Output Notch

Applications Information (Continued)

GRAPH H. Output Notch



TUNING TIPS

In applications where 2 to 3% accuracy is not sufficient to provide the required filter response, the AF100 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the bandpass (pin 13) output.

Before any tuning is attempted the lowpass (pin 7) output should be checked to see that the output is not clipping. At the center frequency of the section the lowpass output is 10 dB higher than the bandpass output and 20 dB higher than the highpass. This should be kept in mind because if clipping occurs the results obtained when tuning will be incorrect.

Frequency Tuning

By adjusting the resistance between pins 7 and 13 the center frequency of a section can be adjusted. If the input is through pin 1 the phase shift at center frequency will be 180° and if the input is through pin 2 the phase shift at center frequency will be 0°. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

"Q" Tuning

The "Q" is tuned by adjusting the resistance between pin 1 or 2 and ground. Low Q tuning resistors will be from pin 2 to ground ($Q < 0.6$). High Q tuning resistors will be from pin 1 to ground. To tune the Q correctly the signal source must have an output impedance very much lower than the input resistance of the filter since the input resistance affects the Q. The input must be driven through the same resistance the circuit will see to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right) \times (f_O)$$

where f_O = center frequency

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q}\right) \times (f_O)$$

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair the notch can be tuned by adjusting the ratio of the summing resistors (lowpass/highpass summing) or the input resistance (input RC).

In either case the signal is connected to the input and the proper resistor is adjusted for a null at the output.

Special Cases

When using the input RC notch the unit cannot be tuned through the normal input so an additional 100k resistor can be added at pin 1 and the unit can be tuned normally. Then the 100k input resistor should be grounded and the notch tuned through the normal RC input.

An alternative way of tuning is to tune using the Q resistor as the input. This requires the Q resistor be lifted from ground and connecting the signal source to the normally grounded end of the Q resistor. This has the problem that when the Q resistor is grounded after tuning, its value is decreased by the output impedance of the source. This technique has the advantage of not requiring an additional resistor.

TUNING PROCEDURE (See *Figure 17*)

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the lowpass output pin 5 (AF100J).

Adjust the resistance between pins 13 and 7 until the phase shift between input and bandpass output is 180°.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

Zero Tuning

Set the oscillator output to the zero frequency and tune the zero resistor for a null at the output of the summing amplifier.

Gain Adjust

Set the oscillator to any desired frequency and the gain can be adjusted by measuring the output of the summing amplifier and adjusting the feedback resistance.

Applications Information (Continued)

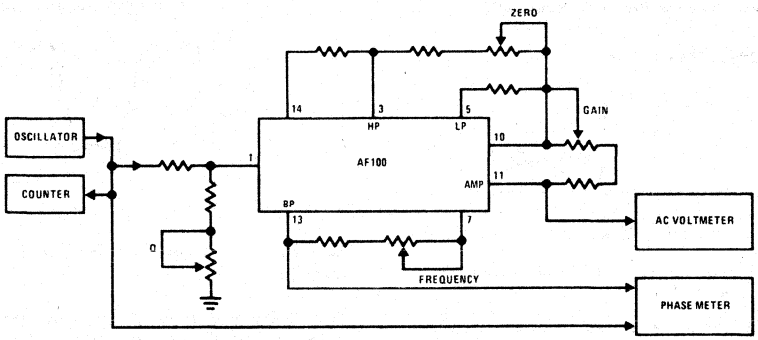


FIGURE 17. Filter Tuning Setup

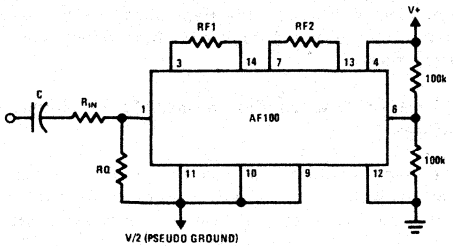


FIGURE 18. Single Power Supply Connection Using Uncommitted Amplifier to Split Supply

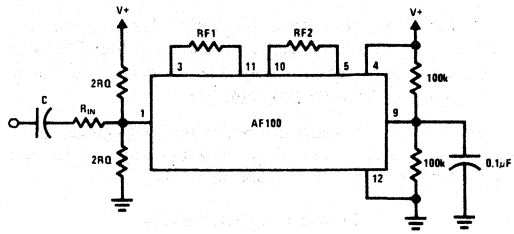
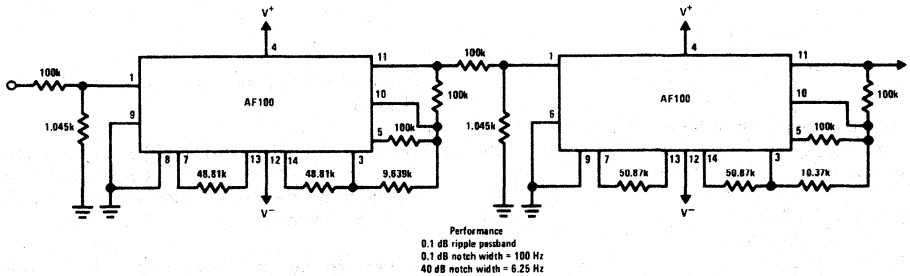
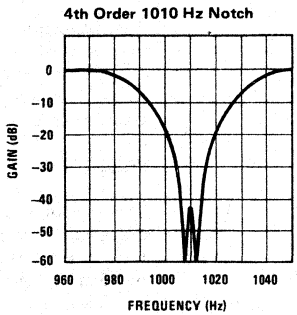


FIGURE 19. Single Power Supply Connection Using Resistive Dividers





STAGE 1

F_C = 1031.1 Hz
Q = 28.34
F_Z = 1012.2 Hz

STAGE 2

F_C = 989.3 Hz
Q = 28.34
F_Z = 1007.8 Hz

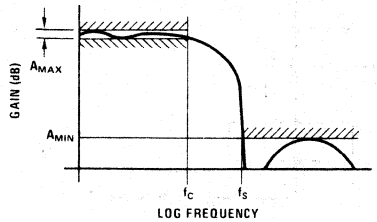
FIGURE 20. 1010 Hz Notch—Telephone Holding Tone Reject Filter

FILTER DESIGN

Since most filter tables are in terms of a normalized lowpass prototype, the filter to be designed is usually reduced to a lowpass prototype. After the lowpass transfer function is found, it is transformed to obtain the transfer function for the actual filter desired. *Graph I* shows the lowpass amplitude response which can be defined by four quantities.

Applications Information (Continued)

GRAPH I. Lowpass Prototype Response



A_{MAX} = the maximum peak to peak ripple in the passband.

A_{MIN} = the minimum attenuation in the stopband.

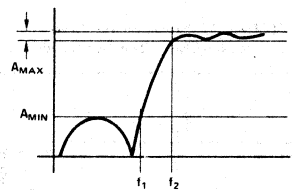
f_C = the passband cutoff frequency.

f_S = the stopband start frequency.

By defining these four quantities for the lowpass prototype the normalized pole and zero locations and the Q (quality) of the poles can be determined from tables or by computer programs.

To obtain the lowpass prototype for the highpass filter (*Graph J*) A_{MAX} and A_{MIN} are the same as for the lowpass case but $f_C = 1/f_2$ and $f_S = 1/f_1$.

GRAPH J. Highpass Response



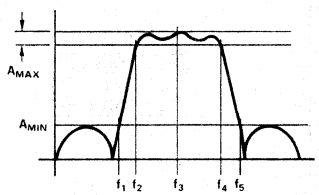
To obtain the lowpass prototype for a bandpass filter (*Graph K*) A_{MAX} and A_{MIN} are the same as for the lowpass case but

$$f_C = 1 \quad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$ i.e. geometric symmetry

$f_5 - f_1$ = A_{MIN} bandwidth
$f_4 - f_2$ = Ripple bandwidth

GRAPH K. Bandpass Response

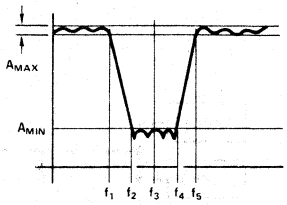


To obtain the lowpass prototype for the notch filter (*Graph L*) A_{MAX} and A_{MIN} are the same as for the lowpass case and

$$f_C = 1 \qquad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$

GRAPH L. Notch Response



Normalized Lowpass Transformed To Un-Normalized Lowpass

The normalized lowpass filter has the passband edge normalized to unity. The un-normalized lowpass filter instead has the passband edge at f_C. The normalized and un-normalized lowpass filters are related by the transformation $s = s\omega_c$. This transforms the normalized passband edge $s = j$ to the un-normalized passband edge $s = j\omega_C$.

Normalized Lowpass Transformed To Un-Normalized Highpass

The transformation that can be used for lowpass to highpass is $S = \omega_C/s$. Since S is inversely proportional to s, the low frequency and high frequency responses are interchanged. The normalized lowpass $1/(S^2 + S/Q+1)$ transforms to the un-normalized highpass

$$\frac{s^2}{s^2 + \frac{\omega_C}{Q}s + \omega_C{}^2}$$

Normalized Lowpass Transformed To Un-Normalized Bandpass

The transformation that can be used for lowpass to bandpass is $S = (s^2 + \omega_0{}^2)$ BWs where $\omega_0{}^2$ is the center frequency of the desired bandpass filter and BW is the ripple bandwidth.

Normalized Lowpass Transformed To Un-Normalized Bandstop (Or Notch)

The bandstop filter has a reciprocal response to a bandpass filter. Therefore a bandstop filter can be obtained by first transforming the lowpass prototype to a highpass and then performing the bandpass transformation.

SELECTION OF TRANSFER FUNCTION

The selection of a function which approximates the shape of the response desired is a complicated process. Except in the simplest cases it requires the use of tables or computer programs. The form of the transfer function desired is in terms of the pole and zero locations. The most common approximations found in tables are Butterworth, Tschebycheff, Elliptic, and Bessel. The decision as to which approximation to use is usually a function of the requirements and system objectives. Butterworth filters are the simplest but have the disadvantage of requiring high order transfer functions to obtain sharp roll-offs.

Applications Information (Continued)

The Tschebycheff function is a min/max approximation in the passband. This approximation has the property that it is equiripple which means that the error oscillates between maximums and minimums of equal amplitude in the passband. The Tschebycheff approximation, because of its equiripple nature, has a much steeper transition region than the Butterworth approximation.

The elliptic filter, also known as Cauer or Zolotarev filters, are equiripple in the passband and stopband and have a steeper transition region than the Butterworth or the Tschebycheff.

For a specific lowpass filter three quantities can be used to determine the degree of the transfer function: the maximum passband ripple, the minimum stopband attenuation, and the transition ratio (tr = ω_S/ω_C). Decreasing A_{MAX}, increasing A_{MIN}, or decreasing tr will increase the degree of the transfer function. But for the same requirements the elliptic filter will require the lowest order transfer function. Tables and graphs are available in reference books such as "Reference Data for Radio Engineers," Howard W. Sams & Co., Inc., 5th Edition, 1970 and Erich Christian and Egon Eisenmann, "Filter Design Tables and Graphs," John Wiley and Sons, 1966.

For specific transfer functions and their pole locations such text as Louis Weinberg, "Network Analysis and Synthesis," McGraw Hill Book Company, 1962 and Richard W. Daniels, "Approximation Methods for Electronic Filter Design," McGraw-Hill Book Company, 1974, are available.

DESIGN OF CASCADED MULTISECTION FILTERS

The first step in designing is to define the response required and define the performance specifications:

1. Type of filter:
   Lowpass, highpass, bandpass, notch, allpass
2. Attenuation and frequency response
3. Performance
   Center frequency/corner frequency plus tolerance and stability

   Insertion loss/gain plus tolerance and stability

   Source impedance

   Load impedance

   Maximum output noise

   Power consumption

   Power supply voltage

   Dynamic range

   Maximum output level

Second step is to find the pole and zero location for the transfer function which meet the above requirements. This can be done by using tables and graphs or network synthesis. The form of the transfer function which is easiest to convert to a cascaded filter is a product of first and second order terms in these forms:

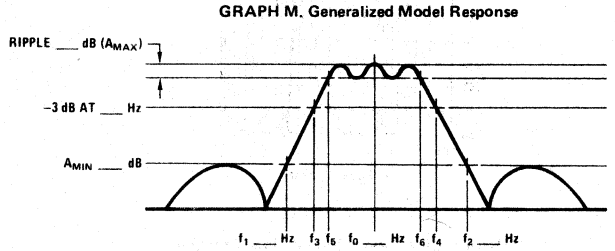
First Order	Second Order	
$\frac{K}{s+\omega_R}$	$\frac{K}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}$	(low pass)
$\frac{Ks}{s+\omega_R}$	$\frac{Ks^2}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}$	(highpass)
	$\frac{Ks}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}$	(bandpass)
	$\frac{K(s^2+\omega_Z^2)}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}$	(notch)
	$\frac{s^2-\frac{\omega_0}{Q}s+\omega_0^2}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}$	(allpass)

Each of the second order functions is realizable by tuning an AF100 stage. By cascading these stages the desired transfer function is realized.

CASCADING SECOND ORDER STAGES

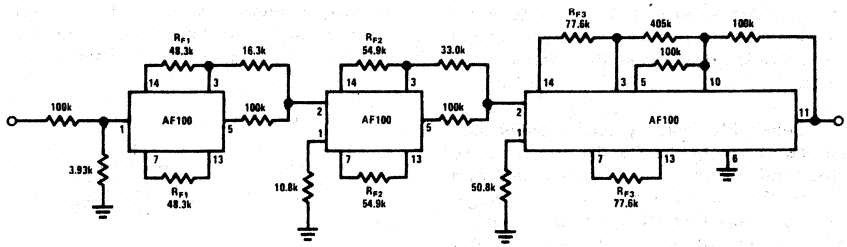
The primary concern in cascading second order stages is to minimize the maximum difference in amplitude from input to output over the frequencies of interest. A computer program is probably required in very complicated cases but some general rules that can be used that will usually give satisfactory results are:

GRAPH M. Generalized Model Response



Applications Information (Continued)

1. The highest "Q" pole pair should be paired with the zero pair closest in frequency.
2. If highpass and lowpass stages are cascaded the lowpass sections should be the higher frequency and highpass sections the lower frequency.
3. In cascaded filters of more than two sections the first section should be the section with "Q" closest to 0.707 and then additional stages should be added in order of least difference between first stage Q and their Q.



Lowpass Elliptic Filter

$F_C = 1$

$F_S = 1.3$

$A_{MAX} = 0.1$ dB

$A_{MIN} = 40$ dB

$N = 6$

$f_{O1} = 1.0415 \quad Q_1 = 7.88 \quad f_{Z1} = 1.329 \quad f_Z/f_O = 1.28 \quad \left(\frac{f_Z}{f_O}\right)^2 = 1.63$

$f_{O2} = 0.9165 \quad Q_2 = 1.79 \quad f_{Z2} = 1.664 \quad f_Z/f_O = 1.82 \quad \left(\frac{f_Z}{f_O}\right)^2 = 3.30$

$f_{O3} = 0.649 \quad Q_3 = 0.625 \quad f_{Z3} = 4.1285 \quad f_Z/f_O = 6.36 \quad \left(\frac{f_Z}{f_O}\right)^2 = 40.5$

$$R_{F1} = \frac{(503.3)}{f_{O1} \times f_C} \times 10^5 \qquad R_{F2} = \frac{(503.3)}{f_{O2} \times f_C} \times 10^5 \qquad R_{F3} = \frac{(503.3)}{f_{O3} \times f_C}$$

at 1000 Hz = f_C

$R_{F1} = 48.3k \qquad R_{F2} = 54.9k \qquad R_{F3} = 77.6k$

6th Order Elliptic Filter

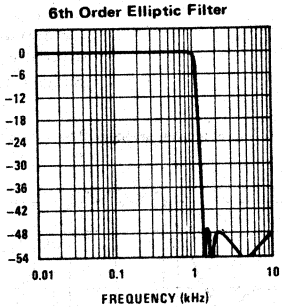


FIGURE 21. Lowpass Elliptic Filter Example

Applications Information (Continued)

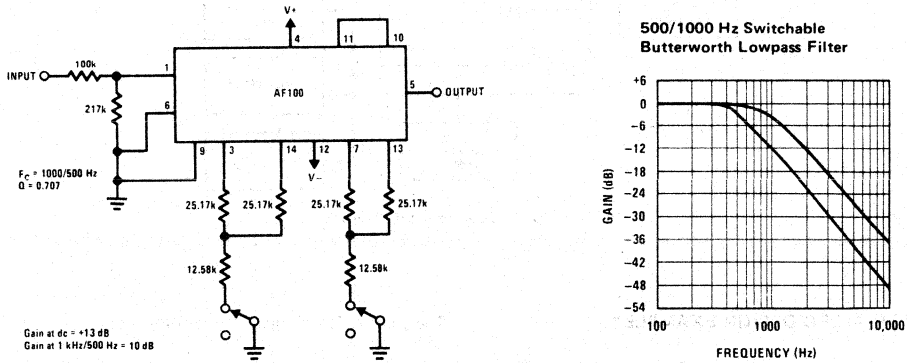


FIGURE 22. Switchable Filter Example: 500 Hz/1000 Hz Butterworth Lowpass

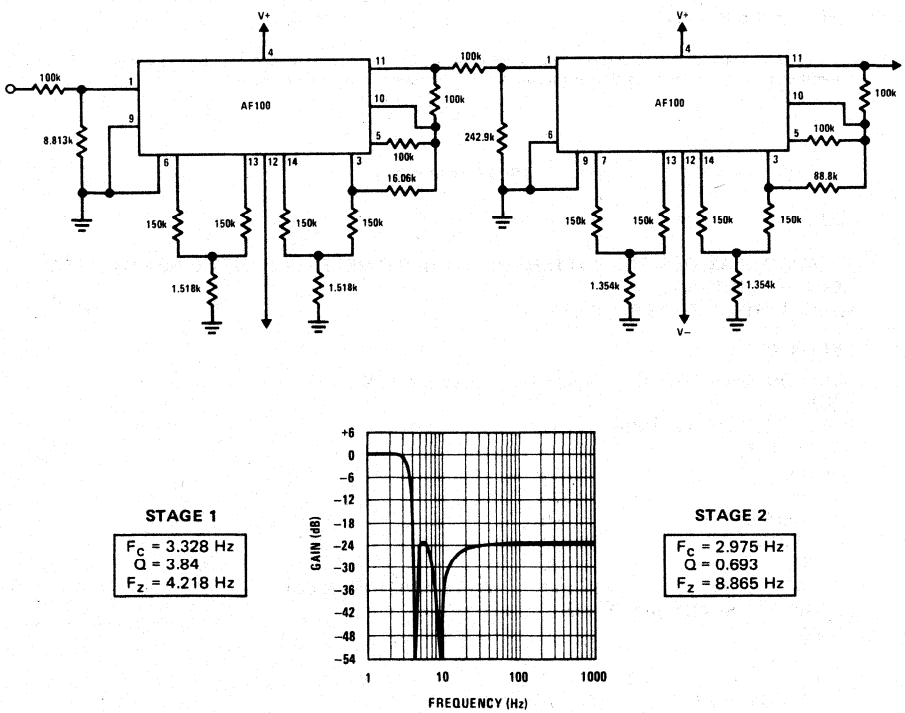


FIGURE 23. EEG Delta Filter—3 Hz Lowpass

Applications Information (Continued)

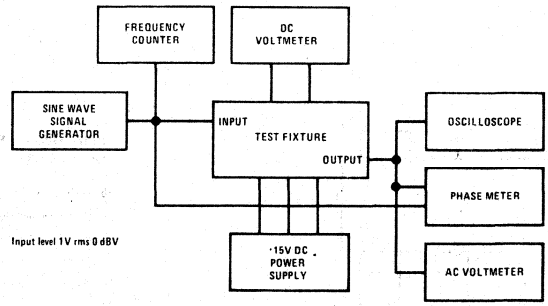


FIGURE 25. Test Circuit Block Diagram

COMPUTER AIDED DESIGN EXAMPLE*

This design is an example of a 60 Hz notch filter. The response is to have the following specifications:

Maximum passband ripple 0.1 dB

Minimum rejection 35 dB

0.1 dB bandwidth 15 Hz max

−35 dB bandwidth 1.5 Hz min

The steps in the design of this filter are:

1. Design a lowpass "prototype" for the filter.
2. Transformation of the lowpass prototype into a notch filter design.
3. Using the pole and zero locations found in step two calculate the value of the resistors required to build the filter.
4. Draw a schematic of filter using values obtained in step three.

*Computer programs shown are user interactive. Underlined copy is user input, non-underlined copy is computer response, and line indications in parenthesis are included for easy identification of data common to several programs.

PROGRAM NO. 1

```
RUN

THIS PROGRAM DESIGNS BUTTERWORTH CHEBYCHEFF OR ELLIPTIC NORMALIZED
LOWPASS FILTERS
WHAT TYPE OF FILTER ? B-C-E

ELLIPTIC
 DO YOU KNOW THE ORDER OF THE FILTER ? Y/N
? NO
INPUT FC,FS,AMAX,AMIN
? 1, 10, .1, 35
     FC                1.000
     FS               10.000
     AMAX               .100
     AMIN             35.000
     N                 2.000
     ATT AT FS       −35.671     (ATTENUATION IN dB)
IS THIS SATISFACTORY ? Y/N
? YES

   F                 Q
    1.823 (Line 1.1)      .775 (Line 1.2)
   Z
   14.124 (Line 1.3)
```

Applications Information (Continued)

PROGRAM NO. 2
(DETERMINES UN-NORMALIZED
POLE + ZERO LOCATIONS OF FIRST SECTION)
(DATA ENTERED FROM PROGRAM NO. 1)

```
RUN
WHAT TYPE FILTER BANDPASS OR NOTCH
? NOTCH
ENTER # OF POLE PAIRS? 1

ENTER # OF JW AXIS ZEROS? 1

  ENTER # OF REAL POLES? 0

  ENTER # OF ZEROS AT ZERO? 0

  ENTER # OF COMPLEX ZEROS? 0

ENTER # OF REAL ZEROS? 0

   ENTER F & Q OF EACH POLE PAIR
? 1.823, .775  (FROM LINE 1.1 AND LINE 1.2)

ENTER VALUES OF JW AXIS ZEROS
? 14.124  (FROM LINE 1.3)

ENTER FREQUENCY SCALING FACTOR
? 1
  ENTER THE # OF FILTERS TO BE DESIGNED
? 1
  ENTER THE C.F. AND BW OF EACH FILTER
? 60, 15
```

OUTPUT OF PROGRAM NO. 2
TRANSFORMED POLE/ZERO LOCATIONS
FIRST SECTION

POLE LOCATIONS

CENTER FREQ.		Q	
56.93601	*(From Line 2.3)*	11.31813	*(From Line 2.4)*
63.228877	*(From Line 2.5)*	11.31813	*(From Line 2.6)*

JW AXIS ZEROS

59.471339 *(From Line 2.1)*
60.533361 *(From Line 22*

PROGRAM NO. 3
(CHECK OF FILTER RESPONSE USING
PROGRAM NO. 2 DATA BASE)

```
RUN

NUMERATOR (ZEROS)
A(I)S^2+R(I)S+Z(I)^2
 1     0     59.471339     (From Line 2.1)
 1     0     60.533361     (From Line 2.2)

REAL POLE

COMPLEX POLE PAIRS

        F          Q
1     56.93601   11.31813   (From Lines 2.3 and 2.4)
2     63.228877  11.31813   (From Lines 2.5 and 2.6)
```

RUN

FREQUENCY	NOR. GAIN (DB)	PHASE	DELAY	NOR. DELAY	FREQUENCY	NOR. GAIN (DB)	PHASE	DELAY	NOR. DELAY
40.000	.032	347.69	.002275	5.847169	60.600	−47.102	169.17	.050801	108.232021
45.000	.060	342.20	.004107	8.749738	60.800	−33.650	165.48	.051677	110.096278
50.000	.100	330.70	.009983	21.268142	61.000	−27.577	161.72	.052809	112.508334
55.000	−.795	290.54	.046620	99.324027	61.200	−23.418	157.87	.054167	115.403169
56.000	−2.298	270.61	.063945	136.234562	61.400	−20.198	153.92	.055712	118.694436
57.000	−5.813	245.51	.072894	155.299278	61.600	−17.554	149.85	.057391	122.270086
58.000	−12.748	220.19	.065758	140.096912	61.800	−15.308	145.65	.059136	125.989157
58.200	−14.740	215.54	.063369	135.006390	62.000	−13.362	141.33	.060869	129.681062
58.400	−17.032	211.06	.060979	129.914831	63.000	−6.557	118.23	.065975	140.559984
58.600	−19.722	206.76	.058692	125.043324	64.000	−2.936	95.30	.059402	126.556312
58.800	−22.983	202.61	.056588	120.561087	65.000	−1.215	76.38	.045424	96.774832
59.000	−27.172	198.60	.054724	116.589928	66.000	−.463	62.43	.032614	69.484716
59.200	−33.235	194.72	.053139	113.212012	67.000	−.138	52.44	.023498	50.062947
59.400	−46.300	190.94	.051856	110.478482	70.000	.091	35.43	.010452	22.267368
59.600	−42.909	7.24	.050888	108.417405	75.000	.085	23.44	.004250	9.054574
59.800	−36.897	3.60	.050242	107.040235	80.000	.060	17.80	.002310	4.921727
60.00	−35.567	360.00	.049916	106.346516	85.000	.043	14.50	.001460	3.110493
60.200	−36.887	356.41	.049907	106.326777	90.000	.032	12.31	.001011	2.154297
60.400	−42.757	352.81	.050206	106.963750					

Applications Information (Continued)

PROGRAM NO. 4

DESIGN OF FIRST SECTION

```
)RUN
WHICH FILTER AF100 -J OR G ?
? J
WHAT TYPE OF FILTER SECTION? HIGHPASS-BANDPASS-LOWPASS-NOTCH-ALLPASS
? NOTCH
INPUT FC AND Q VALUES
? 56.93601, 11.31813  (FROM LINES 2.3 AND 2.4)
INPUT REAL POLE AND CAPACITOR VALUES IF NONE ENTER 0
? 0
INPUT ZERO LOCATION
? 59.471339      (FROM LINE 2.1)
ARE TUNING INSTRUCTIONS REQUIRED ?
? YES
```

TUNING INSTRUCTION

PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 180 DEG. AT 56.93601 HZ.
IF TUNING IS REQUIRED, RF2 FROM PINS 7 TO 13 SHOULD BE ADJUSTED.
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 135 DEG. AT 59.506798HZ.
OR 225 DEG. AT 54.476284 HZ.
IF TUNING IS REQUIRED RQ FROM 1 OR 2 TO GROUND SHOULD BE ADJUSTED
GAIN AT PIN 11 AT 59.471339 SHOULD BE 0 IF NOT
ADJUST RHP FROM PIN 3 TO 10 FOR NULL

FC= 56.93601 Q= 11.31813 F(L-3DB) = 54.476284 F(H-3DB) = 59.506798

GAIN AT F)) FC= .00DB

FUNCTION	CONNECTION FROM	TO	VALUE OF EXTERNAL RESISTORS IN OHMS
R IN	INPUT	1	100000.000
RQ	1	GND	2675.931
RF1	3	14	883960.996
RF2	7	13	883960.996
RLP	5	10	100000.000
RHP	3	10	10910.418
RG	10	11	357910.697
+V		4	
-V		12	
GND		9	
GND		6	
OUTPUT	PIN 11		

PROGRAM NO. 4

DESIGN OF SECOND SECTION

WHAT TYPE OF FILTER SECTION? HIGHPASS-BANDPASS-LOWPASS-NOTCH-ALLPASS
? NOTCH
INPUT FC AND Q VALUES
? 63.228877, 11.31813 *(FROM LINES 2.5 AND 2.6)*
INPUT REAL POLE AND CAPACITOR VALUES IF NONE ENTER 0
? 0
INPUT ZERO LOCATION
? 60.533361 *(FROM LINE 2.2)*
ARE TUNING INSTRUCTIONS REQUIRED ?
? YES

TUNING INSTRUCTION

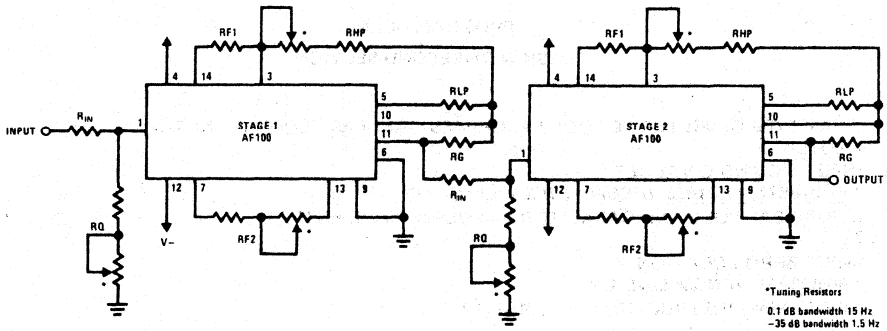
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 180 DEG. AT 63.228877 HZ.
IF TUNING IS REQUIRED RF2 FROM PINS 7 TO 13 SHOULD BE ADJUSTED
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 135 DEG. AT 66.083802 HZ.
OR 225 DEG. AT 60.497289 HZ.
IF TUNING IS REQUIRED RQ FROM 1 OR 2 TO GROUND SHOULD BE ADJUSTED
GAIN AT PIN 11 AT 60.533361 SHOULD BE 0 IF NOT
ADJUST RHP FROM PIN 3 TO 10 FOR NULL

FC= 63.228877 Q= 11.31813 F(L-3DB)= 60.497289 F(H-3DB)= 66.083802

GAIN AT F((FC= .00DB

FUNCTION	CONNECTION FROM	CONNECTION TO	VALUE OF EXTERNAL RESISTORS IN OHMS
R IN	INPUT	1	100000.000
RQ	1	GND	2675.931
RF1	3	14	795984.596
RF2	7	13	795984.596
RLP	5	10	100000.000
RHP	3	10	9165.552
RG	10	11	328044.920
+V		4	
−V		12	
GND		9	
GND		6	
OUTPUT	PIN 11		

Applications Information (Continued)



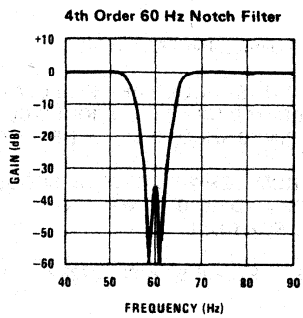


FIGURE 26. Implementation of a 60 Hz Notch From Computer Calculations

DEFINITION OF TERMS

A_{MAX}	Maximum passband peak-to-peak ripple
A_{MIN}	Minimum stopband loss
f_Z	Frequency of jw axis pair
f_O	Frequency of complex pole pair
Q	Quality of pole
f_C	Passband edge
f_S	Stopband edge
A_{HP}	Gain from input to highpass output
A_{BP}	Gain from input to bandpass output
A_{LP}	Gain from input to lowpass output
A_{AMP}	Gain from input to output of amplifier
R_f	Pole frequency determining resistance
R_Z	Zero Frequency determining resistance
R_Q	Pole Quality determining resistance
f_H	Frequency above center frequency at which the gain decreases by 3 dB for a bandpass filter
f_L	Frequency below center frequency at which the gain decreases by 3 dB for a bandpass filter
BW	The bandwidth of a bandpass filter
N	Order of the denominator of a transfer function

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AF150 Universal Wideband Active Filter

General Description

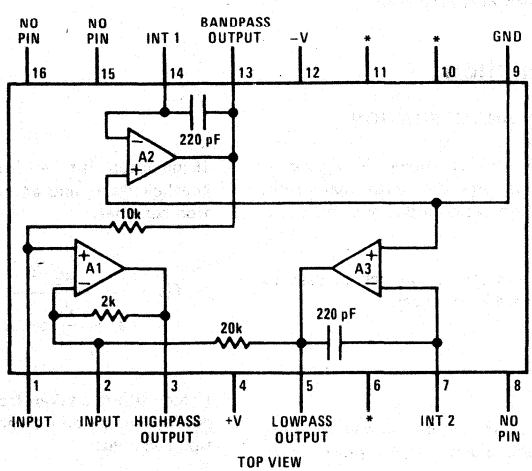
The AF150 wide band active filter is a general second order lumped RC network. Only four external resistors are required to program the AF150 for specific second order functions. Low pass, high pass and band pass functions are available simultaneously at separate outputs. Notch and all pass functions can be formed by summing the outputs with an external amplifier. Higher order filters are realized by cascading AF150 active filters with appropriate programming resistors.

Any of the classical filter configurations, such as Butterworth, Bessel, Cauer and Chebyshev can be formed.

Features

- Independent Q, frequency, gain adjustments
- Low sensitivity to external component variation
- Separate low pass, high pass, band pass outputs
- Inputs may be differential, inverting or non-inverting
- All pass and notch outputs may be formed
- Operates to 100 kHz
- Q range to 500
- Power supply range ±5V to ±18V
- High accuracy ±1% unadjusted
- Q frequency product 2×10^5

Connection Diagrams



TOP VIEW

Ceramic Dual-In-Line Package HY13A
AF150-1CJ
AF150-2CJ

***Note:** Internally connected. DO NOT USE.

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	900 mW/Package (500 mW/Amp)
Differential Input Voltage	±36V
Output Short-Circuit Duration (Note 1)	Infinite
Operating Temperature	−25°C to +85°C
Storage Temperature	−25°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Specifications apply for V_S = ±15V, over −25°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Frequency Range	$f_c \times Q \leq 2 \times 10^5$			100k	Hz
	Q Range	$f_c \times Q \leq 2 \times 10^5$			500	Hz/Hz
	f_o Accuracy					
	AF150-1J	$f_c \times Q \leq 5 \times 10^4$, T_A = 25°C			±2.5	%
	AF150-2J	$f_c \times Q \leq 5 \times 10^4$, T_A = 25°C			±1.0	%
$\Delta f_o/\Delta T$	f_o Temperature Coefficient			±50	±150	ppm/°C
	Q Accuracy	$f_c \times Q \leq 5 \times 10^4$, T_A = 25°C			±7.5	%
$\Delta Q/\Delta T$	Q Temperature Coefficient			±300	±750	ppm/°C
PSRR	Power Supply Rejection Ratio		80	100		dB
CMRR	Common-Mode Rejection		80	100		dB
I_{os}	Input Offset Current	T_j = 25°C		3	50	pA
I_B	Input Bias Current	T_j = 25°C		30	200	pA
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	±12		V
I_s	Power Supply Current	V_S = ±15V, T_A = 25°C		15	30	mA

Note 1: Any of the amplifier's outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum package power dissipation will be exceeded.

Applications Information

CIRCUIT DESCRIPTION AND OPERATION

A schematic of the AF150 is shown in *Figure 1*. Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input.

By adding external resistors the circuit can be used to generate the second order transfer function:

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_o = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_o}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(high pass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer function becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(band pass)}$$

Applications Information (Continued)

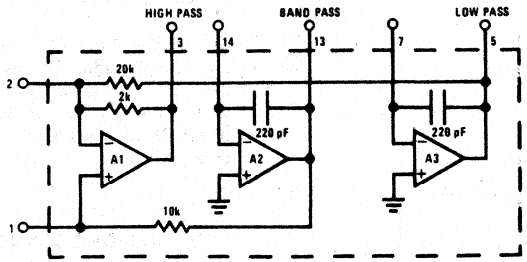


FIGURE 1. AF150 Schematic

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(low pass)}$$

Using an external op amp and the proper input and output connections, the circuit can also be used to generate the transfer functions for a notch and all pass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals ω_z^2 and a_3 equals 1. The transfer function becomes:

$$T(s) = \frac{s^2 + \omega_z^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(notch)}$$

In the all pass transfer function $a_3 = 1$, $a_2 = -\omega_o/Q$ and $a_1 = \omega_o^2$. The transfer function becomes:

$$T(s) = \frac{s^2 - \frac{\omega_o}{Q} s + \omega_o^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(all pass)}$$

The relationships between the generalized coefficients and the external resistors will be found in the appendix. It is not, however, necessary to use these theoretical, if not "messy", equations to solve for the proper external resistor values. In general, it is assumed that the user has knowledge of the frequency and Q of the specific filter he is designing. For higher order filters of various types, the reader is directed to any of the available texts on filters (see bibliography) for information and tables concerning the location of the poles and zeros. Once the specifics of the filter are found from the tables, it is simply a matter of cascading the sections with proper attention to some general guidelines which are included later in the application section.

The following discussion gives a step-by-step procedure for designing filters with several examples given for clarity.

FREQUENCY TUNING

Two equal value frequency setting resistors are required for frequencies above 1 kHz. For lower frequencies, T tuning or the addition of external capacitors is required. Using external capacitors allows the user to go as low in frequency as he desires. T tuning and external capacitors can be used together.

Two resistor tuning for 1 kHz to 100 kHz

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega \qquad (1)$$

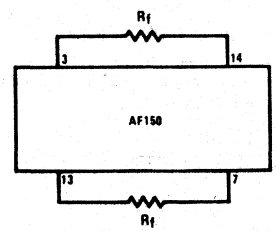
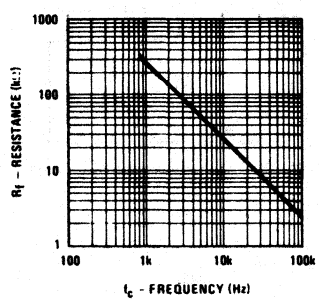


FIGURE 2. Resistive Tuning

GRAPH A. Resistive Tuning



Applications Information (Continued)

T resistive tuning for $f_o < 1$ kHz

$$R_S = \frac{R_T^2}{R_f - 2R_T} \qquad (2)$$

R_f from equation 1.

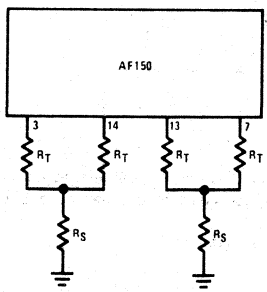
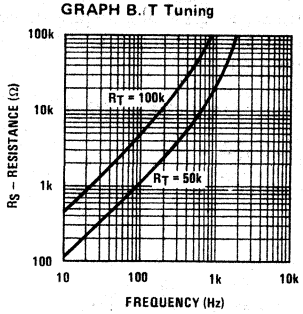


FIGURE 3. T Tuning

GRAPH B. T Tuning



If external capacitors are used for $f_o < 1$ kHz, then equation 3 should be used.

$$R_f = \frac{0.05033}{f_o\,(C + 220 \times 10^{-12})}\ \Omega \qquad (3)$$

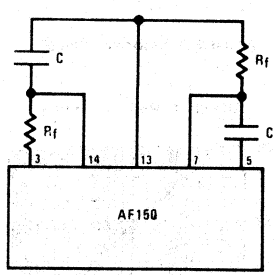


FIGURE 4. Low Frequency RC Tuning

Q DETERMINATION

Setting the Q requires one resistor from either pin 1 or pin 2 to ground. The value of the Q setting resistor depends on the input connection and input resistance as well as the value of the Q. The Q will be inversely proportional to the resistance from pin 1 to ground and directly proportional to resistance from pin 2 to ground.

NON-INVERTING CONNECTION*

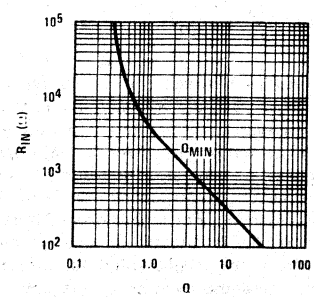
To determine the Q resistor, choose a value of input resistor, R_{IN}, *(Figures 5 and 6)* and calculate Q_{MIN} (graph C).

$$Q_{MIN} = \frac{1 + \frac{10^4}{R_{IN}}}{3.48}$$

If the Q required in the circuit is greater than Q_{MIN}, use the circuit configuration shown in *Figure 5* and equation 4 to calculate R_Q, the Q resistor. If the Q of the circuit is less than Q_{MIN}, use the circuit configuration shown in *Figure 6* and equation 5.

*The discussion of "non-inverting" and "inverting" has to do with the phase relationship between the input port and the *low pass* output port. Refer to *Figure 1* for other output port phase relationships.

GRAPH C. Q_{MIN}, Non-Inverting Input



Applications Information (Continued)

For $Q > Q_{MIN}$ in non-inverting mode:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}} \ \Omega \qquad (4)$$

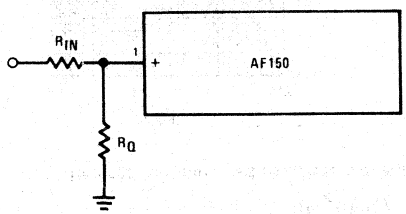
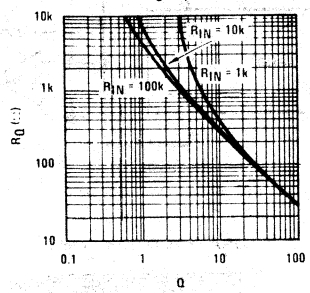


FIGURE 5. Q Tuning for $Q > Q_{MIN}$, Non-Inverting Input

GRAPH D. R_Q for $Q > Q_{MIN}$, Non-Inverting Input



For $Q < Q_{MIN}$ in non-inverting mode:

$$R_Q = \frac{2 \times 10^3}{\left(1 + \frac{10^4}{R_{IN}}\right)} \ \Omega \qquad (5)$$
$$0.3162 \frac{}{Q} - 1.1$$

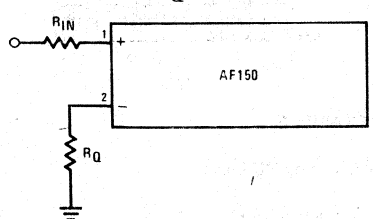
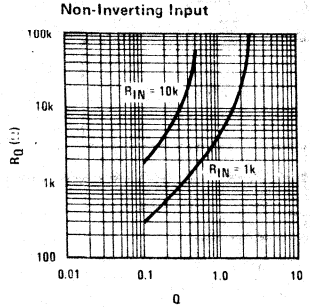


FIGURE 6. Q Tuning for $Q < Q_{MIN}$, Non-Inverting Input

GRAPH E. R_Q for $Q < Q_{MIN}$, Non-Inverting Input



INVERTING CONNECTION*

For any Q in inverting mode:

$$R_Q = \frac{10^4}{3.16Q\left(1.1 + \frac{2 \times 10^3}{R_{IN}}\right) - 1} \ \Omega \qquad (6)$$

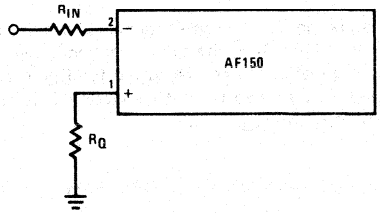
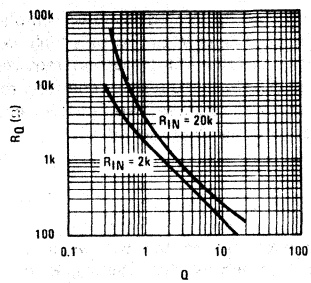


FIGURE 7. Q Tuning, Inverting Input

GRAPH F. Q Tuning, Inverting Input

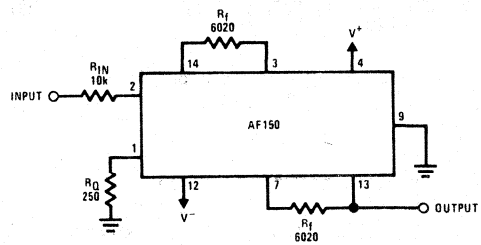


*The discussion of "non-inverting" and "inverting" has to do with the phase relationship between the input port and the *low pass* output port. Refer to *Figure 1* for other output port phase relationships.

DESIGN EXAMPLE

Non-Inverting Band Pass Filter

Center frequency 38 kHz = f_o, 10 Hz/Hz = Q, 10k = R_{IN}.



Using equation 1

$$R_f = \frac{228.8 \times 10^6}{f_o} \ \Omega$$

$$R_f = \frac{228.8 \times 10^6}{38 \times 10^3} = 6020\Omega$$

Applications Information (Continued)

Using equation 6

$$R_Q = \frac{10^4}{3.16Q\left(1.1 + \frac{2 \times 10^3}{R_{IN}}\right) - 1} \ \Omega$$

$$R_Q = 250\Omega$$

From equation 33, the center frequency gain is found to be 6.3 V/V (16 dB). If the center frequency gain is to be adjusted, equation 33 can be solved for R_Q in terms of R_{IN} and this substituted into equation 6 to find the required R_{IN} and R_Q.

NOTCH FILTERS

Notches can be generated by two simple methods: using RC input *(Figure 8)* or low pass/high pass summing *(Figure 9)*. The RC input method requires adding a capacitor to pin 14 and a resistor connects to pin 7. The summing method requires two resistors connected to the low pass and high pass output.

The difference between the two possible methods of generating a notch is that the capacitor connection requires a high quality precision capacitor and the gain of the circuit is difficult to adjust because the gain and zero location are both dependent on C_Z and R_Z. The amplifier summing method requires 3 precision resistors and an external operational amplifier. However, the gain can be adjusted independent of the notch frequency.

For input RC notch tuning:

$$R_Z = \frac{C_Z R_f \times 10^{12}}{220}\left(\frac{f_o}{f_z}\right)^2 \ \Omega \qquad (7)$$

f_Z = frequency of notch (zero location)

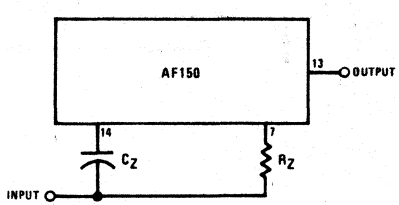
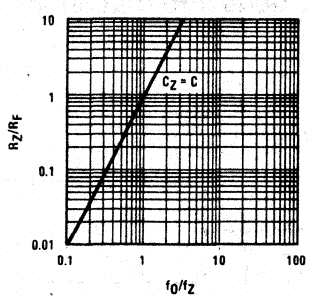


FIGURE 8. Input RC Notch

GRAPH G. Input RC Notch



For the low pass/high pass summing technique,

$$R_h = \left(\frac{f_z}{f_o}\right)^2 \frac{R_L}{10} \qquad (8)$$

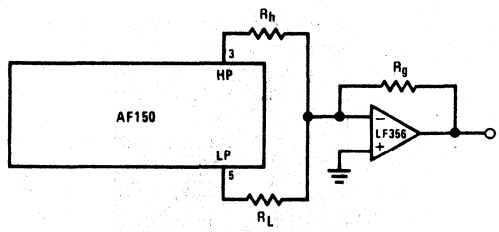
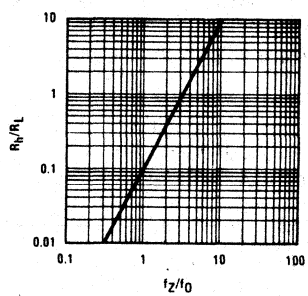


FIGURE 9. Output Notch

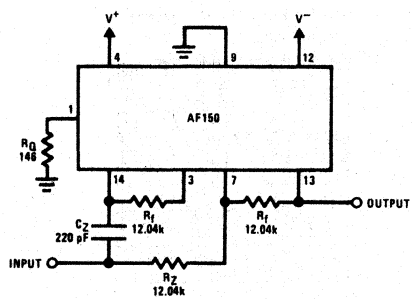
GRAPH H. Output Notch



DESIGN EXAMPLE

19 kHz notch using RC input.

Center frequency	19 kHz	f_o
Zero frequency	19 kHz	f_Z
	20	Q



Applications Information (Continued)

Using equation 1:

$$R_f = \frac{228.8 \times 10^6}{f_o} \ \Omega$$

$$R_f = 12{,}040\Omega$$

Using equation 4 with $R_{IN} = \infty$:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}} \ \Omega$$

$$R_Q = 146\Omega$$

Using equation 7:

$$R_Z = \left(\frac{C_Z R_F \times 10^{12}}{220}\right)\left(\frac{f_o}{f_z}\right)^2 \ \Omega$$

$$R_Z = 12{,}040\Omega$$

DESIGN EXAMPLE

19 kHz notch using low pass/high pass summing

Center frequency	19 kHz	f_o
Zero frequency	19 kHz	f_Z
	20	Q

Using equation 1:

$$R_f = \frac{228.8 \times 10^6}{f_o} \ \Omega$$

$$R_f = 12{,}040\Omega$$

Using equation 4, choose $R_{IN} = 10\ k\Omega$:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}} \Omega$$

$$R_Q = 148\Omega$$

Using equation 8:

$$R_h = \left(\frac{f_Z}{f_o}\right)^2 \frac{R_L}{10}$$

Choose $R_L = 20k$, then $R_h = 2k$

TRIALS, TRIBULATIONS AND TRICKS

Certainly, there is no substitute for experience when applying active filters, working with op amps or riding a bicycle. However, the following section will discuss some of the finer points in more detail, and hopefully alleviate some of the fears and problems that might be encountered.

TUNING TIPS

In applications where 2 to 3% accuracy is not sufficient to provide the required filter response, the AF150 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the band pass (pin 13) output.

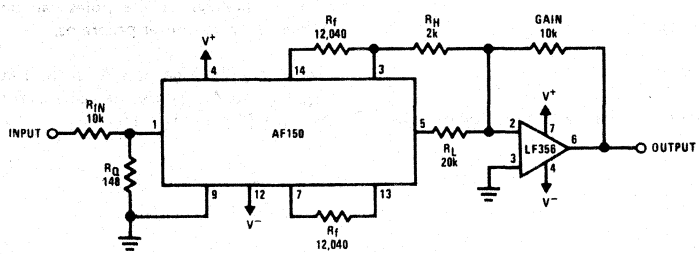
Before any tuning is attempted the low pass (pin 5) output should be checked to see that the output is not clipping. At the center frequency of the section the low pass output is 10 dB higher than the band pass output and 20 dB higher than the high pass. This should be kept in mind because if clipping occurs the results obtained when tuning will be incorrect.

Frequency Tuning

By adjusting the resistance between pins 7 and 13 the center frequency of a section can be adjusted. If the input is through pin 1 the phase shift at center frequency will be 180° and if the input is through pin 2 the phase shift at center frequency will be 0°. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

Q Tuning

The Q is tuned by adjusting the resistance between pin 1 or pin 2 and ground. Low Q tuning resistors will be from pin 2 to ground (Q < 0.6). High Q tuning resistors will be from pin 1 to ground. To tune the Q correctly, the signal source must have an output impedance very much lower than the input resistance of the filter since



Applications Information (Continued)

the input resistance affects the Q. The input must be driven through the same resistance the circuit will see to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right) \times (f_o)$$

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q} \right) \times (f_o)$$

where f_o = center frequency

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair the notch can be tuned by adjusting the ratio of the summing resistors (low pass/high pass summing) or the input resistance (input RC).

In either case the signal is connected to the input and the proper resistor is adjusted for a null at the output.

Special Cases

When using the input RC notch the unit cannot be tuned through the normal input so an additional 100k resistor can be added at pin 1 and the unit can be tuned normally. Then the 100k input resistor should be grounded and the notch tuned through the normal RC input.

An alternative way of tuning is to tune using the Q resistor as the input. This requires the Q resistor be lifted from ground and connecting the signal source to the normally grounded end of the Q resistor. This has the problem that when the Q resistor is grounded after tuning, its value is decreased by the output impedance of the source. This technique has the advantage of not requiring an additional resistor.

TUNING PROCEDURE

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the low pass output pin 5.

Adjust the resistance between pins 13 and 7 until the phase shift between input and band pass output is 180°.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

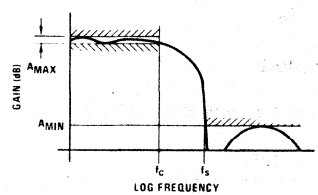
Zero Tuning

Set the oscillator output to the zero frequency and tune the zero resistor for a null at the output of the summing amplifier.

FILTER DESIGN

Since most filter tables are in terms of a normalized low pass prototype, the filter to be designed is usually reduced to a low pass prototype. After the low pass transfer function is found, it is transformed to obtain the transfer function for the actual filter desired. The low pass amplitude response which can be defined by four quantities, defined below:

Low Pass Response



A_{MAX} = the maximum peak-to-peak ripple in the pass band

A_{MIN} = the minimum attenuation in the stop band

f_c = the pass band cutoff frequency

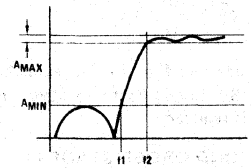
f_s = the stop band start frequency

By defining these four quantities for the low pass prototype the normalized pole and zero locations and the Q (quality) of the poles can be determined from tables or by computer programs.

To obtain the high pass from the low pass filter tables, A_{MAX} and A_{MIN} are the same as for the low pass case, but $f_c = 1/f_2$ and $f_s = 1/f_1$.

Applications Information (Continued)

High Pass Response



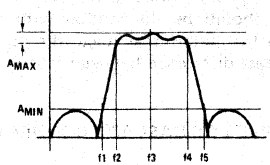
To obtain the band pass from the low pass filter tables, A_{MAX} and A_{MIN} are the same as for the low pass case, but:

$$f_c = 1 \qquad f_s = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 \cdot f_5} = \sqrt{f_2 \cdot f_4}$ i.e., geometric symmetry

$f_5 - f_1 = A_{MIN}$ bandwidth
$f_4 - f_2$ = Ripple bandwidth

Band Pass Response

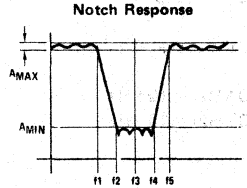


To obtain the notch from the low pass filter tables, A_{MAX} and A_{MIN} are the same as for the low pass case and

$$f_c = 1, \quad f_s = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 \cdot f_5} = \sqrt{f_2 \cdot f_4}$

Notch Response



Normalized Low Pass Transformed to Un-Normalized Low Pass

The normalized low pass filter has the pass band edge normalized to unity. The un-normalized low pass filter instead has the pass band edge at f_c. The normalized and un-normalized low pass filters are related by the transformation $s = s\omega_c$. This transforms the normalized pass band edge $s = j$ to the un-normalized pass band edge $s = j\omega_c$.

Normalized Low Pass Transformed to Un-Normalized High Pass

The transformation that can be used for low pass to high pass is $S = \omega_c/s$. Since S is inversely proportional to s, the low frequency and high frequency responses are interchanged. The normalized low pass $1/(S^2 + S/Q + 1)$ transforms to the un-normalized high pass:

$$\frac{s^2}{s^2 + \frac{\omega_c}{Q} s + \omega_c^2}$$

Normalized Low Pass Transformed to Un-Normalized Band Pass

The transformation that can be used for low pass to band pass is:

$$S = \frac{s^2 + \omega_o^2}{BW \cdot s}$$

where ω_o^2 is the center frequency of the desired band pass filter and BW is the ripple bandwidth.

Normalized Low Pass Transformed to Un-Normalized Band Stop (Or Notch)

The bandstop filter has a reciprocal response to a band pass filter. Therefore, a bandstop filter can be obtained by first transforming the low pass prototype to a high pass and then performing the band pass transformation.

SELECTION OF TRANSFER FUNCTION

The selection of a function which approximates the shape of the response desired is a complicated process. Except in the simplest cases, it requires the use of tables or computer programs. The form of the transfer function desired is in terms of the pole and zero locations. The most common approximations found in tables are Butterworth, Chebychev, Elliptic and Bessel. The decision as to which approximation to use is usually a function of the requirements and system objectives. Butterworth filters are the simplest but have the disadvantage of requiring high order transfer functions to obtain sharp roll-offs.

The Chebychev function is a min/max approximation in the pass band. This approximation has the property that it is equiripple which means that the error oscillates between maximums and minimums of equal amplitude in the pass band. The Chebychev approximation, because of its equiripple nature, has a much steeper transition region than the Butterworth approximation.

The elliptic filter, also known as Cauer or Zolotarev filters, are equiripple in the pass band and stop band and have a steeper transition region than the Butterworth or the Chebychev.

For a specific low pass filter three quantities can be used to determine the degree of the transfer function: the maximum pass band ripple, the minimum stop band attenuation, and the transition ratio ($tr = \omega_s/\omega_c$). Decreasing A_{MAX}, increasing A_{MIN}, or decreasing tr will increase the degree of the transfer function. But for

Applications Information (Continued)

the same requirements the elliptic filter will require the lowest order transfer function. Tables and graphs are available in reference books such as "Reference Data for Radio Engineers", Howard W. Sams & Co., Inc., 5th Edition, 1970 and Erich Christian and Egon Eisenmann, "Filter Design Tables and Graphs", John Wiley and Sons, 1966.

For specific transfer functions and their pole locations such text as Louis Weinberg, "Network Analysis and Synthesis", McGraw Hill Book Company, 1962 and Richard W. Daniels, "Approximation Methods for Electronic Filter Design", McGraw-Hill Book Company, 1974, are available.

DESIGN OF CASCADED MULTISECTION FILTERS

The first step in designing is to define the response required and define the performance specifications:

1. Type of filter:
   Low pass, high pass, band pass, notch, all pass
2. Attenuation and frequency response
3. Performance
   Center frequency/corner frequency plus tolerance and stability
   Insertion loss/gain plus tolerance and stability
   Source impedance
   Load impedance
   Maximum output noise
   Power consumption
   Power supply voltage
   Dynamic range
   Maximum output level

Second step is to find the pole and zero location for the transfer function which meet the above requirements. This can be done by using tables and graphs or network synthesis. The form of the transfer function which is easiest to convert to a cascaded filter is a product of first and second order terms in these forms:

First Order	Second Order	
$\frac{K}{s+\omega_r}$	$\frac{K}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(low pass)
$\frac{Ks}{s+\omega_r}$	$\frac{Ks^2}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(high pass)
	$\frac{Ks}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(band pass)
	$\frac{K(s^2+\omega_z^2)}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(notch)
	$\frac{s^2-\frac{\omega_o}{Q}s+\omega_o^2}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(all pass)

Each of the second order functions is realizable by using an AF150 stage. By cascading these stages the desired transfer function is realized.

CASCADING SECOND ORDER STAGES

The primary concern in cascading second order stages is to minimize the difference in amplitude from input to output over the frequencies of interest. A computer program is probably required in very complicated cases but some general rules that can be used that will usually give satisfactory results are:

1. The highest Q pole pair should be paired with the zero pair closest in frequency.
2. If high pass and low pass stages are cascaded, the low pass sections should be the higher frequency and high pass sections the lower frequency.
3. In cascaded filters of more than two sections, the first section should be the section with Q closest to 0.707 and then additional stages should be added in order of least difference between first stage Q and their Q.

DESIGN EXAMPLES OF CASCADE CONNECTIONS

Example 1.

Consider a 4th order Butterworth low pass filter with a 10 kHz cutoff (−3 dB) frequency and input impedance $\geq 30\ k\Omega$.

From tables, the normalized filter parameters are:

F1 = 1.0 Q1 = 0.541
F2 = 1.0 Q2 = 1.306

Thus, relative to the design required

F1 = (1.0)(10 kHz) = 10 kHz
F2 = (1.0)(10 kHz) = 10 kHz

Section 1

F = 10 kHz, Q = 1.306

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega \qquad \text{(Using equation 1)}$$

$R_f = 22{,}880\Omega$

Select input resistor 31.6 kΩ

$$Q_{MIN} = \frac{1+\frac{10^4}{R_{IN}}}{3.48}$$

$Q_{MIN} = 0.378$

Applications Information (Continued)

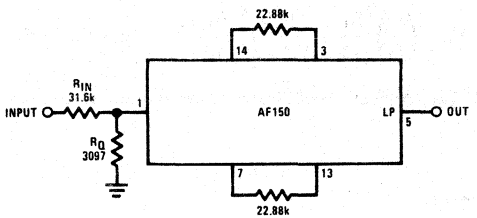
Thus, $Q > Q_{MIN}$

Therefore:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega \qquad \text{(Using equation 4)}$$

$R_Q = 3097\Omega$

First Stage



Section 2

$f_o = 10k$, $Q = 0.541$

Since f_o is the same as for the first section:

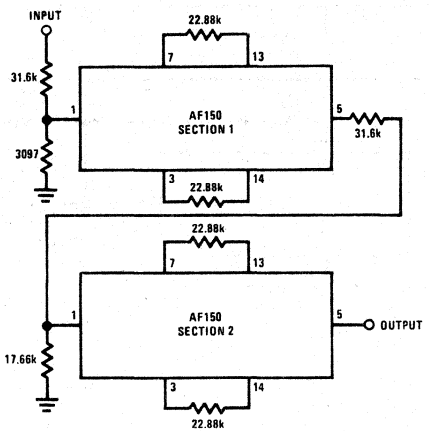
$R_f = 22.88\ k\Omega$

Select $R_{IN} = 31.6\ k\Omega$

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega \qquad \text{(Using equation 4)}$$

$R_Q = 17{,}661\Omega$

Complete Filter, Example 1



Example 2.

Consider the design of a low pass filter with the following performance:

$f_c = 10$ kHz
$f_s = 11$ kHz
$A_{MAX} = 1$ dB
$A_{MIN} = 40$ dB

It is found that a 6th order elliptic filter will satisfy the above requirements. The parameters of the design are:

STAGE	f_o (kHz)	Q	f_z (kHz)
1	5.16	0.82	29.71
2	8.83	3.72	13.09
3	10.0	20.89	11.15

Stage 1

a) From equation 1, R_F is found to be 44.34k
b) From equation 4, R_Q is found to be 11.72k, assuming R_{IN} (arbitrary) is 10 kΩ.

To create the transmission zero, f_z, at 29.71 kHz, use equation 8.

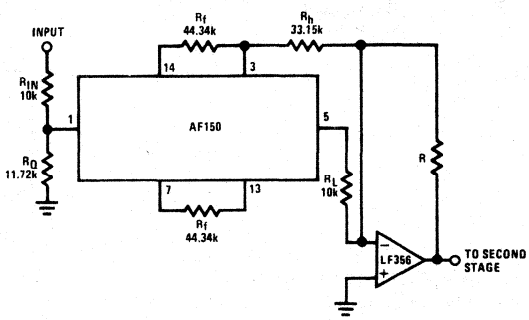
$$R_h = \left(\frac{f_z}{f_o}\right)^2 \frac{R_L}{10}, \text{ or } R_h = \left(\frac{29.71}{5.16}\right)^2 \frac{R_L}{10}$$

Thus,

$R_h = 3.315\ R_L$

If R_L is arbitrarily chosen as 10 kΩ, R_h = 33.15k.

Thus, the design of the first stage is:



where the feedback resistor, R, around the external op amp may be used to adjust the gain.

Applications Information (Continued)

Stage 2

The second stage design follows exactly the same procedure as the first stage design. The results are:

a) From equation 1, $R_f = 25.91k$

b) From equation 4, $R_Q = 913.6\Omega$, again assuming R_{IN} is arbitrarily 10k.

c) $R_h = \left(\frac{13.09}{8.83}\right)^2 \frac{R_L}{10}$ or $R_h = 0.22\ R_L$

Selecting R_L = 10k, then R_h = 2.2k, the second stage design is shown below.

Stage 3

The third stage design, again, is identical to the first 2 stages and the results are (for R_{IN} = 10k):

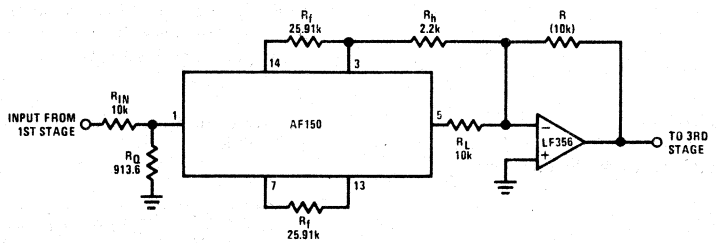
$$R_f = \frac{228.8 \times 10^6}{f_o} = 22.88k$$

$$R_Q = \frac{10^4}{3.48\Omega - 1 - \frac{10^4}{R_{IN}}} = 141.4\Omega$$

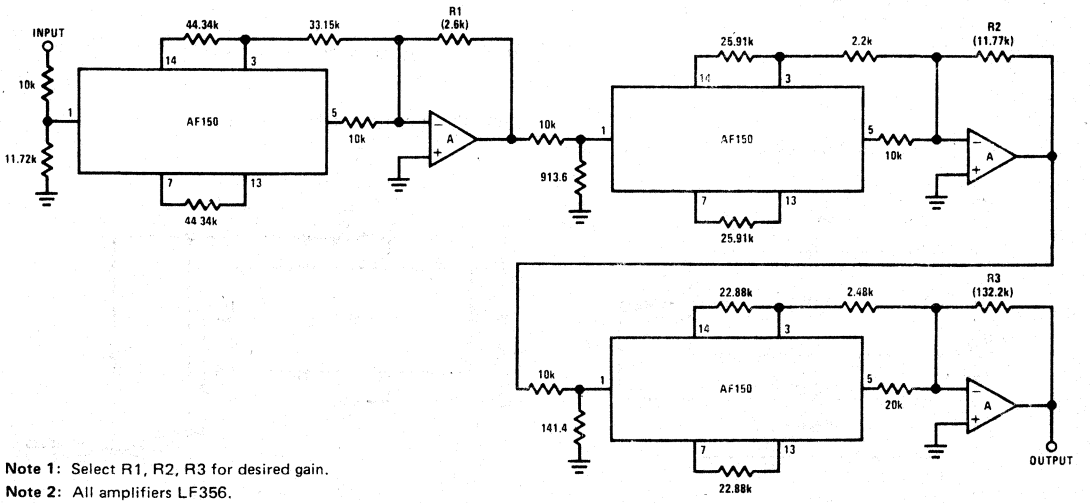
$$R_h = \left(\frac{f_z}{f_o}\right)^2 \frac{R_L}{10} = \left(\frac{11.5}{10}\right)^2 \frac{R_L}{10} \qquad R_h = 0.124\ R_L$$

Let R_L = 20k, R_h = 2.48k

Second Stage



Filter for Example 2



Note 1: Select R1, R2, R3 for desired gain.

Note 2: All amplifiers LF356.

Applications Information (Continued)

From equation 13, the DC gain of the first section is

$$A_{V1} = \frac{11}{1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}}$$

$$A_{V1} = \frac{11}{1 + \frac{10^4}{10^4} + \frac{10^4}{11.72 \times 10^3}} = 3.86 \text{ V/V}$$

Similarly, the DC gain of the second and third sections are:

$A_{V2} = 0.850$
$A_{V3} = 0.151$

Therefore, the overall DC gain is 0.495 and can be adjusted by selecting R1 with respect to 10k, R2 with respect to 10k or R3 with respect to 20k.

For convenience, a standard resistor value table is given below.

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.33 can represent 1.33Ω, 133Ω, 1.33 kΩ, 13.3 kΩ, 133 kΩ, 1.33 MΩ.

Standard 5% and 2% Resistance Values

OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	MEGOHMS	
10	27	68	180	470	1,200	3,300	8,200	22,000	56,000	150,000	0.24	0.62
11	30	75	200	510	1,300	3,600	9,100	24,000	62,000	160,000	0.27	0.68
12	33	82	220	560	1,500	3,900	10,000	27,000	68,000	180,000	0.30	0.75
13	36	91	240	620	1,600	4,300	11,000	30,000	75,000	200,000	0.33	0.82
15	39	100	270	680	1,800	4,700	12,000	33,000	82,000	220,000	0.36	0.91
16	43	110	300	750	2,000	5,100	13,000	36,000	91,000		0.39	1.0
18	47	120	330	820	2,200	5,600	15,000	39,000	100,000		0.43	1.1
20	51	130	360	910	2,400	6,200	16,000	43,000	110,000		0.47	1.2
22	56	150	390	1,000	2,700	6,800	18,000	47,000	120,000		0.51	1.3
24	62	160	430	1,100	3,000	7,500	20,000	51,000	130,000		0.56	1.5

Decade Table Determining 1/2% and 1% Standard Resistance Values

1.00	1.21	1.47	1.78	2.15	2.61	3.16	3.83	4.64	5.62	6.81	8.25
1.02	1.24	1.50	1.82	2.21	2.67	3.24	3.92	4.75	5.76	6.98	8.45
1.05	1.27	1.54	1.87	2.26	2.74	3.32	4.02	4.87	5.90	7.15	8.66
1.07	1.30	1.58	1.91	2.32	2.80	3.40	4.12	4.99	6.04	7.32	8.87
1.10	1.33	1.62	1.96	2.37	2.87	3.48	4.22	5.11	6.19	7.50	9.09
1.13	1.37	1.65	2.00	2.43	2.94	3.57	4.32	5.23	6.34	7.68	9.31
1.15	1.40	1.69	2.05	2.49	3.01	3.65	4.42	5.36	6.49	7.87	9.53
1.18	1.43	1.74	2.10	2.55	3.09	3.74	4.53	5.49	6.65	8.06	9.76

Appendix (See footnote)

The specific transfer functions for some of the most useful circuit configurations using the AF150 are illustrated in *Figures 10 through 16*. Also included are the gain equations for each transfer function in the frequency band of interest, the Q equation, center frequency equation and the Q determining resistor equation. Q_{MIN} is a function of R_{IN} (see graph C).

a) Non-inverting input *(Figure 10)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^4}+\dfrac{R_{IN}}{R_Q}}\right]}{\Delta} \text{ (high pass)} \quad (9)$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1 \left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^4}+\dfrac{R_{IN}}{R_Q}}\right]}{\Delta} \text{ (band pass)} \quad (10)$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2 \left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^4}+\dfrac{R_{IN}}{R_Q}}\right]}{\Delta} \text{ (low pass)} \quad (11)$$

where

$$\Delta = s^2 + s\left[\frac{1.1}{1+\frac{10^4}{R_Q}+\frac{10^4}{R_{IN}}}\right]\omega_1 + 0.1\,\omega_1\omega_2 \quad (12)$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{11}{\left(1+\dfrac{R_{IN}}{10^4}+\dfrac{R_{IN}}{R_Q}\right)} \text{ (DC Gain)} \quad (13)$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to \infty} = \frac{1.1}{\left(1+\dfrac{R_{IN}}{10^4}+\dfrac{R_{IN}}{R_Q}\right)} \text{ (High Freq. Gain)} \quad (14)$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{\left(1+\dfrac{10^4}{R_Q}+\dfrac{10^4}{R_{IN}}\right)}{\left(1+\dfrac{R_{IN}}{10^4}+\dfrac{R_{IN}}{R_Q}\right)} \text{ (Center Freq. Gain)} \quad (15)$$

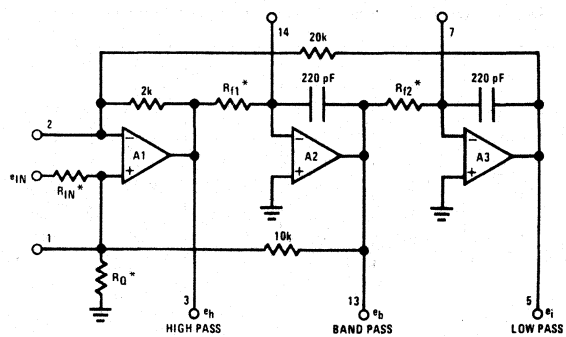
$$\omega_1 = \frac{10^{12}}{R_{f1}\cdot 220} \qquad \omega_2 = \frac{10^{12}}{R_{f2}\cdot 220}$$

where

$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$, (see footnote)

$$Q = \left(\frac{1+\dfrac{10^4}{R_{IN}}+\dfrac{10^4}{R_Q}}{1.1}\right)\sqrt{0.1\left(\frac{\omega_2}{\omega_1}\right)} \quad (16)$$

$$R_Q = \frac{10^4}{\left(\dfrac{1.1Q}{\sqrt{0.1\,\dfrac{\omega_2}{\omega_1}}}\right) - 1 - \dfrac{10^4}{R_{IN}}} \quad (17)$$



*External components

FIGURE 10. Non-Inverting Input ($Q > Q_{MIN}$)

FOOTNOTE:

It should be noted that in the text of this paper, ω_1 and ω_2 have been assumed equal, and hence $R_{f1} = R_{f2}$. No generality is lost in this assumption and it facilitates the design. However, for completeness, the equations given are exact.

Appendix (Continued)

b) Non-inverting input *(Figure 11)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}}\right]}{\Delta} \text{ (high pass)} \quad (18)$$

$$\frac{e_b}{e_{IN}} = \frac{-s\omega_1 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}}\right]}{\Delta} \text{ (band pass)} \quad (19)$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}}\right]}{\Delta} \text{ (low pass)} \quad (20)$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{\frac{10^4}{1 + \frac{R_{IN}}{10^4}}}\right] + 0.1\,\omega_1\omega_2 \quad (21)$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s \to 0} = \frac{1.1 + \frac{2 \times 10^3}{R_Q}}{0.1\left(1 + \frac{R_{IN}}{10^4}\right)} \quad (22)$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = \frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}} \quad (23)$$

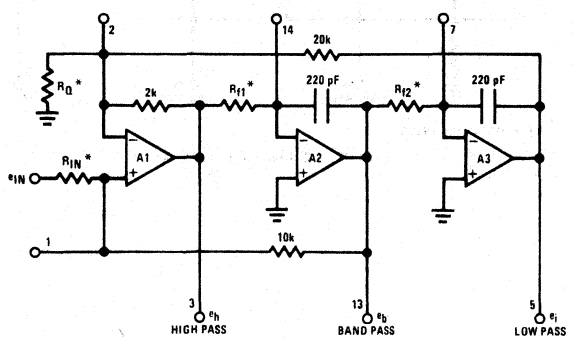
$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_o} = -\frac{1 + \frac{10^4}{R_{IN}}}{1 + \frac{R_{IN}}{10^4}} \quad (24)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220}, \; \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \frac{10^4}{R_{IN}}}{1.1 + \frac{2 \times 10^3}{R_Q}}\right] \sqrt{0.1\,\frac{\omega_2}{\omega_1}} \quad (25)$$

$$R_Q = \frac{2 \times 10^7}{\left(1 + \frac{10^4}{R_{IN}}\right)\left(\frac{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}{Q}\right) - 1.1} \quad (26)$$



*External components

FIGURE 11. Non-Inverting Input ($Q < Q_{MIN}$)

Appendix (Continued)

c) Inverting input *(Figure 12)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{-s^2\left(\frac{2\times10^3}{R_{IN}}\right)}{\Delta} \quad \text{(high pass)} \qquad (27)$$

$$\frac{e_b}{e_{IN}} = \frac{s\,\omega_1\left(\frac{2\times10^3}{R_{IN}}\right)}{\Delta} \quad \text{(band pass)} \qquad (28)$$

$$\frac{e_\ell}{e_{IN}} = \frac{-\omega_1\omega_2\left(\frac{2\times10^3}{R_{IN}}\right)}{\Delta} \quad \text{(low pass)} \qquad (29)$$

$$\omega_1 = \frac{10^{12}}{R_{f1}\cdot 220},\ \omega_2 = \frac{10^{12}}{R_{f2}\cdot 220}$$

where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1+\frac{2\times10^3}{R_{IN}}}{1+\frac{10^4}{R_Q}}\right] + 0.1\,\omega_1\omega_2 \qquad (30)$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{2\times10^4}{R_{IN}} \quad \text{(low pass) (DC gain)} \qquad (31)$$

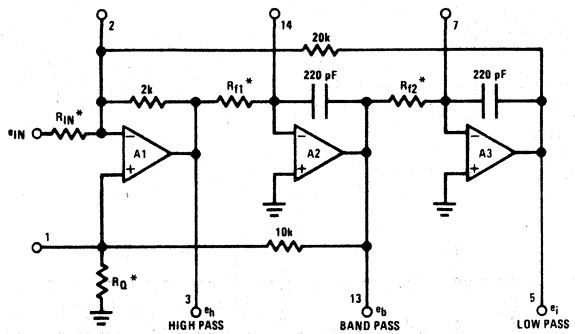
$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = -\frac{2\times10^3}{R_{IN}} \quad \text{(high pass) (high freq. gain)} \qquad (32)$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = \frac{\frac{2\times10^3}{R_{IN}}\left(1+\frac{10^4}{R_Q}\right)}{1.1+\frac{2\times10^3}{R_{IN}}} \quad \text{(band pass) (center freq. gain)} \qquad (33)$$

$$\omega_0 = \sqrt{0.1\,\omega_1\,\omega_2}$$

$$Q = \left[\frac{1+\frac{10^4}{R_Q}}{1.1+\frac{10^4}{R_{IN}}}\right]\sqrt{0.1\,\frac{\omega_2}{\omega_1}} \qquad (34)$$

$$R_Q = \frac{10^4}{\frac{Q}{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}\left(1.1+\frac{2\times10^3}{R_{IN}}\right)-1} \qquad (35)$$



*External components

FIGURE 12. Inverting Input, Any Q

Appendix (Continued)

d) Differential input *(Figure 13)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left(\frac{2\times10^3}{R_{IN2}}\right)}{\Delta} \quad \text{(high pass)} \qquad (36)$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left(\frac{2\times10^3}{R_{IN2}}\right)}{\Delta} \quad \text{(band pass)} \qquad (37)$$

$$\frac{e_l}{e_{IN}} = \frac{\omega_1\omega_2\left(\frac{2\times10^3}{R_{IN2}}\right)}{\Delta} \quad \text{(low pass)} \qquad (38)$$

$$\omega_1 = \frac{10^{12}}{R_{f1}\cdot 220}, \quad \omega_2 = \frac{10^{12}}{R_{f2}\cdot 220}$$

where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1 + \frac{2\times10^3}{R_{IN2}}}{1 + \frac{10^4}{R_Q} + \frac{10^4}{R_{IN1}}}\right] + 0.1\,\omega_1\omega_2 \qquad (39)$$

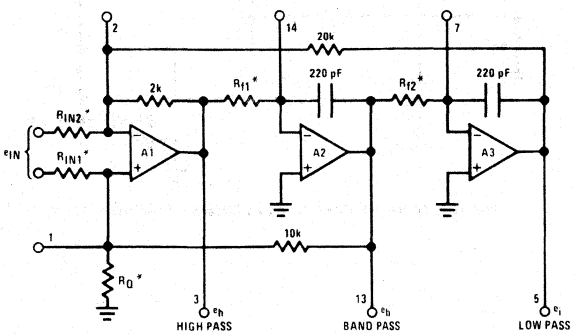
$$\left.\frac{e_l}{e_{IN}}\right|_{s\to 0} = \frac{2\times10^4}{R_{IN2}} \text{ (DC gain) (low pass)} \qquad (40)$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{2\times10^3}{R_{IN2}} \text{ (high freq. gain) (high pass)} \qquad (41)$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = \frac{\frac{2\times10^3}{R_{IN2}}\left(1 + \frac{10^4}{R_{IN1}} + \frac{10^4}{R_Q}\right)}{\left(1.1 + \frac{2\times10^3}{R_{IN2}}\right)} \text{ (center freq. gain) (band pass)} \qquad (42)$$

$$Q = \left[\frac{1 + \frac{10^4}{R_Q} + \frac{10^4}{R_{IN1}}}{1.1 + \frac{2\times10^3}{R_{IN2}}}\right]\sqrt{0.1\,\frac{\omega_2}{\omega_1}} \qquad (43)$$

$$R_Q = \frac{10^4}{\frac{Q}{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}\left(1.1 + \frac{2\times10^3}{R_{IN2}}\right) - 1 - \frac{10^4}{R_{IN1}}} \qquad (44)$$



*External components

FIGURE 13. Differential Input

Appendix (Continued)

e) Notch filter *(Figure 14)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{(s^2 + \omega_z^2)\left[\frac{1.1}{1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}}\right]\frac{R_g}{R_h}}{s^2 + s\,\omega_1\left[\frac{1.1}{1 + \frac{10^4}{R_Q} + \frac{10^4}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2} \quad (45)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220},\ \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220},\ \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\omega_z = \omega_0\sqrt{\frac{10\,R_h}{R_L}}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to 0} = \frac{11}{\left(1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}\right)}\frac{R_g}{R_L} \quad \text{(DC gain) (46)}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to \infty} = \frac{1.1}{\left(1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}\right)}\frac{R_g}{R_h} \quad \text{(high freq. gain) (47)}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega = \omega_z} = 0 \quad (48)$$

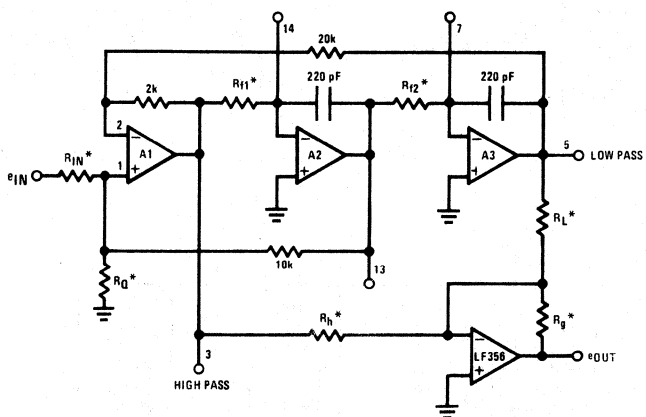


FIGURE 14. Notch Filter Using an External Amplifier

Appendix (Continued)

j) Input notch filter *(Figure 15)* transfer function equations are:

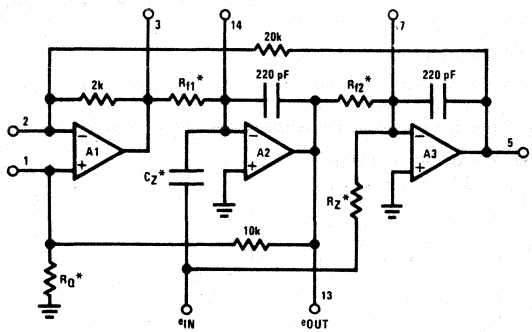
$$\frac{e_{IN}}{e_n} = -\frac{\dfrac{C_Z}{220 \times 10^{-12}}\left[s^2 + \omega_Z{}^2\right]}{s^2 + s\,\omega_1\left[\dfrac{1.1\,R_Q}{10^4 + R_Q}\right] + \omega_0{}^2} \quad (49)$$

$$\omega_Z = \omega_0 \sqrt{\frac{R_{f2} \cdot 220 \times 10^{-12}}{R_Z C_Z}}, \quad \omega_0 = \sqrt{0.1\,\omega_1\omega_2} \quad (50)$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to 0} = \frac{-R_{F2}}{R_Z} \quad (51)$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to \infty} = -\frac{C_Z}{220 \times 10^{-12}} \quad (52)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220}, \quad \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$



*External components

FIGURE 15. Input Notch Filter Using 3 Amplifiers

g) All pass *(Figure 16)* transfer function equations are:

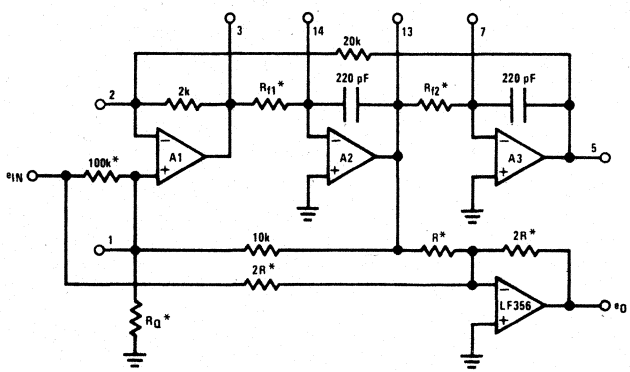
$$\frac{e_o}{e_{IN}} = -\left[\frac{s^2 - s\,\omega_1\left[\dfrac{1.1}{2 + \dfrac{R_{IN}}{R_Q}}\right] + \omega_o{}^2}{s^2 + s\,\omega_1\left[\dfrac{1.1}{2 + \dfrac{R_{IN}}{R_Q}}\right] + \omega_0{}^2}\right] \quad (53)$$

$$Q = \left[\frac{2 + \dfrac{10^4}{R_Q}}{1.1}\right]\sqrt{0.1\,\frac{\omega_2}{\omega_1}} \quad (54)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220}, \quad \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

Time delay at ω_0 is $\dfrac{2Q}{\omega_0}$ seconds



*External components

FIGURE 16. All Pass

Definition of Terms

A_{MAX}	Maximum pass band peak-to-peak ripple
A_{MIN}	Minimum stop band loss
f_z	Frequency of jw axis pole pair
f_o	Frequency of complex pole pair
Q	Quality of pole
f_c	Pass band edge
f_s	Stop band edge
R_f	Pole frequency determining resistance
R_z	Zero Frequency determining resistance
R_Q	Pole quality determining resistance
f_H	Frequency above center frequency at which the gain decreases by 3 dB for a band pass filter
f_L	Frequency below center frequency at which the gain decreases by 3 dB for a band pass filter

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AF151 Dual Universal Active Filter

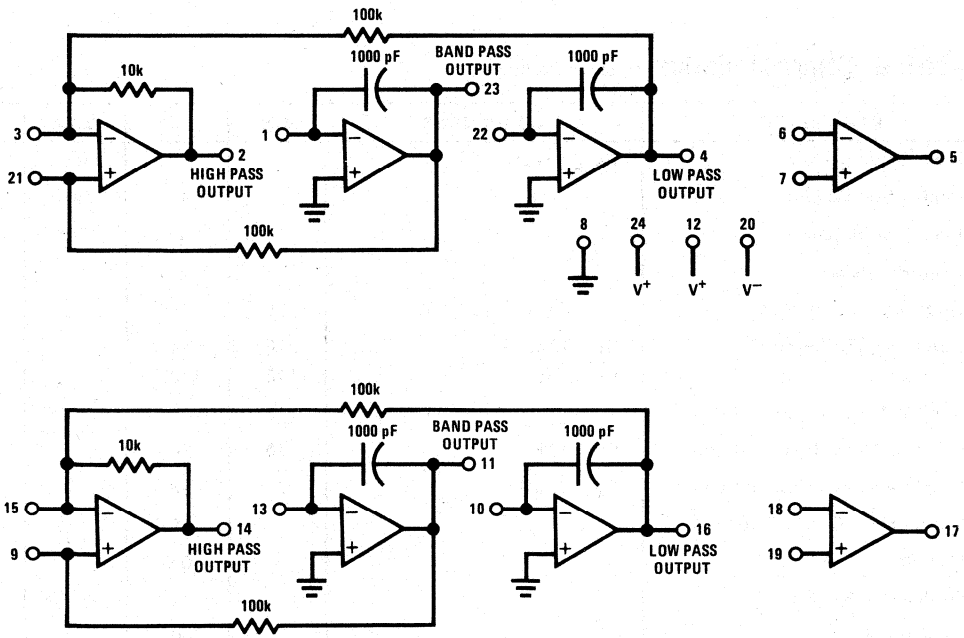
General Description

The AF151 consists of 2 general purpose state variable active filters in a single package. By using only 4 external resistors for each section, various second order functions may be formed. Low pass, high pass and band pass functions are available simultaneously at separate outputs. In addition, there are 2 uncommitted operational amplifiers which are available for buffering or for forming all pass and notch functions. Any of the classical filter configurations, such as Butterworth, Bessel, Cauer and Chebyshev can be easily formed.

Features

- Independent Q, frequency and gain adjustment
- Very low sensitivity to external component variation
- Separate low pass, high pass and band pass outputs
- Operation to 10 kHz
- Q range to 500
- Wide power supply range—±5V to ±18V
- Accuracy—±1%
- Fourth order functions in one package

Circuit Diagrams



Ceramic Dual-In-Line Package HY24A
AF151-1CJ
AF151-2CJ

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	900 mW/Package
Differential Input Voltage	±36V
Output Short-Circuit Duration (Note 1)	Infinite
Operating Temperature	−25°C to +85°C
Storage Temperature	−25°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Complete Active Filter)

Specifications apply for V_S = ±15V and over −25°C to +85°C unless otherwise specified. (Specifications apply for each section).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_c \times Q \leq 50{,}000$			10k	Hz
Q Range	$f_c \times Q \leq 50{,}000$			500	Hz/Hz
f_o Accuracy					
AF151-1C	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±2.5	%
AF151-2C	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±1.0	%
f_o Temperature Coefficient			±50	±150	ppm/°C
Q Accuracy	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±7.5	%
Q Temperature Coefficient			±300	±750	ppm/°C
Power Supply Current	V_S = ±15V		2.5	4.5	mA

Electrical Characteristics (Internal Op Amp) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance			2.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2k$, V_{OUT} = ±10V	25	160		V/mV
Output Voltage Swing	R_L = 10 kΩ	±12	±14		V
	R_L = 2 kΩ	±10	±13		V
Input Voltage Range		±12			V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		dB
Output Short-Circuit Current			25		mA
Slew Rate (Unity Gain)			0.6		V/μs
Small Signal Bandwidth			1		MHz
Phase Margin			60		Degrees

Note 1: Any of the amplifiers can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: Specifications apply for V_S = ±15V, T_A = 25°C.

Applications Information

The AF151 consists of 2 identical filter sections and 2 uncommitted op amps. The op amps may be used for buffering inputs and outputs, summing amplifiers (for notch filter generation), adjusting gain through the filter sections, additional passive networks to create higher order filters, or simply used elsewhere in the user's system.

The design equations given apply to both sections; however, for clarity, only the pin designations for section 1 will be shown in the examples and discussion.

See the AF100 data sheet for additional information on this type of filter.

The design equations assume that the user has knowledge of the frequency and Q values for the particular design to be synthesized. If this is not the case, various references and texts are available to help the user in determining these parameters. A bibliography of recommended texts can also be found in the AF100 data sheet.

CIRCUIT DESCRIPTION AND OPERATION

A schematic of one section of the AF151 is shown in *Figure 1*. Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input. Amplifier A4 is an uncommitted amplifier.

By adding external resistors the circuit can be used to generate the second order system.

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_o = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_o}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(high pass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer functions becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(band pass)}$$

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(low pass)}$$

Using proper input and output connections the circuit can also be used to generate the transfer functions for a notch and all pass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals ω_z^2 and a_3 equals 1. The transfer function becomes:

$$T(s) \quad \frac{s^2 + \omega_z^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(notch)}$$

In the all pass transfer function $a_1 = \omega_o^2$, $a_2 = -\omega_o/Q$ and $a_3 = 1$. The transfer function becomes:

$$T(s) \quad \frac{s^2 - \frac{\omega_o}{Q} s + \omega_o^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(all pass)}$$

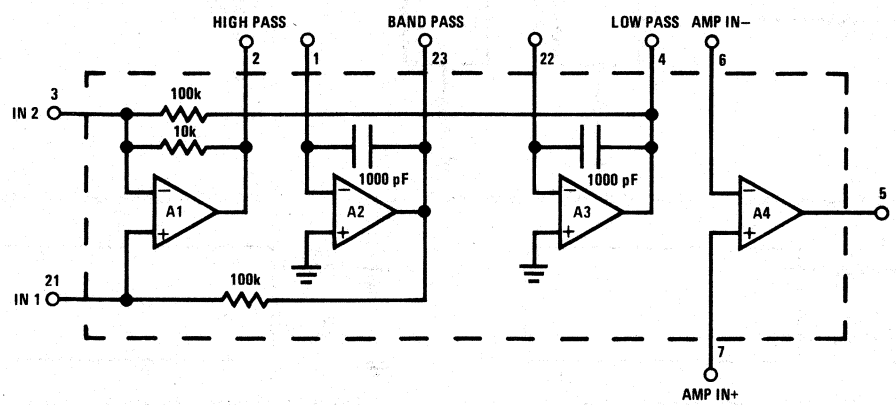


FIGURE 1. AF151 Schematic (Section 1)

Applications Information (Continued)

FREQUENCY CALCULATIONS

For operation above 200 Hz, the frequency of each section of the AF151 is set by 2 equal valued resistors. These resistors couple the output of the first op amp (pin 2) to the input of the second op amp (pin 1) and the output of the second op amp (pin 23) to the input of the third op amp (pin 22).

The value for R_f is given by:

$$R_f = \frac{50.33 \times 10^6}{f_o}\ \Omega \qquad (1)$$

For operation below 200 Hz, "T" tuning should be used as shown in *Figure 3*.

For this configuration,

$$R_S = \frac{R_T{}^2}{R_f - 2R_T} \qquad (2)$$

where R_T or R_S can be chosen arbitrarily, once R_f is found from equation 1.

Q CALCULATIONS

To set the Q of each section of the AF151, one resistor is required. The value of the Q setting resistor depends on the input connection (inverting or non-inverting) and the input resistance. Because the input resistance does affect the Q, it is often desirable to use one of the uncommitted op amps to provide a buffer between the signal source impedance and the input resistor used to set the Q.

To determine which connection is required for a particular Q, arbitrarily select a value of R_{IN} *(Figure 4)* and calculate Q_{MIN} according to equation 3.

$$Q_{MIN} = \frac{1 + \frac{10^5}{R_{IN}}}{3.48} \qquad (3)$$

If the Q required for the circuit is greater than Q_{MIN}, use equation 4 to calculate the value of R_Q and the connection shown in *Figure 4*.

$$R_Q = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}} \qquad (4)$$

If the Q required for the circuit is less than Q_{MIN}, use equation 5 to calculate the value of R_Q and the connection shown in *Figure 5*.

$$R_Q = \frac{10^4}{\frac{0.3162}{Q}\left(1 + \frac{10^5}{R_{IN}}\right) - 1.1} \qquad (5)$$

Both connections shown in *Figures 4 and 5* are "non-inverting" relative to the phase relationship between the input signal and the low pass output.

For any Q, equation 6 may be used with the "inverting" connection shown in *Figure 6*.

$$R_Q = \frac{10^5}{3.16\,Q\left(1.1 + \frac{10^4}{R_{IN}}\right) - 1} \qquad (6)$$

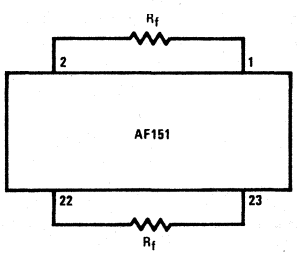


FIGURE 2. Frequency Tuning

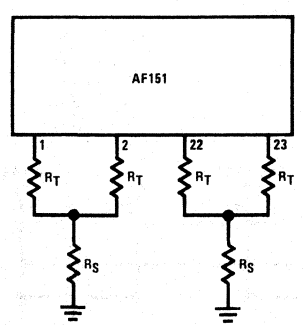


FIGURE 3. "T" Tuning for Low Frequency

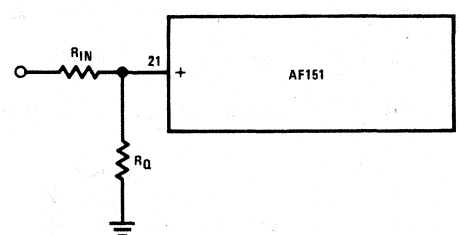


FIGURE 4. Connection for Q > Q_{MIN}

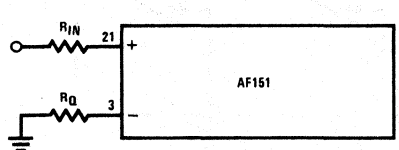


FIGURE 5. Connection for Q < Q_{MIN}

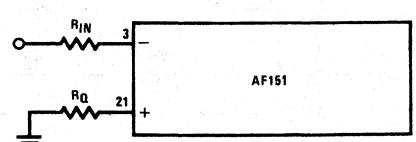


FIGURE 6. Connection for Any Q, Inverting

Applications Information (Continued)

NOTCH TUNING

When the low pass output and the high pass output are summed together, the result is a notch *(Figure 7)*.

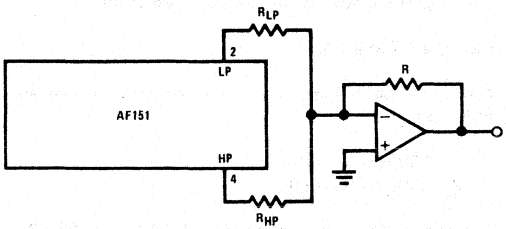


FIGURE 7. Notch Filter

The relationship between R_{LP}, R_{HP}, f_o and f_z, the location of the notch, is given by equation 7.

$$R_{HP} = \left(\frac{f_z}{f_o}\right)^2 \frac{R_{LP}}{10} \qquad (7)$$

Again, it is advantageous to use one of the uncommitted op amps to perform this summing function to prevent loading of this stage or the resistors R_{LP} and R_{HP} from effecting the Q of subsequent stages. Resistor R can be used to set the gain of the filter section.

GAIN CALCULATIONS

The following list of equations will be helpful in calculating the relationship between the external components and various important parameters. The following definitions are use:

A_L – Gain from input to low pass output at DC
A_H – Gain from input to high pass output at high frequency
A_B – Gain from input to band pass output at center frequency

For *Figure 4*:

$$A_L = \frac{11}{\Delta}$$

$$A_H = \frac{1.1}{\Delta}$$

$$A_B = \frac{-\left(1 + \frac{10^5}{R_Q} + \frac{10^5}{R_{IN}}\right)}{\Delta}$$

$$\Delta = 1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}$$

For *Figure 5:*

$$A_L = \frac{11 + \frac{10^5}{R_Q}}{\Delta}$$

$$A_H = \frac{1.1 + \frac{10^4}{R_Q}}{\Delta}$$

$$A_B = \frac{-\left(1 + \frac{10^5}{R_{IN}}\right)}{\Delta}$$

$$\Delta = 1 + \frac{R_{IN}}{10^5}$$

For *Figure 6:*

$$A_L = -\frac{10^5}{R_{IN}}$$

$$A_H = -\frac{10^4}{R_{IN}}$$

$$A_B = \frac{\frac{10^5}{R_{IN}}\left(1 + \frac{10^5}{R_Q}\right)}{11 + \frac{10^5}{R_{IN}}}$$

For *Figure 7*:

At low frequency, when $f_o < f_z$, the gain to the output of the summing op amp is:

$$A_L = \frac{11\left(\frac{R}{R_{LP}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)}$$

At high frequency, when $f_o > f_z$, the gain to the output of the summing op amp is:

$$A_H = \frac{1.1\left(\frac{R}{R_{HP}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)}$$

At the notch, ideally the gain is zero (0).

TUNING TIPS

In applications where 2% to 3% accuracy is not sufficient to provide the required filter response, the AF151 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the band pass output.

Before any tuning is attempted, the low pass output should be checked to see that the output is not clipping. At the center frequency of the section, the low pass output is 10 dB higher than the band pass output and 20 dB higher than the high pass. This should be kept in mind because if clipping occurs, the results obtained when tuning will be incorrect.

Applications Information (Continued)

Frequency Tuning

By adjusting resistor R_f, center frequency of a section can be adjusted. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

Q Tuning

The Q is tuned by adjusting the R_Q resistor. To tune the Q correctly, the signal source must have an output impedance very much lower than the input resistance of the filter since the input resistance affects the Q. The input must be driven through the same resistance the circuit will "see" to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right) \times (f_o)$$

where f_o = center frequency

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q}\right) \times (f_o)$$

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair, the notch can be tuned by adjusting the ratio of the summing resistors (low pass/high pass summing).

In either case, the signal is connected to the input and the proper resistor is adjusted for a null at the output.

TUNING PROCEDURE

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the low pass output.

Adjust the R_f resistor until the phase shift between input and band pass output is 180° or 0°, depending upon the connection.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

Zero Tuning (Notch Tuning)

Set the oscillator output to the zero frequency and tune one of the summing resistors for a null at the output of the summing amplifier.

Gain Adjust

Set the oscillator to any desired frequency and the gain can be adjusted by measuring the output of the summing amplifier and adjusting the feedback resistance.

DESIGN EXAMPLE

Assume 2 band pass filters are required to separate FSK data.

f1 = 800 Hz, Q = 40
f2 = 1000 Hz, Q = 50

The gain through each filter is to be 10 V/V (20 dB).

Since the design is similar for both sections, only the first section design will be shown for the example.

(a) From equation 1

$$R_f = \frac{50.33 \times 10^6}{f_o} = \frac{50.33 \times 10^6}{800}$$

$$\boxed{R_f = 62.9k}$$

(b) Checking Q_{MIN} from equation 3, arbitrarily let R_{IN} = 300k.

$$Q_{MIN} = \frac{1 + \frac{10^5}{R_{IN}}}{3.48} = \frac{1 + \frac{10^5}{3 \times 10^5}}{3.48} = 0.383$$

Since the Q required for the design (Q = 40), is greater than Q_{MIN}, the circuit of *Figure 4* or *Figure 6* may be used. Arbitrarily we shall select the circuit of *Figure 4*.

(c) From equation 4, R_Q is found to be

$$R_Q = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}} = \frac{10^5}{(3.48)(40) - 1 - \frac{10^5}{3 \times 10^5}}$$

or $\boxed{R_Q = 725\Omega}$

(d) Calculate the center frequency gain for *Figure 4*.

$$A_B = \frac{-\left(1 + \frac{10^5}{R_Q} + \frac{10^5}{R_{IN}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)} = \frac{-(1 + 137.9 + 0.333)}{(1 + 3.0 + 414)}$$

$$A_B = 0.333 \text{ V/V}$$

Since the gain at f_o is 0.333 V/V, a gain of 10 V/V can be obtained by using the uncommitted operational amplifier with a gain of 30.03 as shown in *Figure 8*.

Applications Information (Continued)

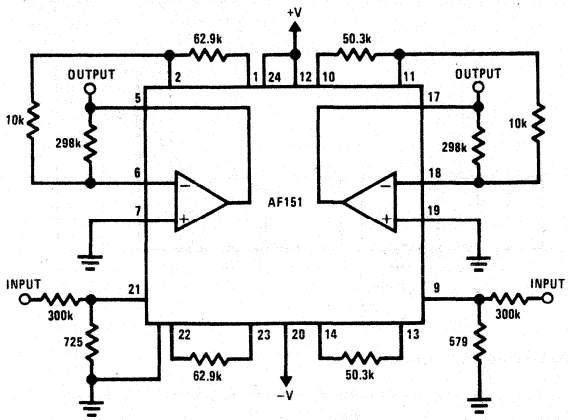


FIGURE 8. Dual Band Pass Filter

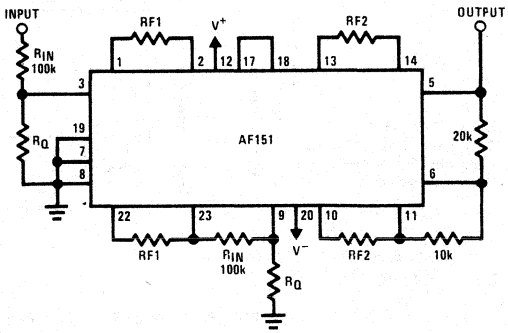


FIGURE 9. Telephone Multifrequency (MF) Band Pass Filter

FREQ	BW	f_c	f1	Q1 & Q2	f2	RF1	RF2	RQ
700	75	698.4	665.6	17	732.8	75.62k	68.68k	1.749k
900	75	898.7	865.8	21.8	932.9	58.13k	53.95k	1.354k
1100	75	1098.8	1065.7	26.7	1132.9	47.23k	44.43k	1.100k
1300	75	1298.9	1265.8	31.6	1332.9	39.76k	37.76k	926.2Ω
1500	75	1499.0	1465.8	36.4	1532.9	34.34k	32.83k	802.1Ω
1700	75	1699.1	1665.9	41.3	1733.0	30.21k	29.04k	705.6Ω

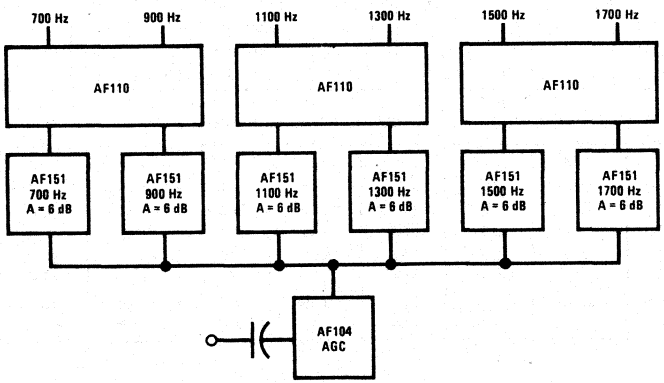
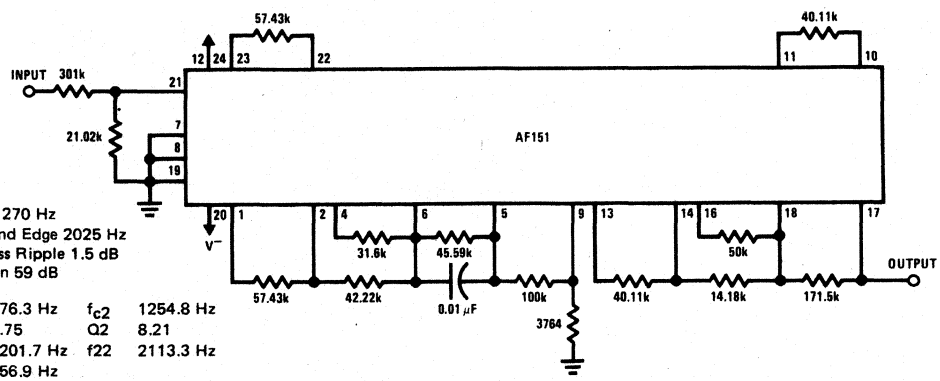


FIGURE 10. MF Tone Receiver

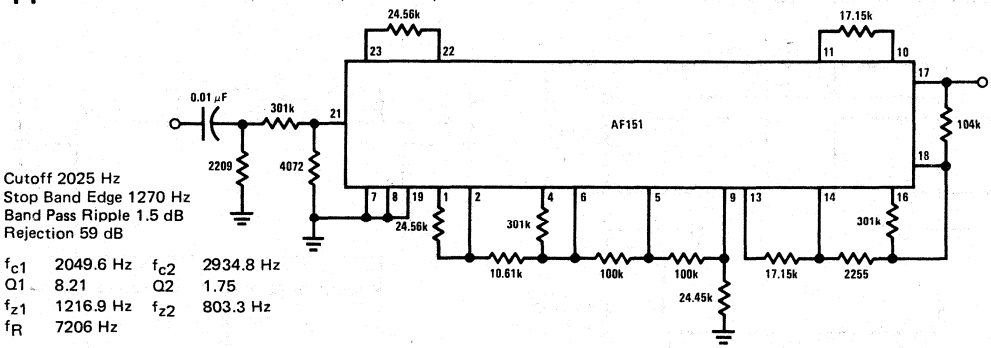


Cutoff 1270 Hz
Stop Band Edge 2025 Hz
Band Pass Ripple 1.5 dB
Rejection 59 dB

f_{c1}	876.3 Hz	f_{c2}	1254.8 Hz
Q1	1.75	Q2	8.21
f_{z1}	3201.7 Hz	f22	2113.3 Hz
f_R	356.9 Hz		

FIGURE 11. Low Pass Low Speed Asynchronous FSK Modem Filter

Applications Information (Continued)



Cutoff 2025 Hz
Stop Band Edge 1270 Hz
Band Pass Ripple 1.5 dB
Rejection 59 dB

f_{c1}	2049.6 Hz	f_{c2}	2934.8 Hz
Q1	8.21	Q2	1.75
f_{z1}	1216.9 Hz	f_{z2}	803.3 Hz
f_R	7206 Hz		

FIGURE 12. High Pass Low Speed Asynchronous FSK Modem Filter

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.33 can represent 1.33Ω, 133Ω, 1.33 kΩ, 13.3 kΩ, 133 kΩ 1.33 MΩ.

Standard 5% and 2% Resistance Values

OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	MEGOHMS	
10	27	68	180	470	1,200	3,300	8,200	22,000	56,000	150,000	0.24	0.62
11	30	75	200	510	1,300	3,600	9,100	24,000	62,000	160,000	0.27	0.68
12	33	82	220	560	1,500	3,900	10,000	27,000	68,000	180,000	0.30	0.75
13	36	91	240	620	1,600	4,300	11,000	30,000	75,000	200,000	0.33	0.82
15	39	100	270	680	1,800	4,700	12,000	33,000	82,000	220,000	0.36	0.91
16	43	110	300	750	2,000	5,100	13,000	36,000	91,000		0.39	1.0
18	47	120	330	820	2,200	5,600	15,000	39,000	100,000		0.43	1.1
20	51	130	360	910	2,400	6,200	16,000	43,000	110,000		0.47	1.2
22	56	150	390	1,000	2,700	6,800	18,000	47,000	120,000		0.51	1.3
24	62	160	430	1,100	3,000	7,500	20,000	51,000	130,000		0.56	1.5

Decade Table Determining 1/2% and 1% Standard Resistance Values

1.00	1.21	1.47	1.78	2.15	2.61	3.16	3.83	4.64	5.62	6.81	8.25
1.02	1.24	1.50	1.82	2.21	2.67	3.24	3.92	4.75	5.76	6.98	8.45
1.05	1.27	1.54	1.87	2.26	2.74	3.32	4.02	4.87	5.90	7.15	8.66
1.07	1.30	1.58	1.91	2.32	2.80	3.40	4.12	4.99	6.04	7.32	8.87
1.10	1.33	1.62	1.96	2.37	2.87	3.48	4.22	5.11	6.19	7.50	9.09
1.13	1.37	1.65	2.00	2.43	2.94	3.57	4.32	5.23	6.34	7.68	9.31
1.15	1.40	1.69	2.05	2.49	3.01	3.65	4.42	5.36	6.49	7.87	9.53
1.18	1.43	1.74	2.10	2.55	3.09	3.74	4.53	5.49	6.65	8.06	9.76

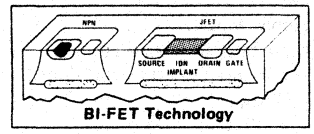
Section 3

Amplifiers

3

Section Contents

National Semiconductor



LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

LF155, LF155A, LF255, LF355, LF355A, LF355B Low Supply Current
LF156, LF156A, LF256, LF356, LF356A, LF356B Wide Band
LF157, LF157A, LF257, LF357, LF357A, LF357B Wide Band Decompensated ($A_{V_{MIN}} = 5$)

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

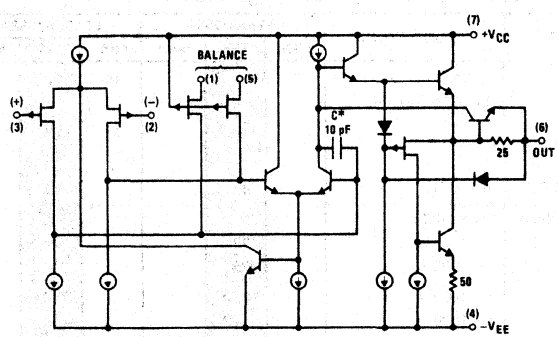
(LF155A, LF156A, LF157A)

Low input bias current	30 pA
Low Input Offset Current	3 pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1 mV
Low input offset voltage temperature drift	$3\mu V/°C$
Low input noise current	0.01 $pA/\sqrt{Hz}$
High common-mode rejection ratio	100 dB
Large dc voltage gain	106 dB

Uncommon Features

	LF155A	LF156A	LF157A ($A_V = 5$)*	UNITS
Extremely fast settling time to 0.01%	4	1.5	1.5	μs
Fast slew rate	5	12	50	$V/\mu s$
Wide gain bandwidth	2.5	5	20	MHz
Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

Simplified Schematic



*C = 2 pF on LF157

Absolute Maximum Ratings

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7 LF356B/6B/7B	LF355A/6A/7A LF355/6/7
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}) (Note 1)				
T_{jMAX}				
(H and J Package)	150°C	150°C	115°C	115°C
(N Package)			100°C	100°C
(H Package) P_d	670 mW	670 mW	570 mW	570 mW
θ_{jA}	150°C/W	150°C/W	150°C/W	150°C/W
(J Package) P_d	670 mW	670 mW	570 mW	570 mW
θ_{jA}	140°C/W	140°C/W	140°C/W	140°C/W
(N Package) P_d			500 mW	500 mW
θ_{jA}			155°C/W	155°C/W
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1	2		1	2	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	10		3	10	pA
		$T_j \leq T_{HIGH}$			10			1	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_J \leq T_{HIGH}$			25			5	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = ±15V$, $T_A = 25°C$ $V_O = ±10V$, $R_L = 2k$	50	200		50	200		V/mV
		Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = ±15V$, $R_L = 10k$	±12	±13		±12	±13		V
		$V_S = ±15V$, $R_L = 2k$	±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = ±15V$	±11	+15.1 −12		±11	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = 25°C$, $V_S = ±15V$

SYMBOL	PARAMETER	CONDITIONS	LF155A/355A			LF156A/356A			LF157A/357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	LF155A/6A; $A_V = 1$,	3	5		10	12					V/μs
		LF157A; $A_V = 5$							40	50		V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz		25			15			15		$nV/\sqrt{Hz}$
		f = 1000 Hz		25			12			12		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_j \leq T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$ $V_O = \pm10V$, $R_L = 2k$	50	200		50	200		25	200		V/mV
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		±12	±13		V
		$V_S = \pm15V$, $R_L = 2k$	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1 −12		±11	+15.1 −12		±10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

PARAMETER	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157 LF257/357B		LF357A/357		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155/255/ 355/355B	LF156/256, LF356B	LF156/256/ 356/356B	LF157/257, LF357B	LF157/257/ 357/357B	UNITS
			TYP	MIN	TYP	MIN	TYP	
SR	Slew Rate	LF155/6: $A_V = 1$,	5	7.5	12			V/μs
		LF157: $A_V = 5$				30	50	V/μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$						
		f = 100 Hz	25		15		15	$nV/\sqrt{Hz}$
		f = 1000 Hz	20		12		12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
		f = 1000 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155/6/7	LF255/6/7	LF355A/6A/7A	LF355B/6B/7B	LF355/6/7
Supply Voltage, V_S	$\pm15V \le V_S \le \pm20V$	$\pm15V \le V_S \le \pm20V$	$\pm15V \le V_S \le \pm18V$	$\pm15V \le V_S \pm20V$	$V_S = \pm15V$
T_A	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ Pd where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

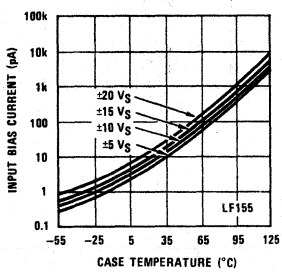
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 3-11).

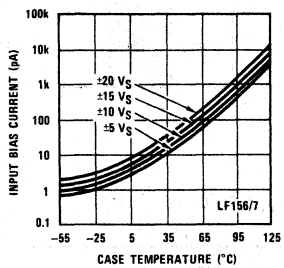
Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.

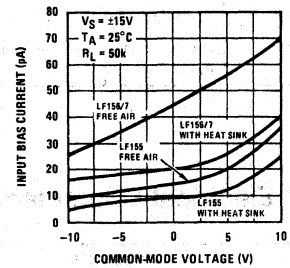
Input Bias Current



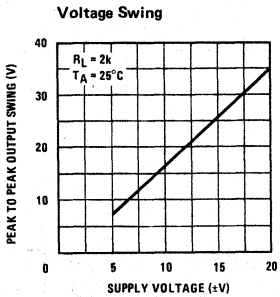
Input Bias Current



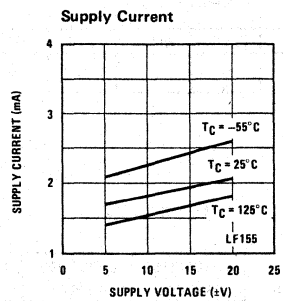
Input Bias Current



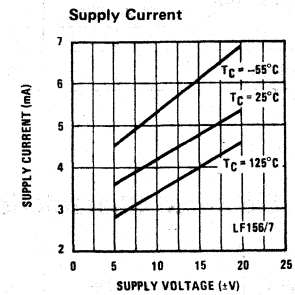
Voltage Swing



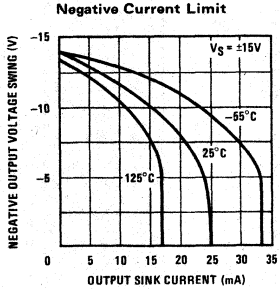
Supply Current



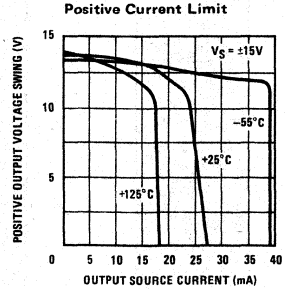
Supply Current



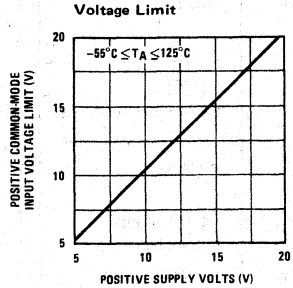
Negative Current Limit



Positive Current Limit

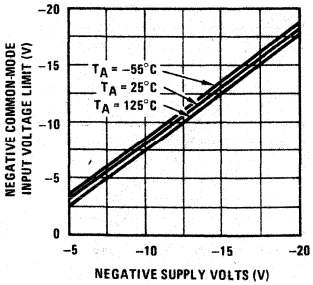


Positive Common-Mode Input Voltage Limit

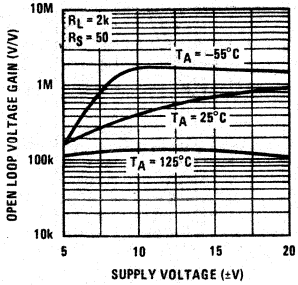


Typical DC Performance Characteristics (Continued)

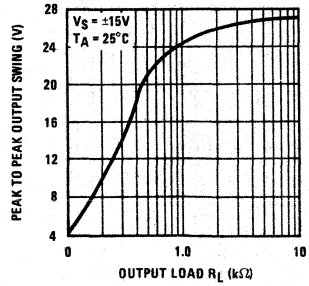
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

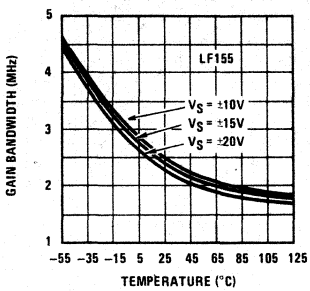


Output Voltage Swing

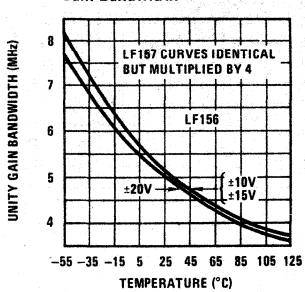


Typical AC Performance Characteristics

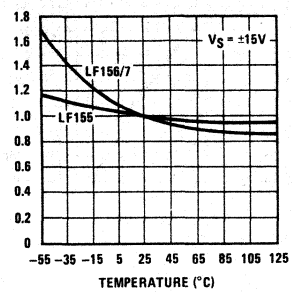
Gain Bandwidth



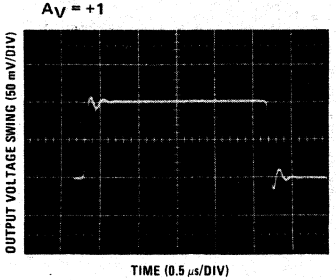
Gain Bandwidth



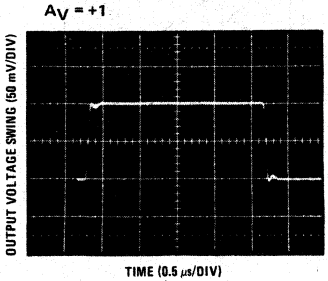
Normalized Slew Rate



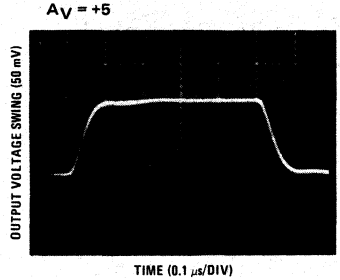
LF155 Small Signal Pulse Response, A_V = +1



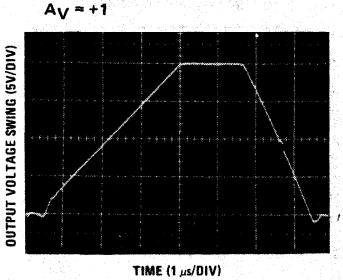
LF156 Small Signal Pulse Response, A_V = +1



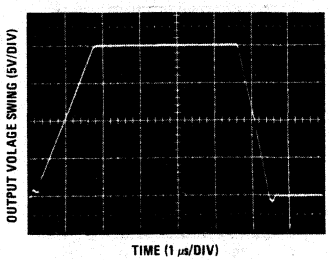
LF157 Small Signal Pulse Response, A_V = +5



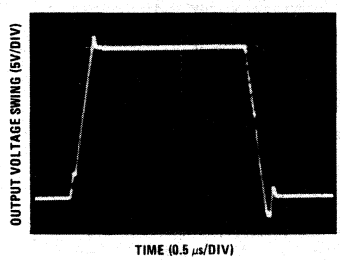
LF155 Large Signal Pulse Response, A_V = +1



LF156 Large Signal Pulse Response, A_V = +1

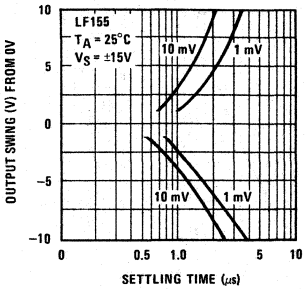


LF157 Large Signal Pulse Response, A_V = +5

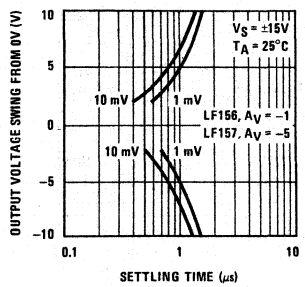


Typical AC Performance Characteristics (Continued)

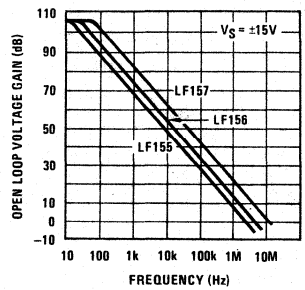
Inverter Settling Time



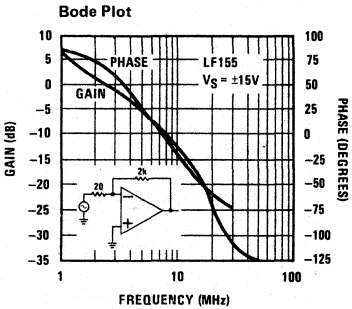
Inverter Settling Time



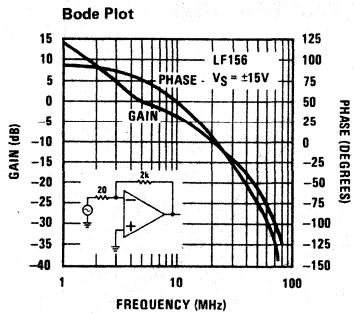
Open Loop Frequency Response



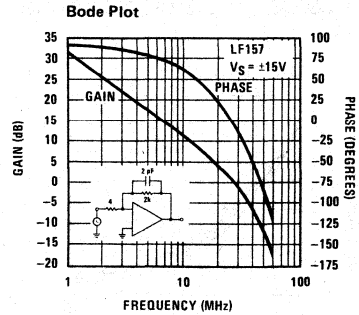
Bode Plot



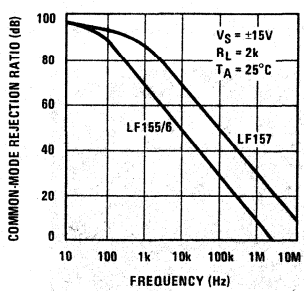
Bode Plot



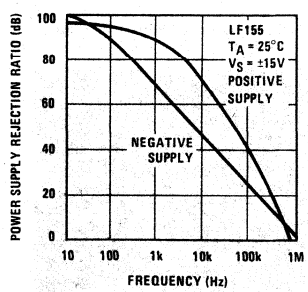
Bode Plot



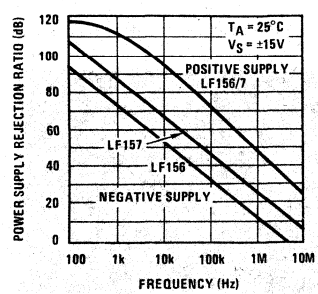
Common-Mode Rejection Ratio



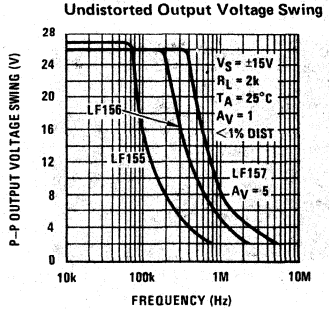
Power Supply Rejection Ratio



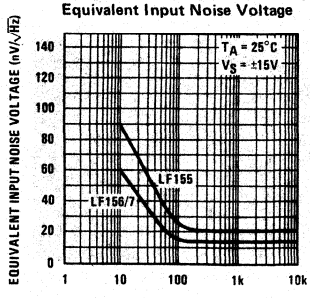
Power Supply Rejection Ratio



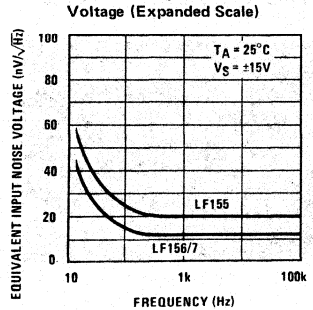
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

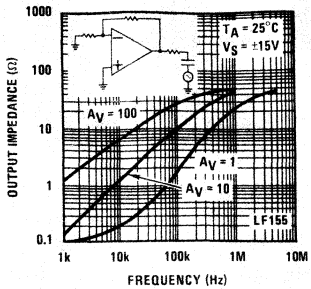


Equivalent Input Noise Voltage (Expanded Scale)

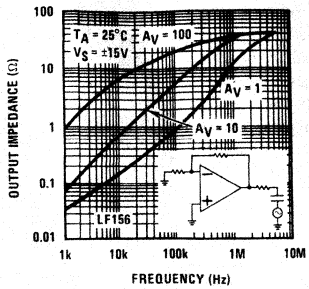


Typical AC Performance Characteristics (Continued)

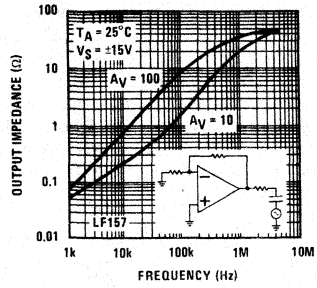
Output Impedance



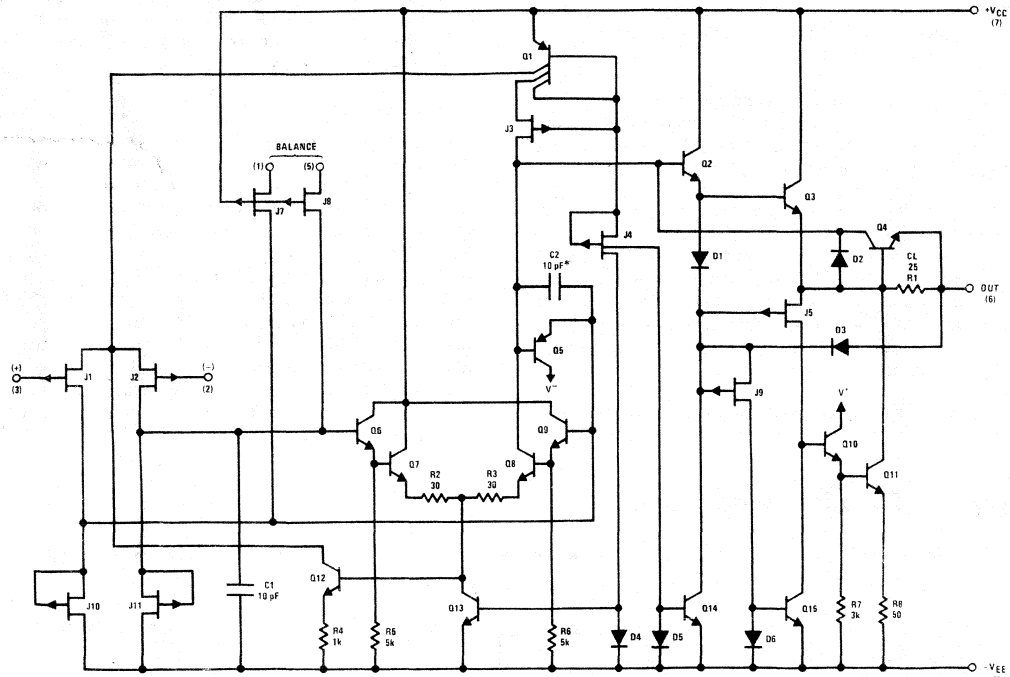
Output Impedance



Output Impedance



Detailed Schematic



*C = 2 pF on LF157

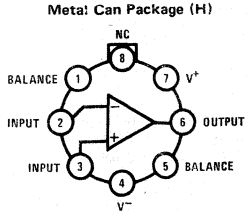
Connection Diagrams (Top Views)

Order Number

LF155AH	LF156AH	LF157AH
LF155H	LF156H	LF157H
LF255H	LF256H	LF257H
LF355AH	LF356AH	LF357AH
LF355H	LF356H	LF357H

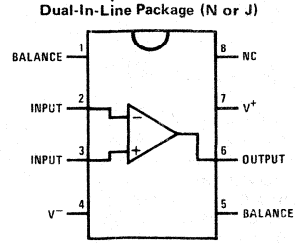
See NS Package H08C

Metal Can Package (H)



Note 4: Pin 4 connected to case.

Dual-In-Line Package (N or J)



Order Number LF355N, LF356N or LF357N
See NS Package N08B

Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

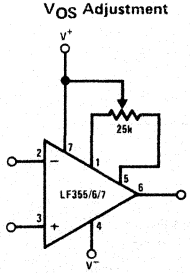
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

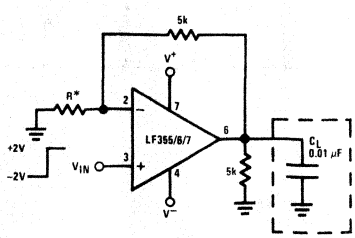
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



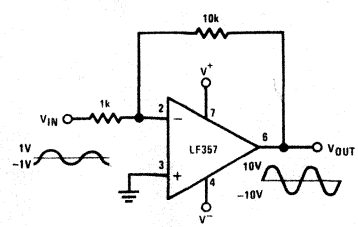
*LF155/6 R = 5k
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \cong 0.01\ \mu F$.

Overshoot ≤ 20%

Settling time (t_s) ≅ 5 μs

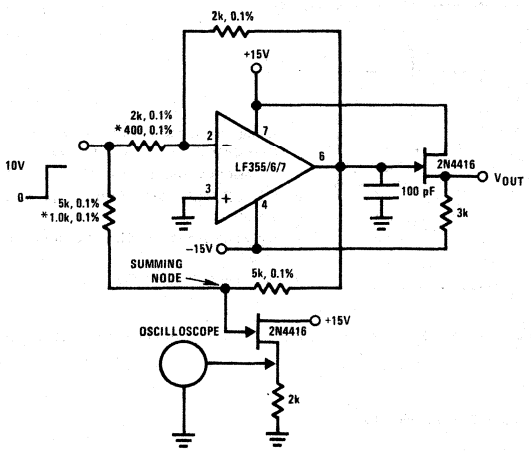
LF157. A Large Power BW Amplifier



For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

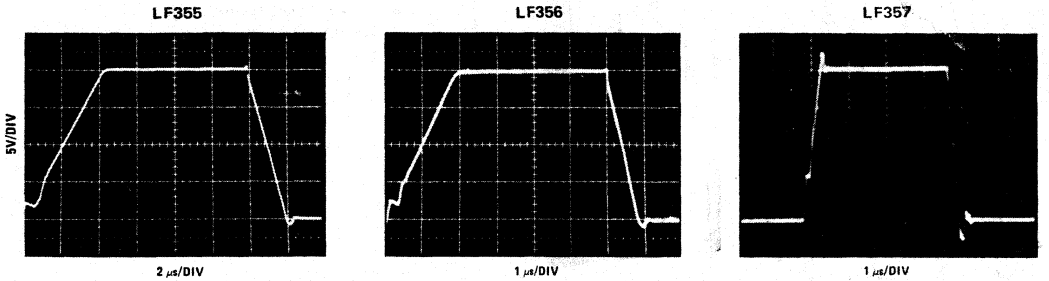
Typical Applications

Settling Time Test Circuit

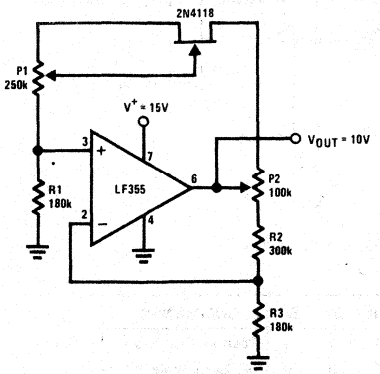


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



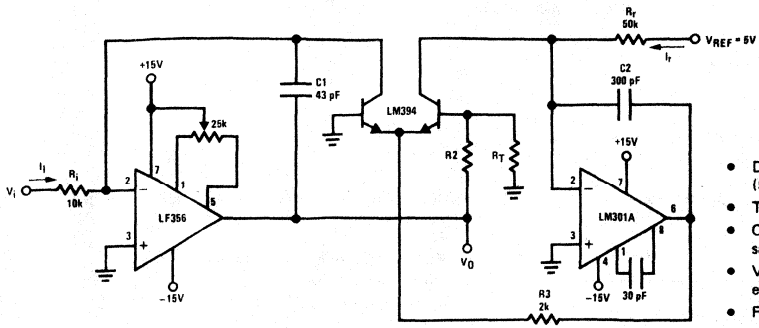
Low Drift Adjustable Voltage Reference



- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - ▲ Low I_B
  - ▲ Low drift
  - ▲ Low supply current

Typical Applications (Continued)

Fast Logarithmic Converter

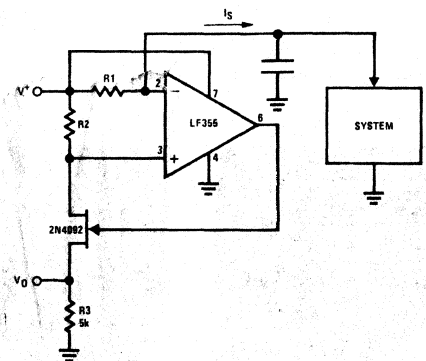


- Dynamic range: 100 μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_i \frac{1}{R_i\, I_r}$$

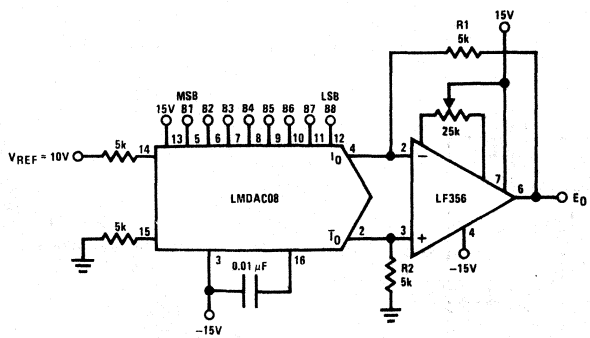
R2 = 15.7k, R_T = 1k, 0.3%/°C (for temperature compensation)

Precision Current Monitor



- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low supply current

8-Bit D/A Converter with Symmetrical Offset Binary Operation

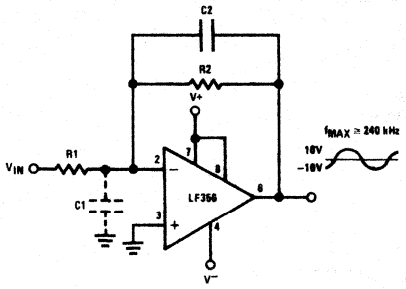


- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3 μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	COMMENTS
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

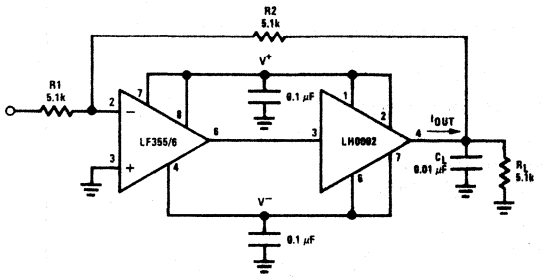
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



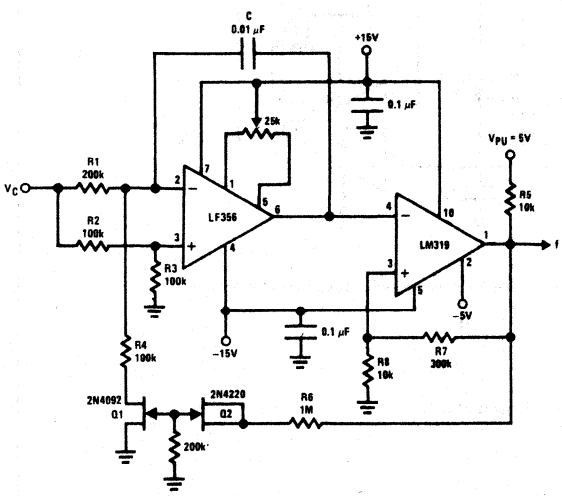
- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 240$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/µs (with C_L shown)
- No additional phase shift added by the current amplifier

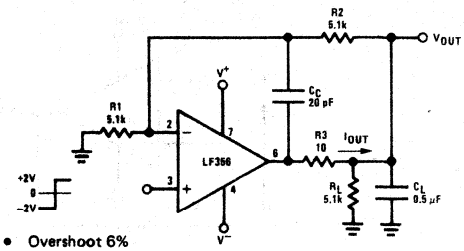
3 Decades VCO



$f = \frac{V_C\,(R8+R7)}{[8\,V_{PU}\,R8\,R1]\,C}$, $0 \leq V_C \leq 30V$, 10 Hz ≤ f ≤ 10 kHz

R1, R4 matched. Linearity 0.1% over 2 decades.

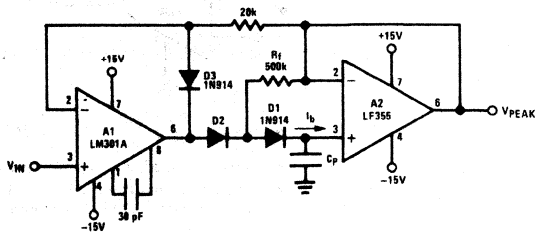
Isolating Large Capacitive Loads



- Overshoot 6%
- t_s 10 µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

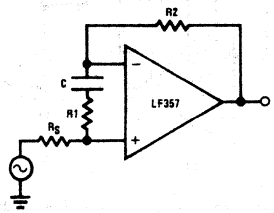
$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5} \text{ V/µs} = 0.04 \text{ V/µs (with } C_L \text{ shown)}$$

Low Drift Peak Detector



- By adding D1 and R_f, V_{D1} = 0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of C_P.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be << $1/2\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

Non-Inverting Unity Gain Operation for LF157



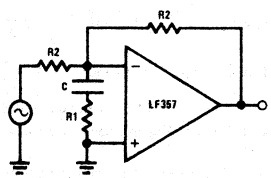
$R1C \geq \frac{1}{(2\pi)\ (5\text{ MHz})}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3\,dB} \approx 5$ MHz

Inverting Unity Gain for LF157



$R1C \geq \frac{1}{(2\pi)\ (5\text{ MHz})}$

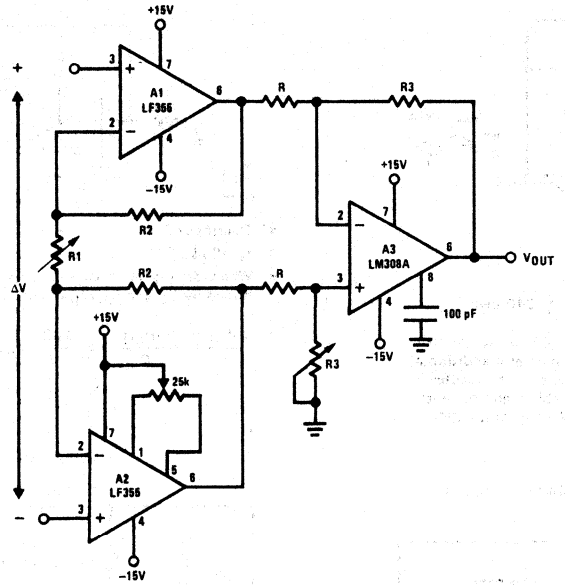
$R1 = \frac{R2}{4}$

$A_{V(DC)} = -1$

$f_{-3\,dB} \approx 5$ MHz

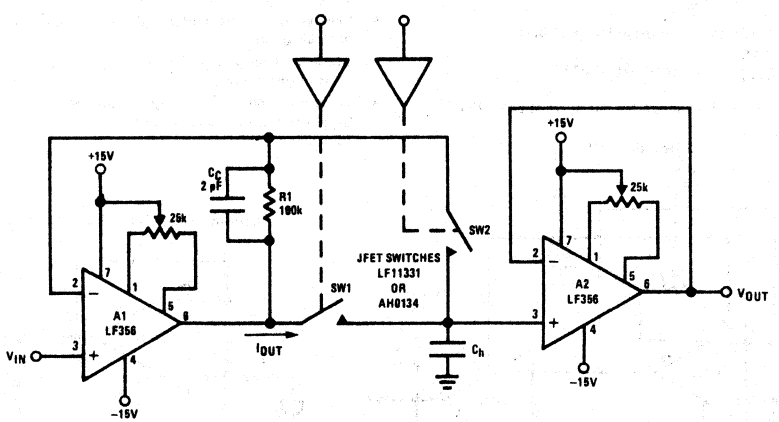
Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V$, $V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier Resistor array RA201 (National Semiconductor) recommended

Fast Sample and Hold



- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

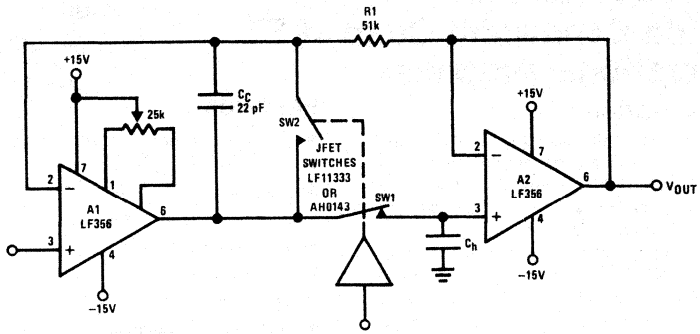
  $T_A \cong \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_h}{S_r}\right]^{1/2}$ provided that:

  $V_{IN} < 2\pi S_r R_{ON} C_h$ and $T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}$, R_{ON} is of SW1

  If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20\ mA}$
- LF156 developes full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

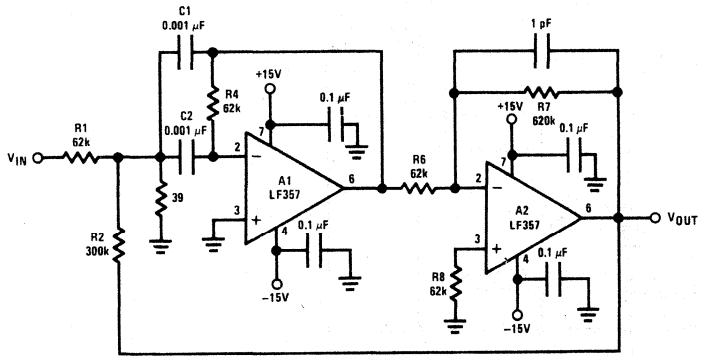
Typical Applications (Continued)

High Accuracy Sample and Hold



- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - ▲ Fast settling time
  - ▲ Low V_{OS}

High Q Band Pass Filter

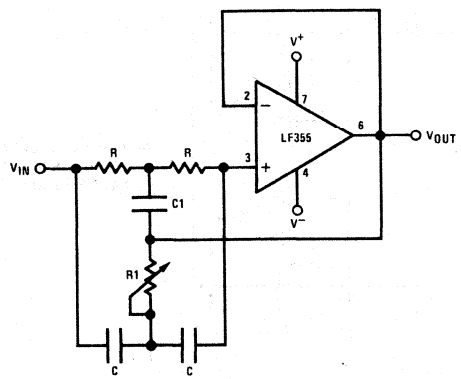


- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

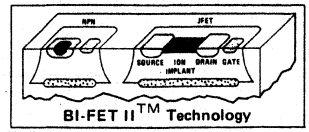
High Q Notch Filter



- 2R1 = R = 10 MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - ▲ Low I_B
  - ▲ Low supply current

National Semiconductor

LF347 Wide Bandwidth Quad JFET Input Operational Amplifier



General Description

The LF347 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF347 is pin compatible with the standard LM348. This feature allows designers to immediately upgrade the overall performance of existing LM348 and LM324 designs.

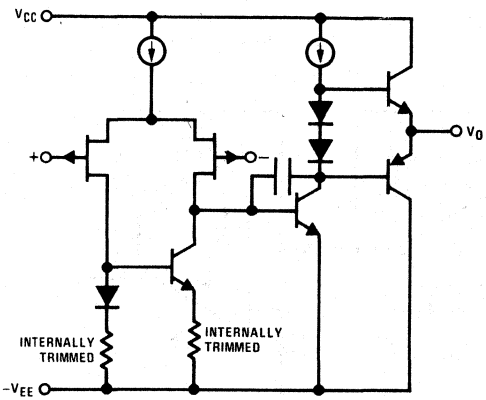
The LF347 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage 2 mV
- Low input bias current 50 pA
- Low input noise voltage 16 nV/√Hz
- Low input noise current 0.01 pA/√Hz
- Wide gain bandwidth 4 MHz
- High slew rate 13 V/μs
- Low supply current 7.2 mA
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz <0.02%
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

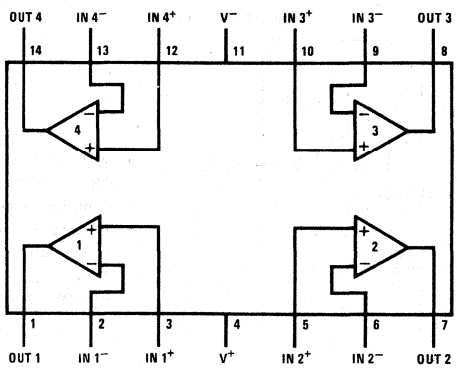
Simplified Schematic

1/4 Quad



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LF347N, LF347AN or LF347BN
See NS Package N14A

Order Number LF347J, LF347AJ or LF347BJ
See NS Package J14A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
T_j(MAX)	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF347A			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10			10			10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 4, 5)		25	100		25	100		25	100	pA
		$T_j \leq 70°C$			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 4, 5)		50	200		50	200		50	200	pA
		$T_j \leq 70°C$			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF347A			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz–20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13			13			13		V/μs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 125°C/W junction to ambient or 95°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: P_D max rating cannot be exceeded.

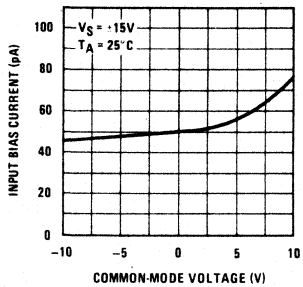
Note 4: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

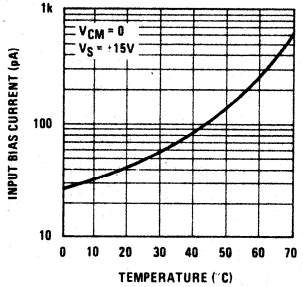
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

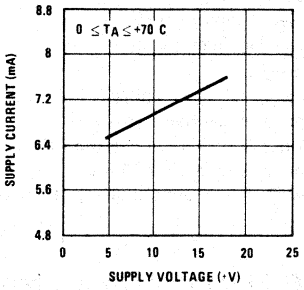
Input Bias Current



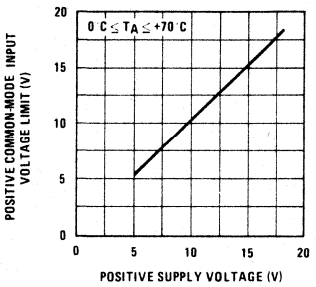
Input Bias Current



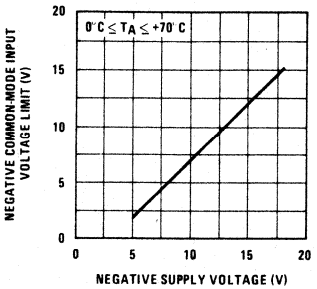
Supply Current



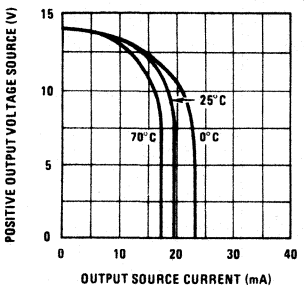
Positive Common-Mode Input Voltage Limit



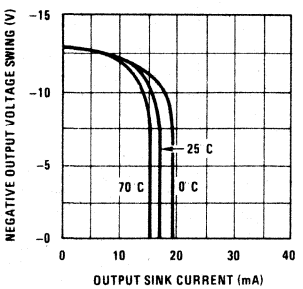
Negative Common-Mode Input Voltage Limit



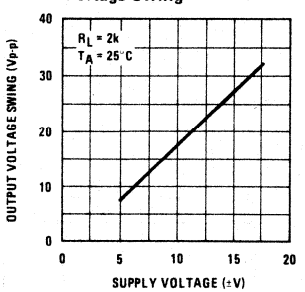
Positive Current Limit



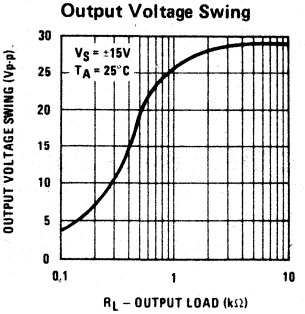
Negative Current Limit



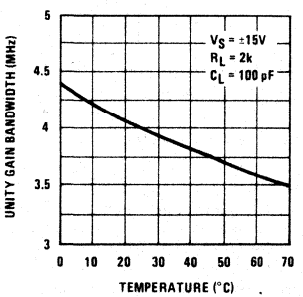
Voltage Swing



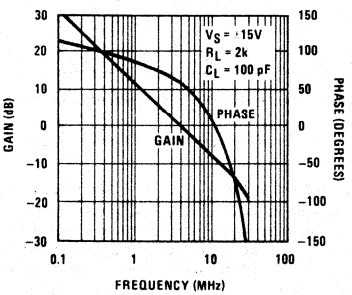
Output Voltage Swing



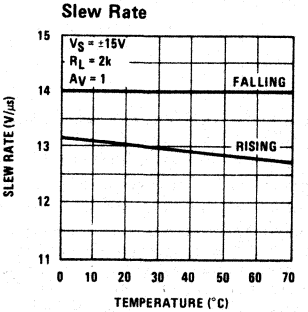
Gain Bandwidth



Bode Plot

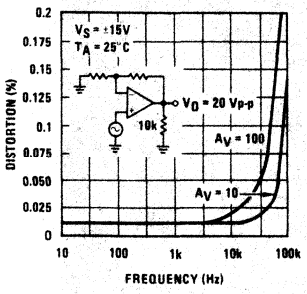


Slew Rate

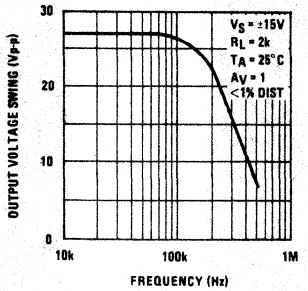


Typical Performance Characteristics (Continued)

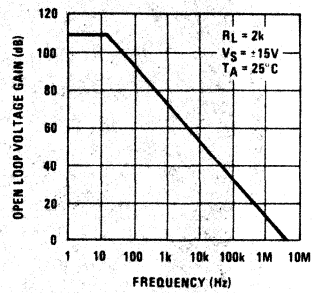
Distortion vs Frequency



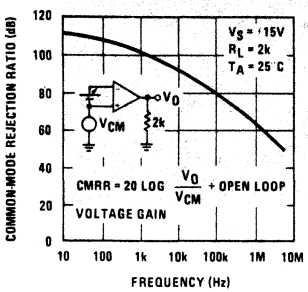
Undistorted Output Voltage Swing



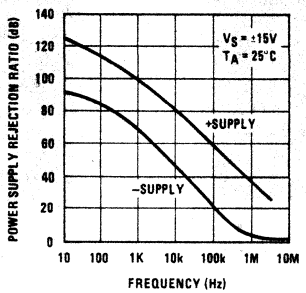
Open Loop Frequency Response



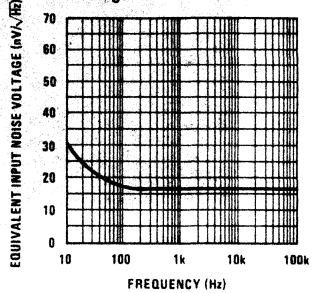
Common-Mode Rejection Ratio



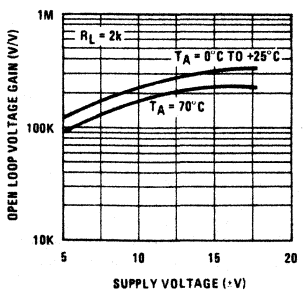
Power Supply Rejection Ratio



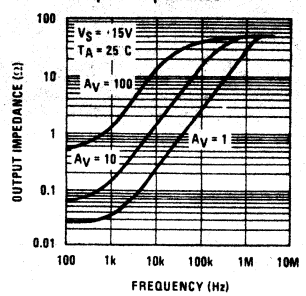
Equivalent Input Noise Voltage



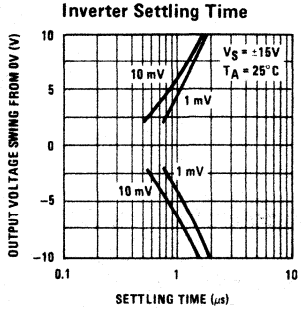
Open Loop Voltage Gain (V/V)



Output Impedance

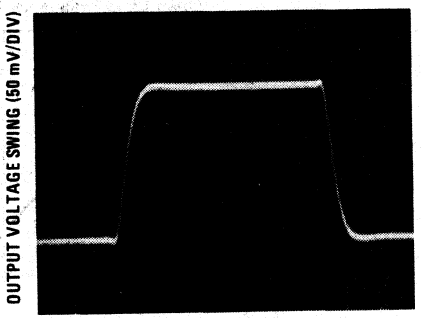


Inverter Settling Time

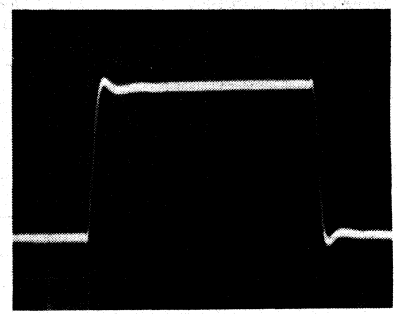


Pulse Response

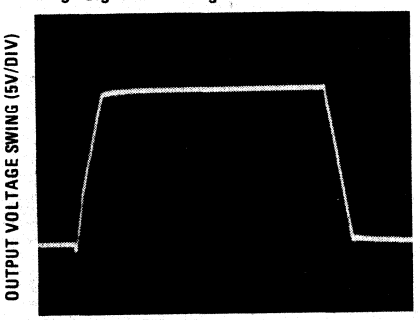
Small Signal Inverting



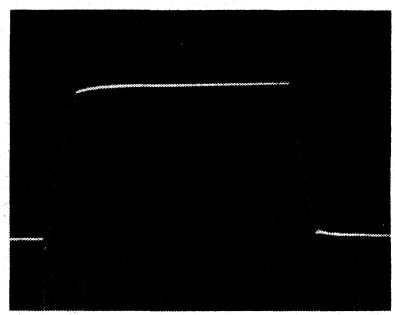
Small Signal Non-Inverting



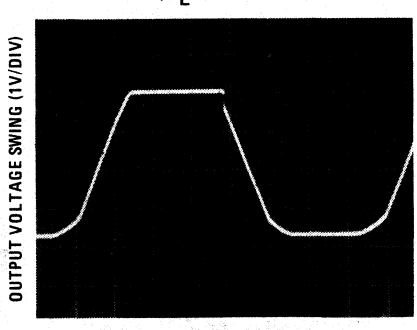
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

The LF347 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF347 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

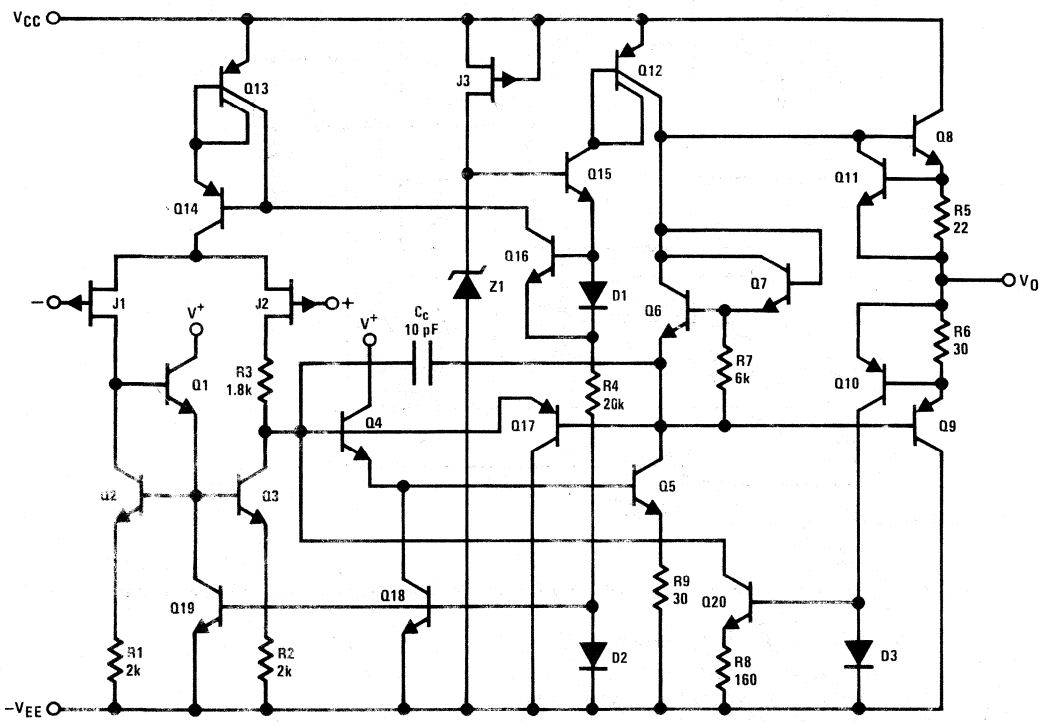
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

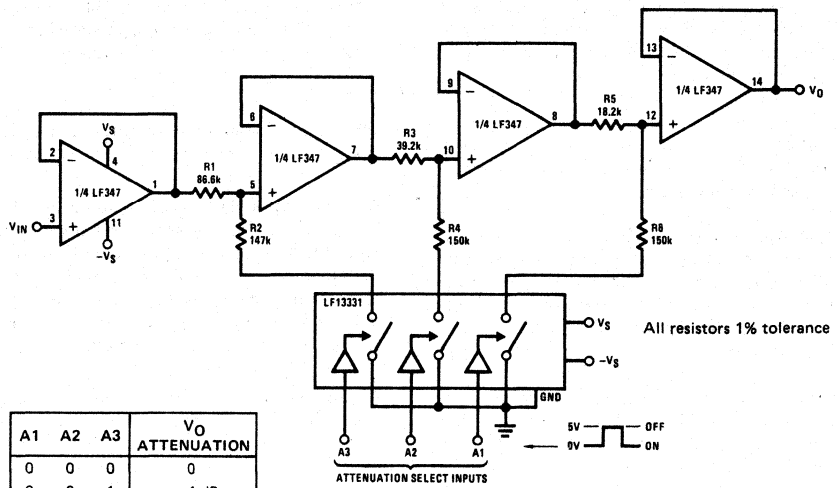
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

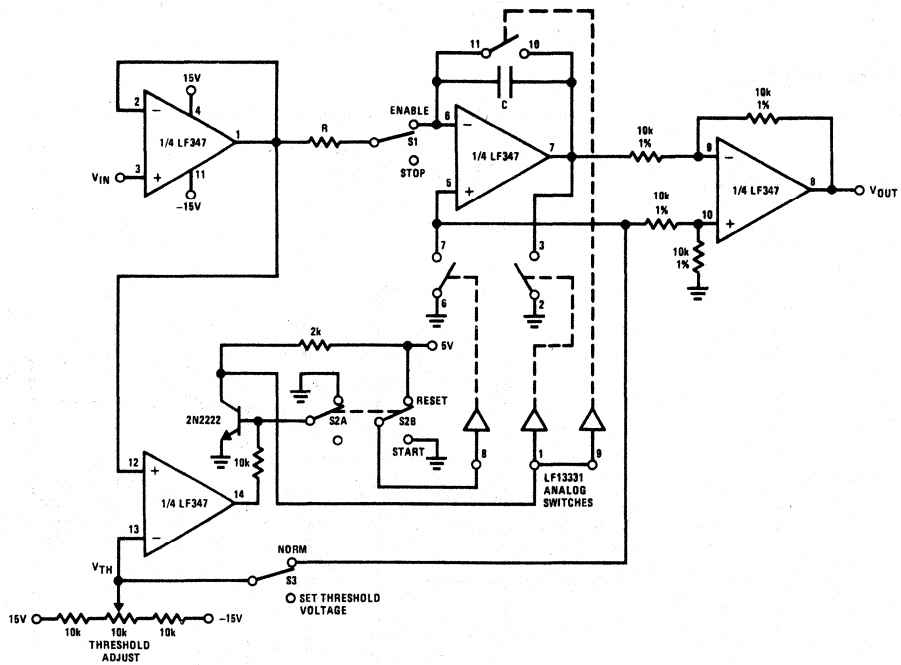
Digitally Selectable Precision Attenuator



A1	A2	A3	V_O ATTENUATION
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



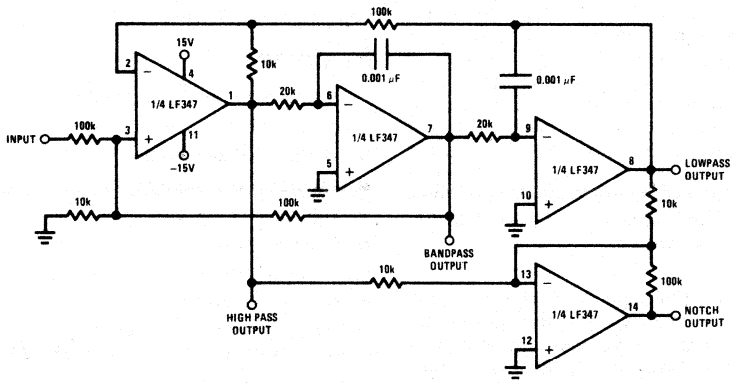
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter

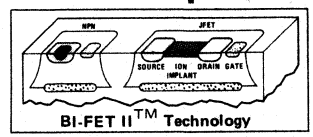


For circuit shown:
f_o = 3 kHz, f_{NOTCH} = 9.5 kHz
Q = 3.4
Passband gain:
Highpass — 0.1
Bandpass — 1
Lowpass — 1
Notch — 10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM348 data sheet for design equations

National Semiconductor

LF351 Wide Bandwidth JFET Input Operational Amplifiers



BI-FET II™ Technology

General Description

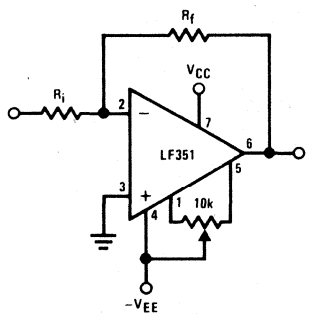
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

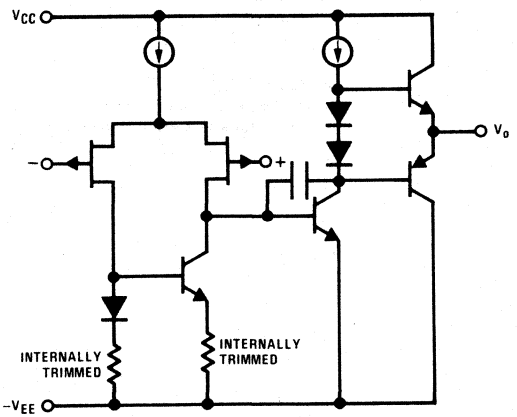
Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/√Hz
- Low input noise current — 0.01 pA/√Hz
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 1.8 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20\,V_{p\text{-}p}$, BW = 20 Hz-20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection

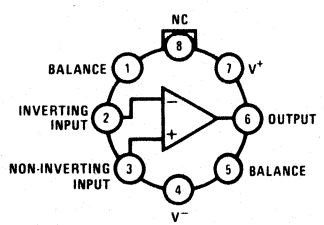


Simplified Schematic



Connection Diagrams (Top Views)

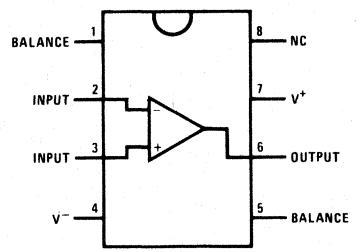
Metal Can Package



Note. Pin 4 connected to case.

Order Number LF351AH, LF351BH or LF351H
See NS Package H08C

Dual-In-Line Package



TOP VIEW

Order Number LF351AN, LF351BN or LF351N
See NS Package N08A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Operating Temperature Range	0°C to +70°C
T_j(MAX)	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351A and LF351A-1			LF351B and LF351B-1			LF351			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10kΩ, T_A = 25°C Over Temperature		1	2 4		3	5 7		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage LF351A-1 LF351B-1	R_S = 10kΩ		10	 20		10	 30		10		µV/°C µV/°C µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		25	100 2		25	100 4		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		50	200 4		50	200 8		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2kΩ Over Temperature	50 25	100		50 25	100		25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		±11	+15 −12		±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	80	100		80	100		70	100		dB
I_S	Supply Current			1.8	2.8		1.8	2.8		1.8	3.4	mA

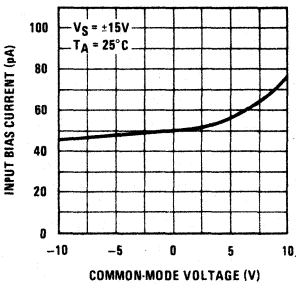
AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351A and LF351A-1			LF351B and LF351B-1			LF351			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate LF351A-1	V_S = ±15V, T_A = 25°C	 10	13			13			13		V/µs V/µs
GBW	Gain Bandwidth Product LF351A-1	V_S = ±15V, T_A = 25°C	 3	4			4			4		MHz MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000Hz		16			16			16		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000Hz		0.01			0.01			0.01		pA/√Hz

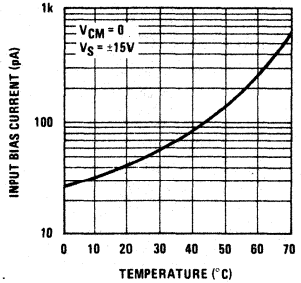
Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.
Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
Note 3: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
Note 5.: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

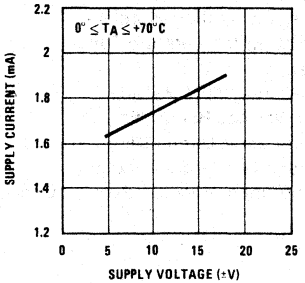
Input Bias Current



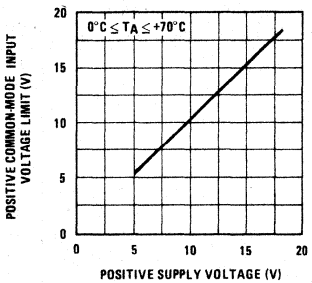
Input Bias Current



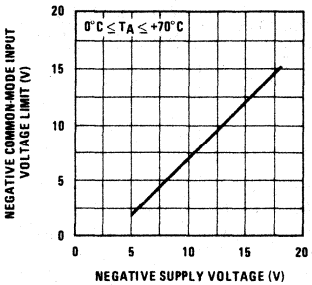
Supply Current



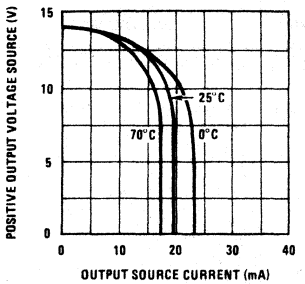
Positive Common-Mode Input Voltage Limit



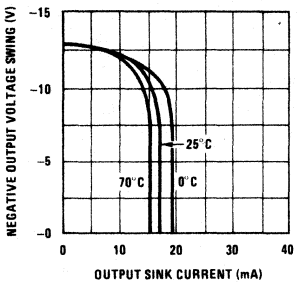
Negative Common-Mode Input Voltage Limit



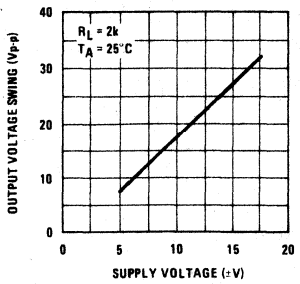
Positive Current Limit



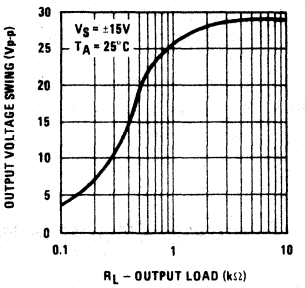
Negative Current Limit



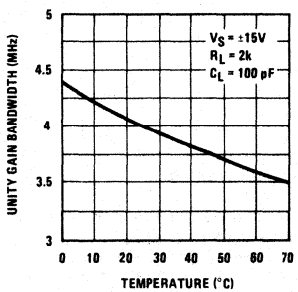
Voltage Swing



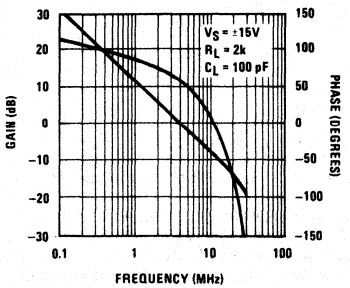
Output Voltage Swing



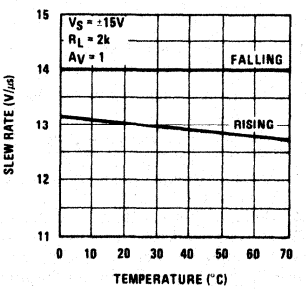
Gain Bandwidth



Bode Plot

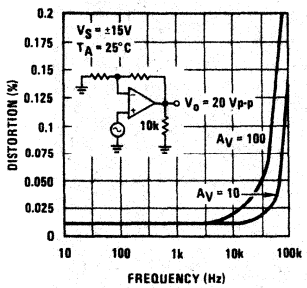


Slew Rate

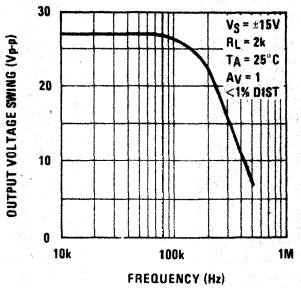


Typical Performance Characteristics (Continued)

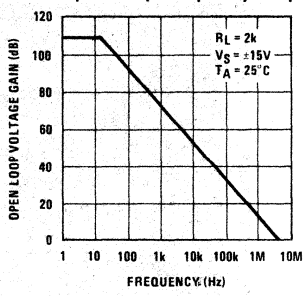
Distortion vs Frequency



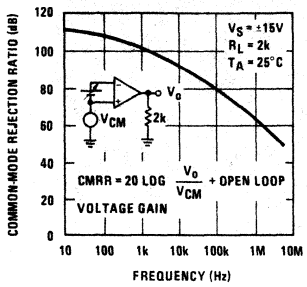
Undistorted Output Voltage Swing



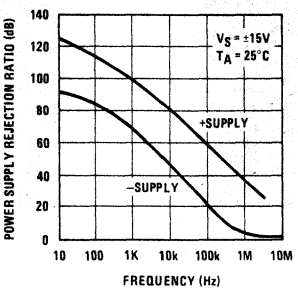
Open Loop Frequency Response



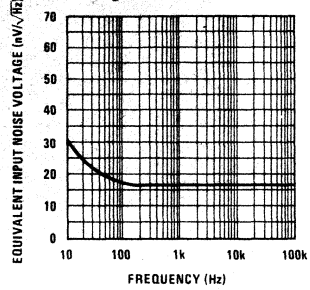
Common-Mode Rejection Ratio



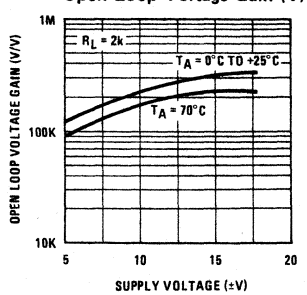
Power Supply Rejection Ratio



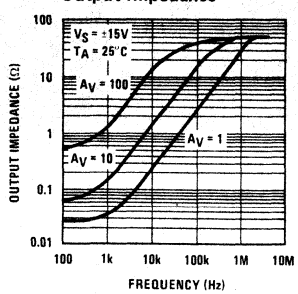
Equivalent Input Noise Voltage



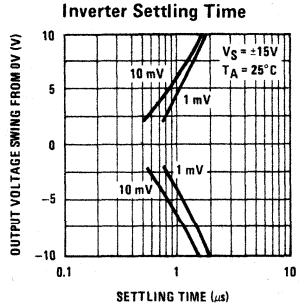
Open Loop Voltage Gain (V/V)



Output Impedance

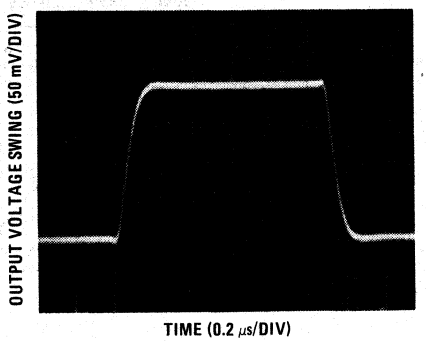


Inverter Settling Time

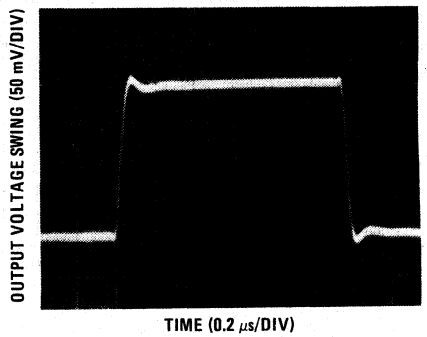


Pulse Response

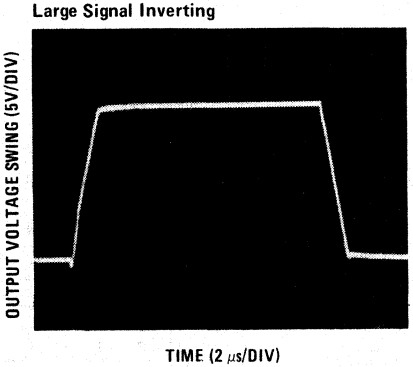
Small Signal Inverting



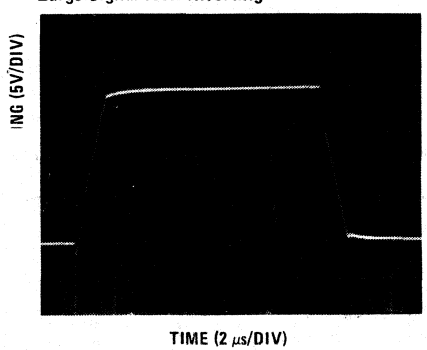
Small Signal Non-Inverting



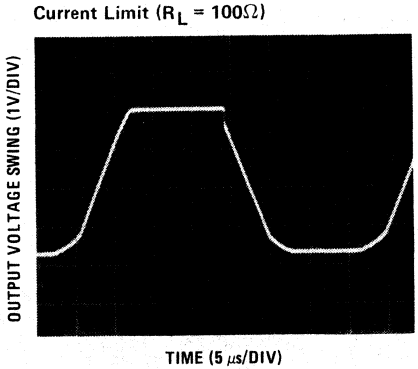
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

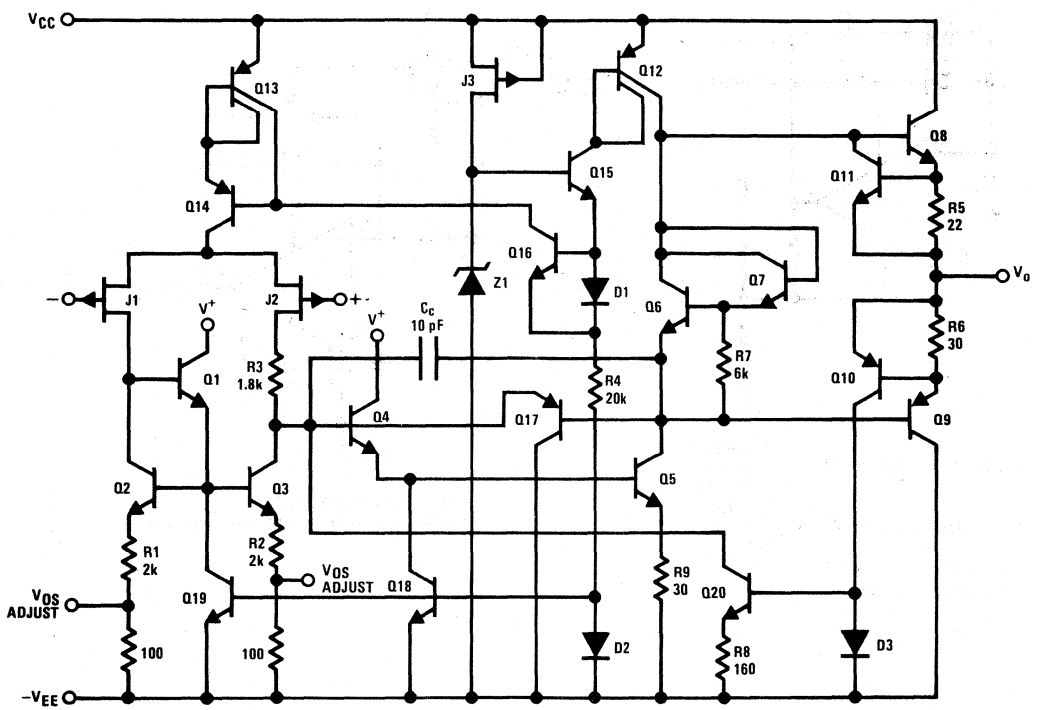
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

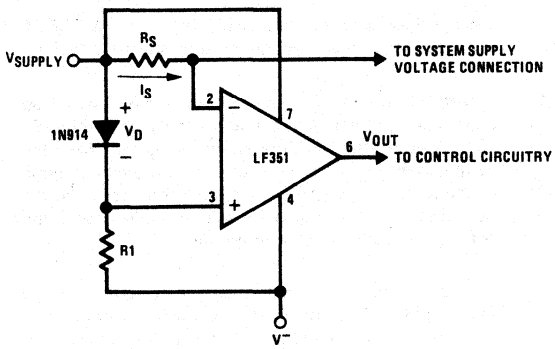
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



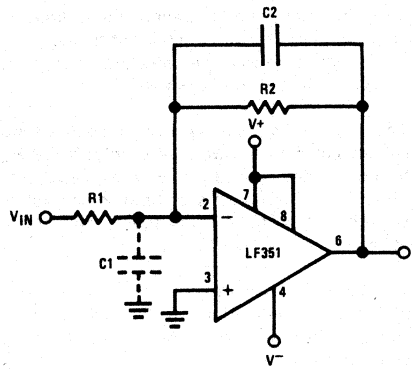
Typical Applications

Supply Current Indicator/Limiter



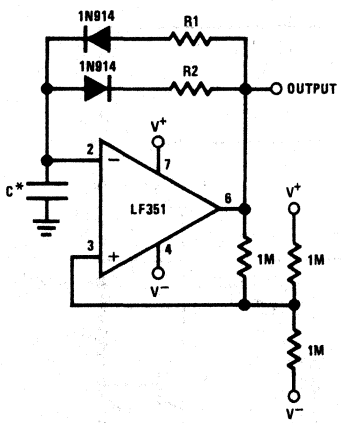
- V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≅ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator

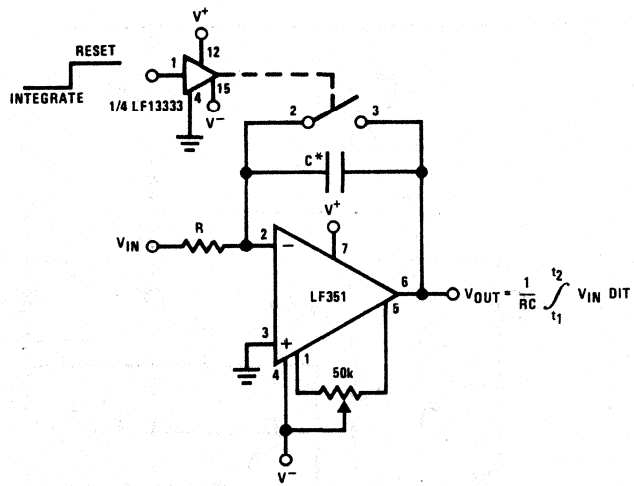


- $t_{OUTPUT\ HIGH} \approx R1C \ln \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C \ln \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator

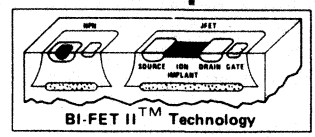


* Low leakage capacitor
- 50k pot used for less sensitive V_{OS} adjust

National Semiconductor

Amplifiers

LF353 Wide Bandwidth Dual JFET Input Operational Amplifiers



General Description

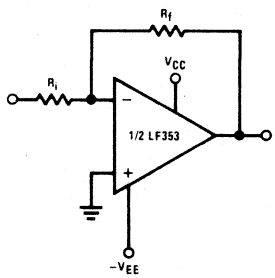
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

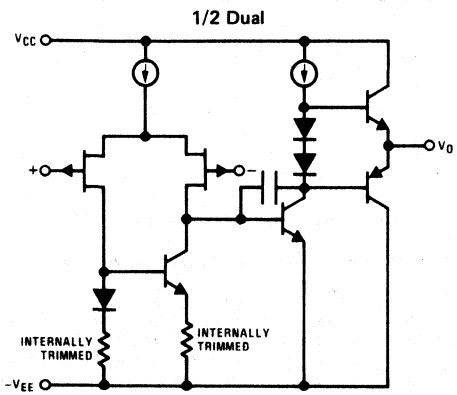
Features

- Internally trimmed offset voltage 2 mV
- Low input bias current 50 pA
- Low input noise voltage 16 nV/√Hz
- Low input noise current 0.01 pA/√Hz
- Wide gain bandwidth 4 MHz
- High slew rate 13 V/μs
- Low supply current 3.6 mA
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20\,Vp-p$, BW = 20 Hz-20 kHz <0.02%
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Typical Connection

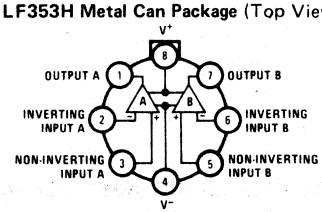


Simplified Schematic



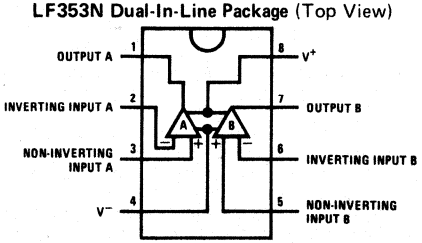
Connection Diagrams

LF353H Metal Can Package (Top View)



Order Number LF353AH, LF353BH or LF353H
See NS Package H08C

LF353N Dual-In-Line Package (Top View)



Order Number LF353AN, LF353BN or LF353N
See NS Package N08A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353A			LF353B and LF353B-1			LF353			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 10k\Omega$, $T_A = 25°C$		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10k\Omega$		10			10			10		µV/°C
	LF351B-1							30				µV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 4, 5)		25	100		25	100		25	100	pA
		$T_j \leq 70°C$			2			4			4	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 4, 5)		50	200		50	200		50	200	pA
		$T_j \leq 70°C$			4			8			8	nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$	50	100		50	100		25	100		V/mV
		$V_O = \pm 10V$, $R_L = 2k\Omega$										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	80	100		80	100		70	100		dB
I_S	Supply Current			3.6	5.6		3.6	5.6		3.6	6.5	mA

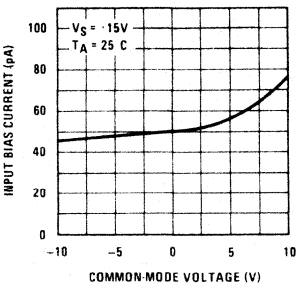
AC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353A			LF353B			LF353			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1Hz–20kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13			13			13		V/µs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000Hz		16			16			16		nV/√Hz
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000Hz		0.01			0.01			0.01		pA/√Hz

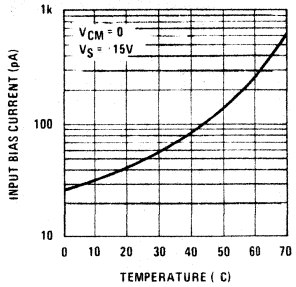
Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 160°C/W junction to ambient for the N package, and 150°C/W junction to ambient for the H package.
Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
Note 3: The power dissipation limit, however, cannot be exceeded.
Note 4: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
Note 6.: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

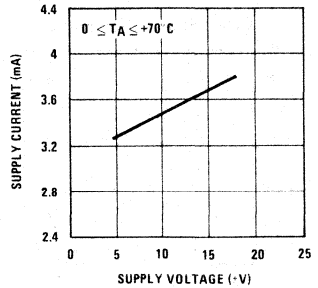
Input Bias Current



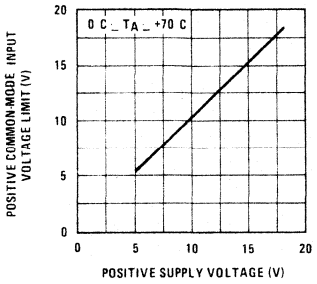
Input Bias Current



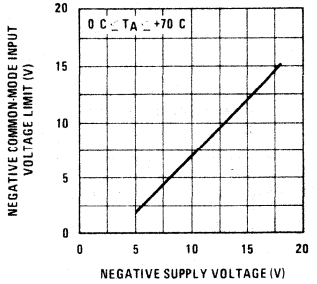
Supply Current



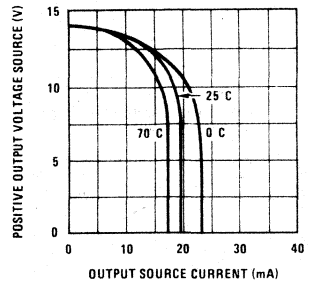
Positive Common-Mode Input Voltage Limit



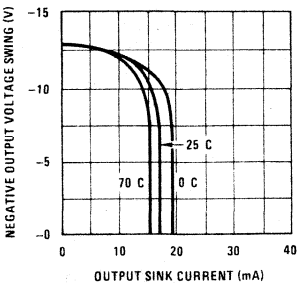
Negative Common-Mode Input Voltage Limit



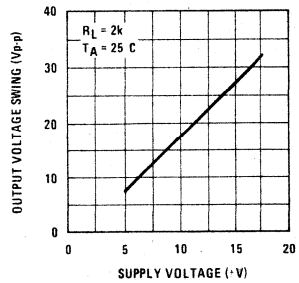
Positive Current Limit



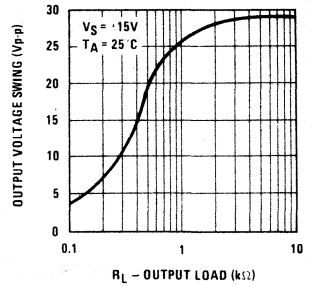
Negative Current Limit



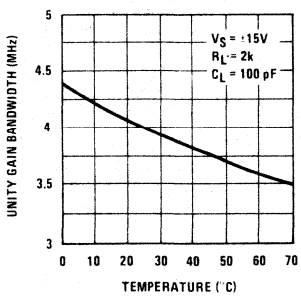
Voltage Swing



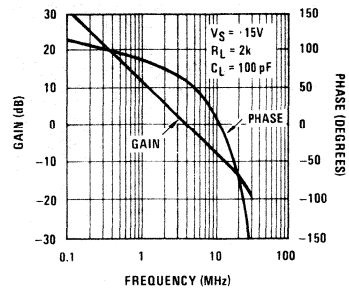
Output Voltage Swing



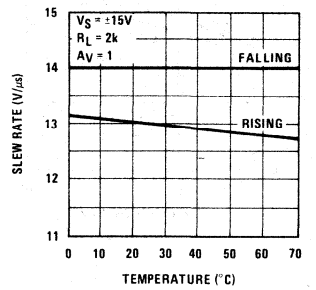
Gain Bandwidth



Bode Plot

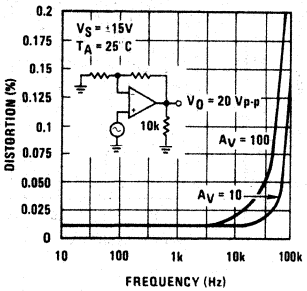


Slew Rate

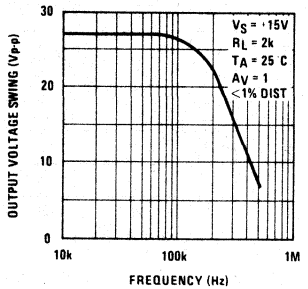


Typical Performance Characteristics (Continued)

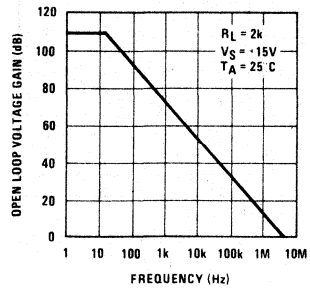
Distortion vs Frequency



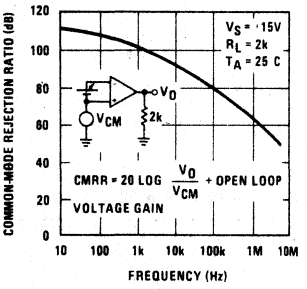
Undistorted Output Voltage Swing



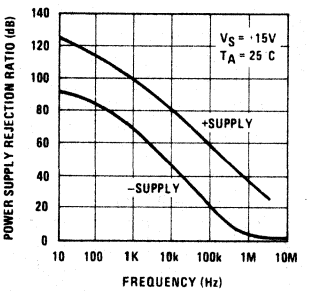
Open Loop Frequency Response



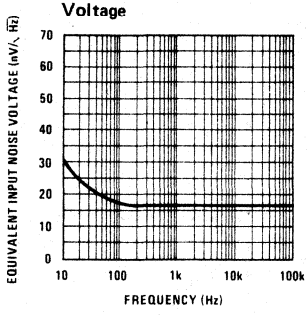
Common-Mode Rejection Ratio



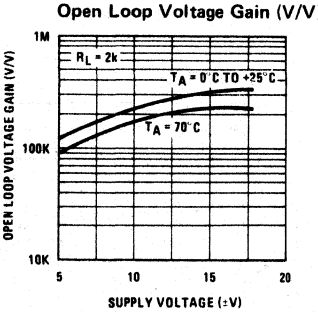
Power Supply Rejection Ratio



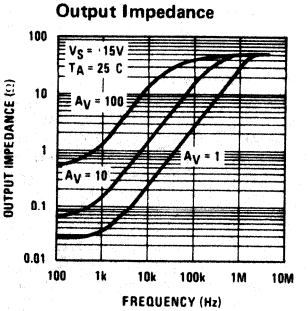
Equivalent Input Noise Voltage



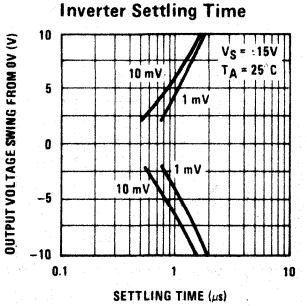
Open Loop Voltage Gain (V/V)



Output Impedance

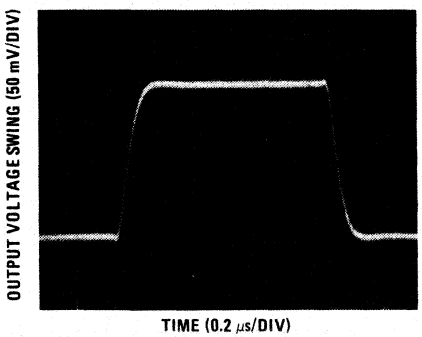


Inverter Settling Time

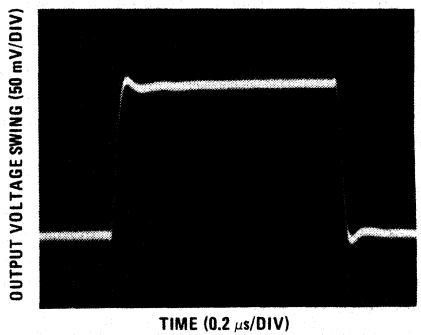


Pulse Response

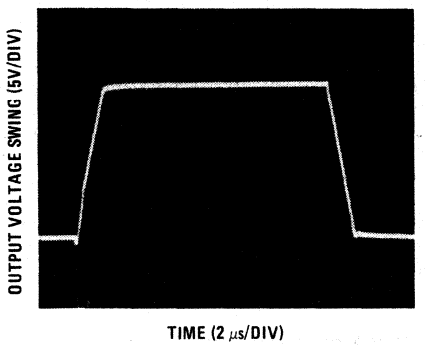
Small Signal Inverting



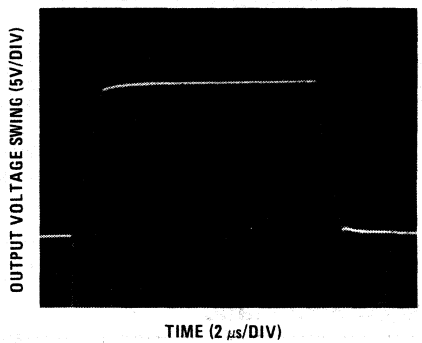
Small Signal Non-Inverting



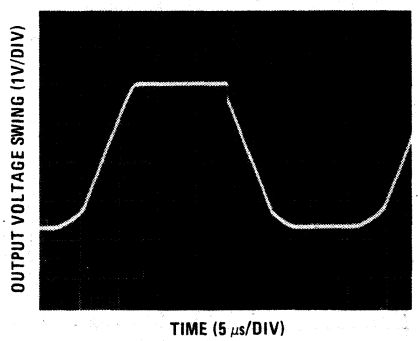
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

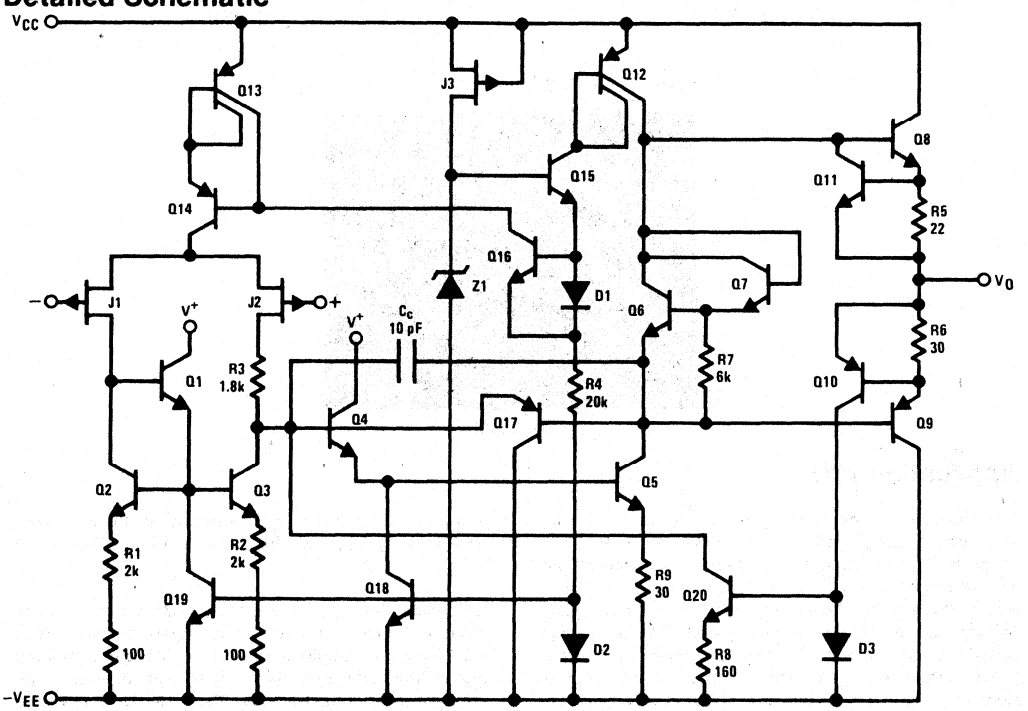
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

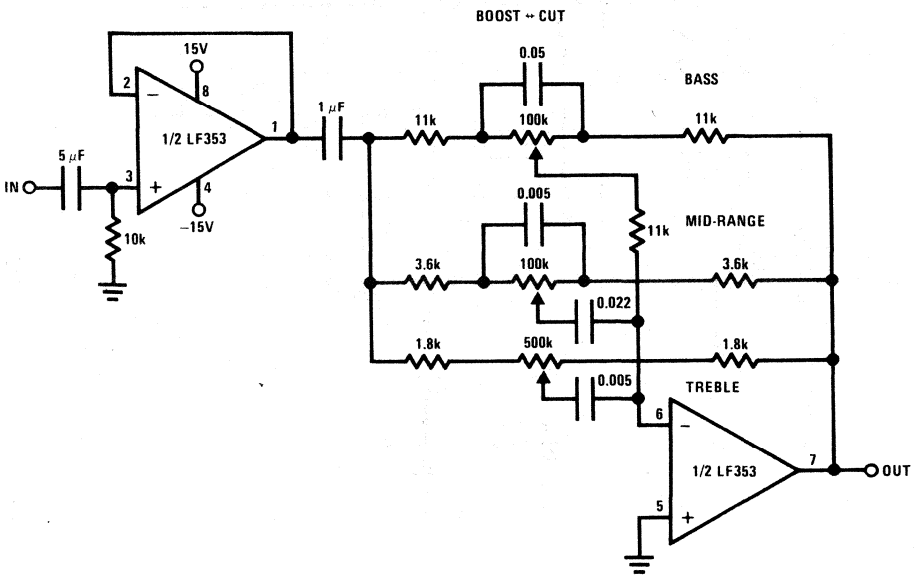
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

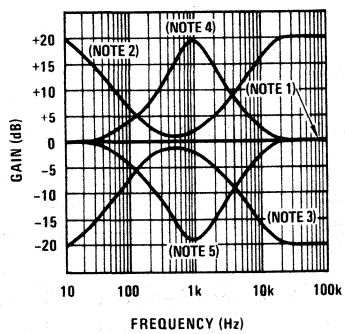
Detailed Schematic



Typical Applications

Three-Band Active Tone Control



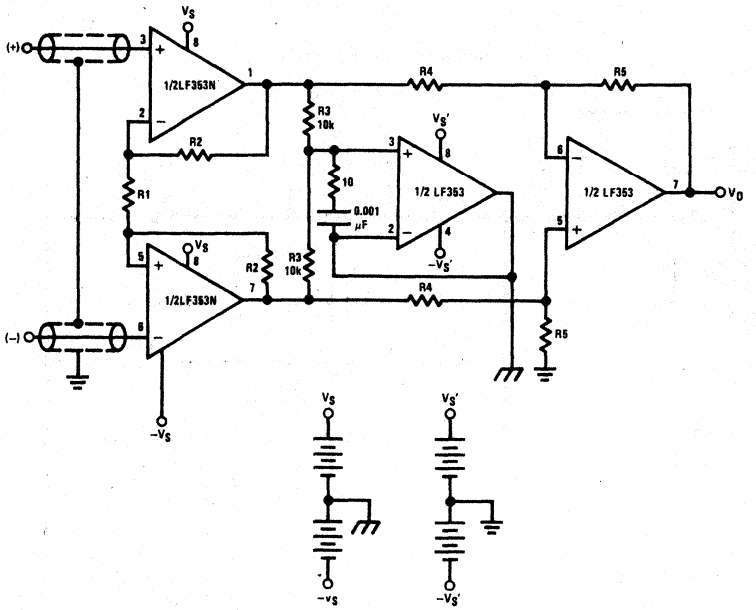


Note 1: All controls flat.
Note 2: Bass and treble boost, mid flat.
Note 3: Bass and treble cut, mid flat.
Note 4: Mid boost, bass and treble flat.
Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



$$A_V = \left(\frac{2R2}{R1} + 1\right) \frac{R5}{R4}$$

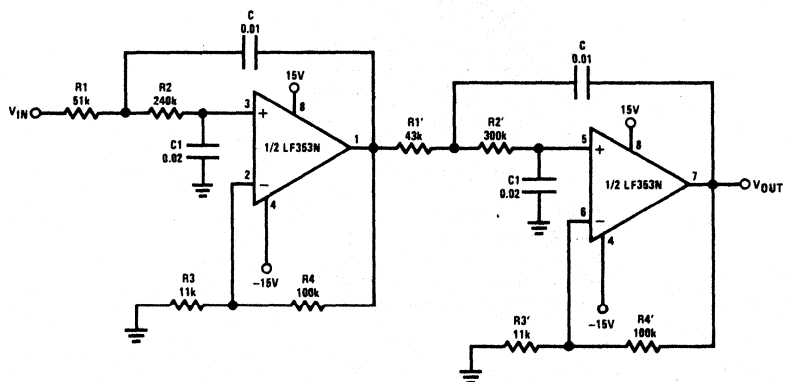
⏚ and ⏚ are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

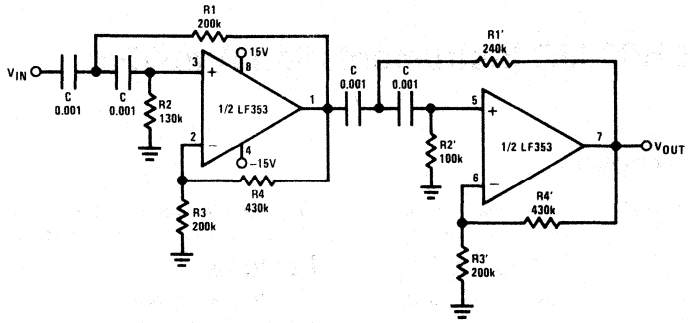
Fourth Order Low Pass Butterworth Filter



- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

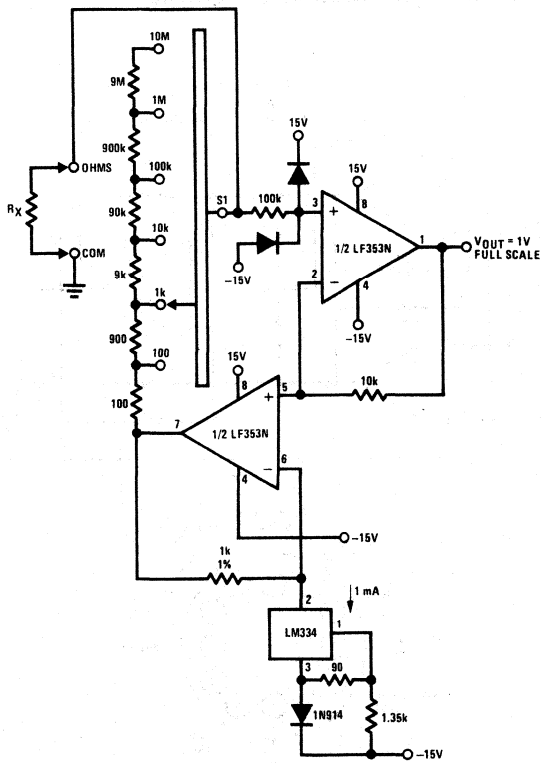
Typical Applications (Continued)

Fourth Order High Pass Butterworth Filter



- Corner frequency $(f_c) = \sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain $(H_O) = (1 + R4/R3)(1 + R4'/R3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter



$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 10 of the LF354.

National Semiconductor

LH0036/LH0036C Instrumentation Amplifier

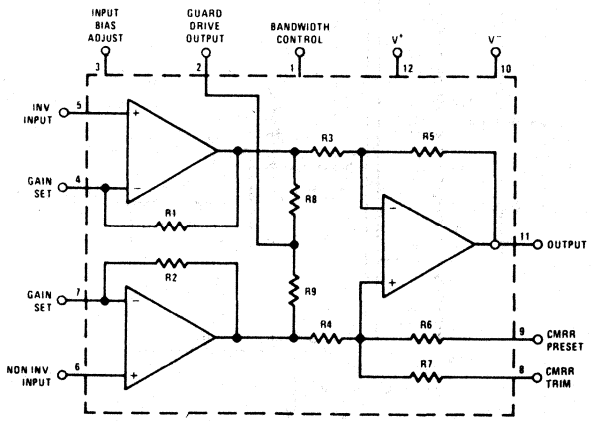
General Description

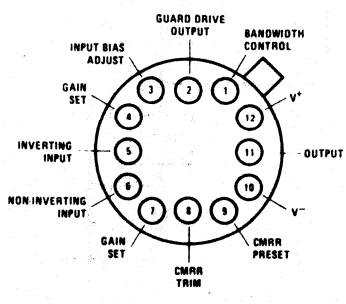
The LH0036/LH0036C is a true micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values. The LH0036 is specified for operation over the −55°C to +125°C temperature range and the LH0036C is specified for operation over the −25°C to +85°C temperature range.

Features

- High input impedance — 300 MΩ
- High CMRR — 100 dB
- Single resistor gain adjust — 1 to 1000
- Low power — 90μW
- Wide supply range — ±1V to ±18V
- Adjustable input bias current
- Adjustable output bandwidth
- Guard drive output

Equivalent Circuits and Connection Diagrams





TOP VIEW

Order Number LH0036G or LH0036CG
See NS Package H12B

Absolute Maximum Ratings

Supply Voltage	±18V	Short Circuit Duration	Continuous
Differential Input Voltage	±30V	Operating Temperature Range	
Input Voltage Range	$\pm V_S$	LH0036	−55°C to +125°C
Shield Drive Voltage	$\pm V_S$	LH0036C	−25°C to +85°C
CMRR Preset Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
CMRR Trim Voltage	$\pm V_S$	Lead Temperature, Soldering 10 seconds	300°C
Power Dissipation (Note 3)	1.5W		

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0036			LH0036C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{IOS})	R_S = 1.0kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
	R_S = 1.0kΩ			2.0			3.0	mV
Output Offset Voltage (V_{OOS})	R_S = 1.0kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
	R_S = 1.0kΩ			6.0			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0kΩ		10			10		µV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15			15		µV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		2.5			6.0		mV
	A_V = 10		0.7			1.5		mV
	A_V = 100		0.52			1.05		mV
	A_V = 1000		0.502			1.005		mV
Input Bias Current (I_B)	T_A = 25°C		40	100		50	125	nA
				150			200	nA
Input Offset Current (I_{OS})	T_A = 25°C		10	40		20	50	nA
				80			100	nA
Small Signal Bandwidth	A_V = 1.0, R_L = 10kΩ		350			350		kHz
	A_V = 10, R_L = 10kΩ		35			35		kHz
	A_V = 100, R_L = 10kΩ		3.5			3.5		kHz
	A_V = 1000, R_L = 10kΩ		350			350		Hz
Full Power Bandwidth	V_{IN} = ±10V, R_L = 10k, A_V = 1		5.0			5.0		kHz
Input Voltage Range	Differential	±10	±12		±10	±12		V
	Common Mode	±10	±12		±10	±12		V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000		±0.3	±1.0		±1.0	±3.0	%
PSRR	±5.0V ≤ V_S ≤ ±15V, A_V = 1.0		1.0	2.5		1.0	5.0	mV/V
	±5.0V ≤ V_S ≤ ±15V, A_V = 100		0.05	0.25		0.10	0.50	mV/V
CMRR	A_V = 1.0 DC to		1.0	2.5		2.5	5.0	mV/V
	A_V = 10 100 Hz		0.1	0.25		0.25	0.50	mV/V
	A_V = 100 ΔR_S = 1.0k		50	100		50	100	µV/V
Output Voltage	V_S = ±15V, R_L = 10kΩ,	±10	±13.5		±10	±13.5		V
	V_S = ±1.5V, R_L = 100kΩ	±0.6	±0.8		±0.6	±0.8		V
Output Resistance			0.5			0.5		Ω
Supply Current			300	400		400	600	µA
Equivalent Input Noise Voltage	0.1 Hz < f < 10 kHz, R_S < 50 Ω		20			20		µV/p-p
Slew Rate	ΔV_{IN} = ±10V, R_L = 10kΩ, A_V = 1.0		0.3			0.3		V/µs
Settling Time	To ±10 mV, R_L = 10kΩ, ΔV_{OUT} = 1.0V							
	A_V = 1.0		3.8			3.8		µs
	A_V = 100		180			180		µs

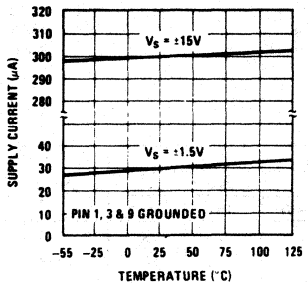
Note 1: Unless otherwise specified, all specifications apply for V_S = ±15V, Pins 1, 3, and 9 grounded, −25°C to +85°C for the LH0036C and −55°C to +125°C for the LH0036.

Note 2: All typical values are for T_A = 25°C.

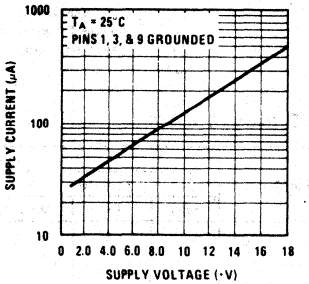
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

Typical Performance Characteristics

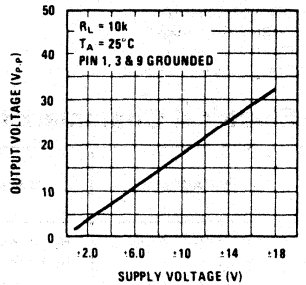
Supply Current vs Temperature



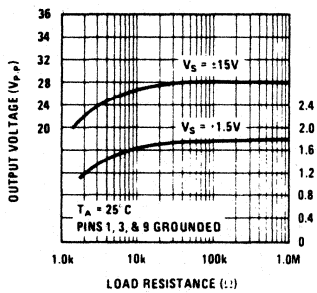
Supply Current vs Supply Voltage



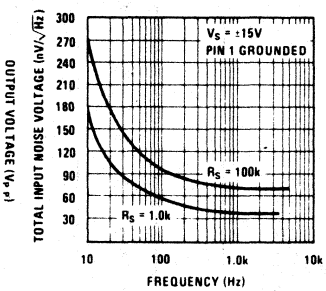
Output Voltage Swing vs Supply Voltage



Peak to Peak Output Voltage Swing vs R_L

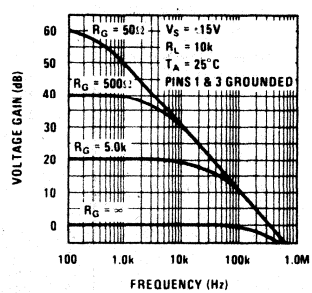


Total Input Noise Voltage* vs Frequency

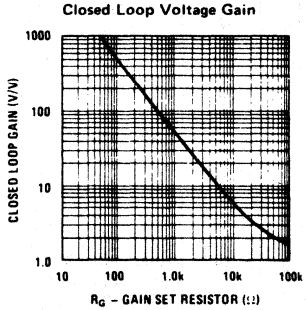


*Noise voltage includes contribution from source resistance

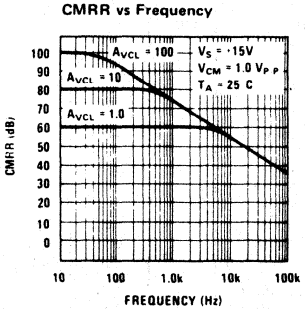
Closed Loop Voltage Gain vs Frequency



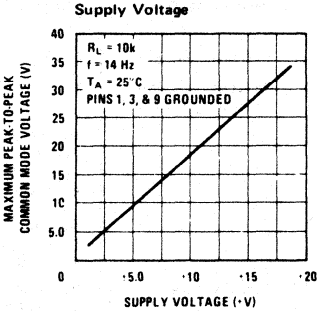
Closed Loop Voltage Gain



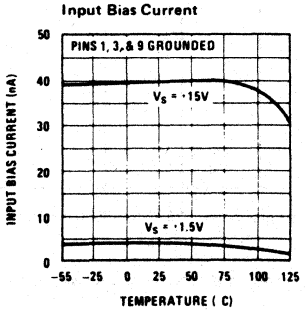
CMRR vs Frequency



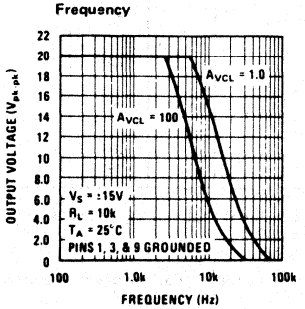
Common Mode Voltage vs Supply Voltage



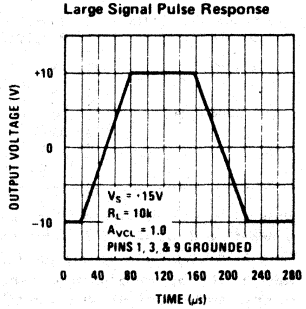
Input Bias Current



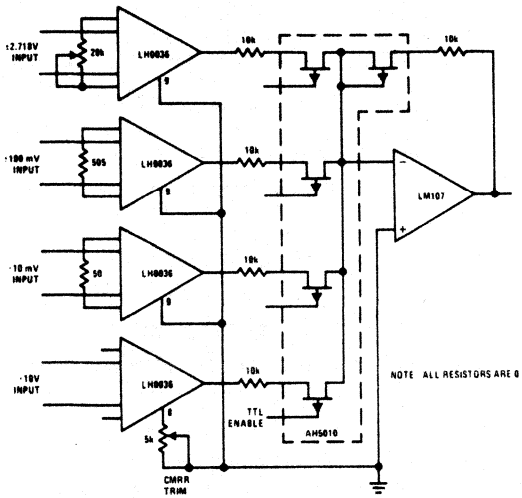
Output Voltage Swing vs Frequency



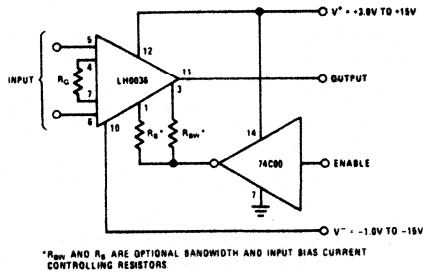
Large Signal Pulse Response



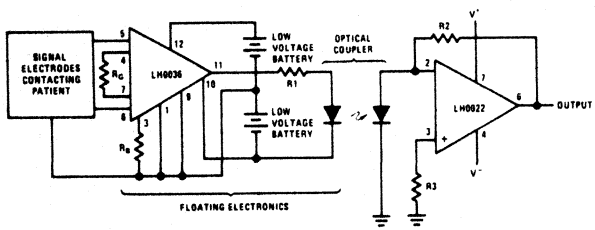
Typical Applications



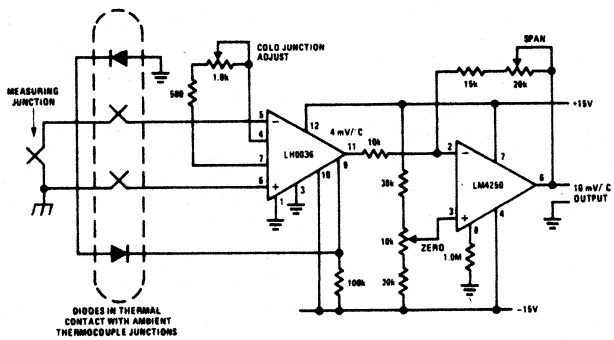
Pre MUX Signal Conditioning



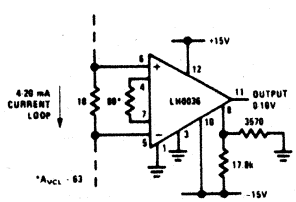
Instrumentation Amplifier with Logic Controlled Shut-Down



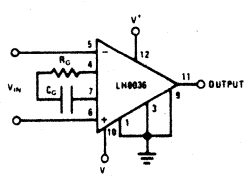
Isolation Amplifier for Medical Telemetry



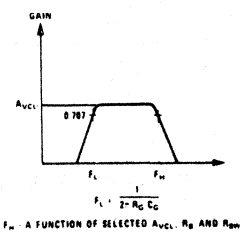
Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface



High Pass Filter



FH = A FUNCTION OF SELECTED AVCL, RG AND RBW

Applications Information

THEORY OF OPERATION

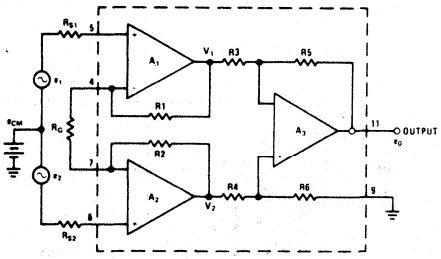


FIGURE 1. Simplified LH0036

The LH0036 is a 2 stage amplifier with a high input impedance gain stage comprised of A_1 and A_2 and a differential to single-ended unity gain stage, A_3. Operational amplifier, A_1, receives differential input signal, e_1, and amplifies it by a factor equal to $(R1 + R_G)/R_G$.

A_1 also receives input e_2 via A_2 and R2. e_2 is seen as an inverting signal with a gain of $R1/R_G$. A_1 also receives the common mode signal e_{CM} and processes it with a gain of +1.

Hence:

$$V_1 = \frac{R1 + R_G}{R_G} e_1 - \frac{R1}{R_G} e_2 + e_{CM} \quad (1)$$

By similar analysis V_2 is seen to be:

$$V_2 = \frac{R2 + R_G}{R_G} e_2 - \frac{R2}{R_G} e_1 + e_{CM} \quad (2)$$

For R1 = R2:

$$V_2 - V_1 = \left[\left(\frac{2R1}{R_G}\right) + 1\right](e_2 - e_1) \quad (3)$$

Also, for R3 = R5 = R4 = R6, the gain of $A_3 = 1$, and:

$$e_0 = (1)(V_2 - V_1) = (e_2 - e_1)\left[1 + \left(\frac{2R1}{R_G}\right)\right] \quad (4)$$

As can be seen for identically matched resistors, e_{CM} is cancelled out, and the differential gain is dictated by equation (4).

For the LH0036, equation (4) reduces to:

$$A_{VCL} = \frac{e_0}{e_2 - e_1} = 1 + \frac{50k}{R_G} \quad (5a)$$

The closed loop gain may be set to any value from 1 ($R_G = \infty$) to 1000 ($R_G \cong 50\Omega$). Equation (5a) re-arranged in more convenient form may be used to select R_G for a desired gain:

$$R_G = \frac{50k}{A_{VCL} - 1} \quad (5b)$$

USE OF BANDWIDTH CONTROL (pin 1)

In the standard configuration, pin 1 of the LH0036 is simply grounded. The amplifier's slew rate in this configuration is typically 0.3V/μs and small signal bandwidth 350 kHz for $A_{VCL} = 1$. In some applications, particularly at low frequency, it may be desirable to limit bandwidth in order to minimize the overall noise bandwidth of the device. A resistor R_{BW} may be placed between pin 1 and ground to accomplish this purpose. Figure 2 shows typical small signal bandwidth versus R_{BW}.

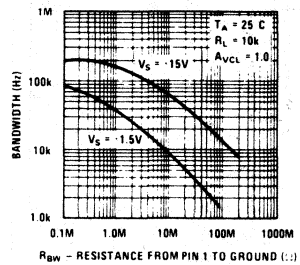


FIGURE 2. Bandwidth vs R_{BW}

It also should be noted that large signal bandwidth and slew rate may be adjusted down by use of R_{BW}. Figure 3 is plot of slew rate versus R_{BW}.

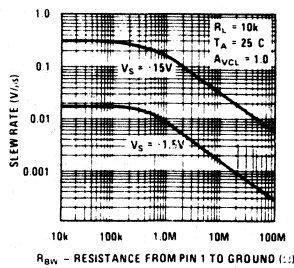


FIGURE 3. Output Slew Rate vs R_{BW}

CMRR CONSIDERATIONS

Use of Pin 9, CMRR Preset

Pin 9 should be grounded for nominal operation. An internal factory trimmed resistor, R6, will yield a CMRR in excess of 80 dB (for $A_{VCL} = 100$). Should a higher CMRR be desired, pin 9 should be left open and the procedure, in this section followed.

DC Off-set Voltage and Common Mode Rejection Adjustments

Off-set may be nulled using the circuit shown in Figure 4.

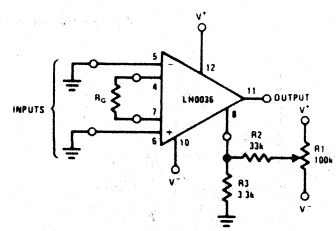


FIGURE 4. V_{OS} Adjustment Circuit

Pin 8 is also used to improve the common mode rejection ratio as shown in Figure 5. Null is

Applications Information (Continued)

achieved by alternately applying ±10V (for V^+ & V^- = 15V) to the inputs and adjusting R1 for minimum change at the output.

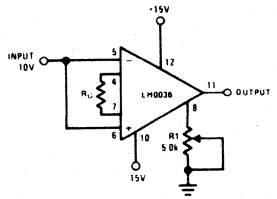


FIGURE 5. CMRR Adjustment Circuit

The circuits of Figure 4 and 5 may be combined as shown in Figure 6 to accomplish both V_{OS} and CMRR null. However, the V_{OS} and CMRR adjustment are interactive and several iterations are required. The procedure for null should start with the inputs grounded.

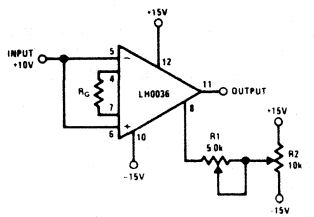


FIGURE 6. Combined CMRR, V_{OS} Adjustment Circuit

R2 is adjusted for V_{OS} null. An input of +10V is then applied and R1 is adjusted for CMRR null. The procedure is then repeated until the optimum is achieved.

A circuit which overcomes adjustment interaction is shown in Figure 7. In this case, R2 is adjusted first for output null of the LH0036. R1 is then adjusted for output null with +10V input. It is always a good idea to check CMRR null with a −10V input. The optimum null achievable will yield the highest CMRR over the amplifiers common mode range.

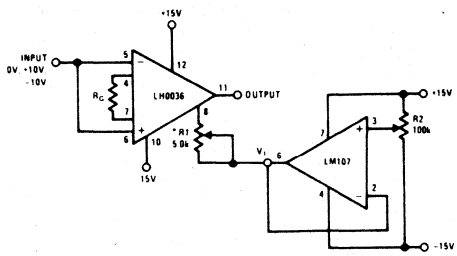


FIGURE 7. Improved V_{OS}, CMRR Nulling Circuit

AC CMRR Considerations

The ac CMRR may be improved using the circuit of Figure 8.

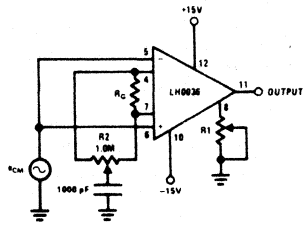


FIGURE 8. Improved AC CMRR Circuit

After adjusting R1 for best dc CMRR as before, R2 should be adjusted for minimum peak-to-peak voltage at the output while applying an ac common mode signal of the maximum amplitude and frequency of interest.

INPUT BIAS CURRENT CONTROL

Under nominal operating conditions (pin 3 grounded), the LH0036 requires input currents of 40 nA. The input current may be reduced by inserting a resistor (R_B) between 3 and ground or, alternatively, between 3 and V^-. For R_B returned to ground, the input bias current may be predicted by:

$$I_{BIAS} \cong \frac{V^+ - 0.5}{4 \times 10^8 + 800\ R_B} \qquad (6a)$$

or

$$R_B = \frac{V^+ - 0\,5 - (4 \times 10^8)\ (I_{BIAS})}{800\ I_{BIAS}} \qquad (6b)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External Resistor connected between pin 3 and ground (Ohms)

V^+ = Positive Supply Voltage (Volts)

Figure 9 is a plot of input bias current versus R_B.

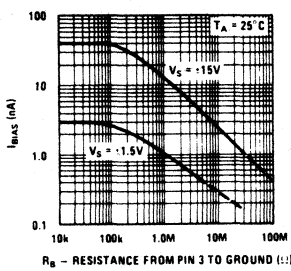


FIGURE 9. Input Bias Current as a Function of R_B

As indicated above, R_B may be returned to the negative supply voltage. Input bias current may then be predicted by:

$$I_{BIAS} \cong \frac{(V^+ - V^-) - 0.5}{4 \times 10^8 + 800\ R_B}$$

Applications Information (Continued)

or

$$R_B \cong \frac{(V^+ - V^-) - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\ I_{BIAS}} \quad (8)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External resistor connected between pin 3 and V^- (Ohms)

V^+ = Positive Supply Voltage (Volts)

V^- = Negative Supply Voltage (Volts)

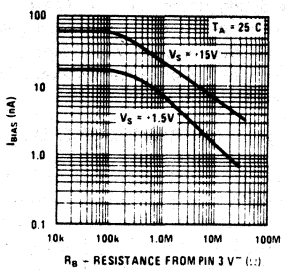


FIGURE 10. Input Bias Current as a Function of R_B

Figure 10 is a plot of input bias current versus R_B returned to V^- it should be noted that bandwidth is affected by changes in R_B. Figure 11 is a plot of bandwidth versus R_B.

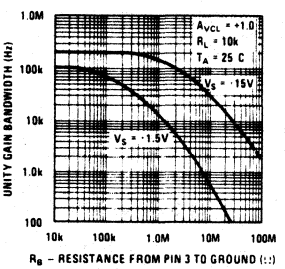


FIGURE 11. Unity Gain Bandwidth as a Function of R_B

BIAS CURRENT RETURN PATH CONSIDERATIONS

The LH0036 exhibits input bias currents typically in the 40 nA region in each input. This current must flow through R_{ISO} as shown in Figure 12.

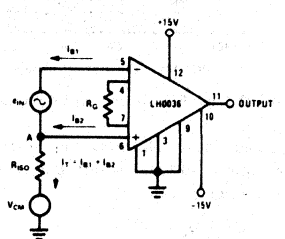


FIGURE 12. Bias Current Return Path

In a typical application, V_S = ±15V, $I_{B1} \cong I_{B2} \cong$ 40 nA, the total current, I_T, would flow through R_{ISO} causing a voltage rise at point A. For values of $R_{ISO} \geq 150$ MΩ, the voltage at point A exceeds the +12V common range of the device. Clearly, for $R_{ISO} = \infty$, the LH0036 would be driven to positive saturation.

The implication is that a finite impedance must be supplied between the input and power supply ground. The value of the resistor is dictated by the maximum input bias current, and the common mode voltage. Under worst case conditions:

$$R_{ISO} \leq \frac{V_{CMR} - V_{CM}}{I_T} \quad (9)$$

Where:

V_{CMR} = Common Mode Range (10V for the LH0036)

V_{CM} = Common Mode Voltage

$I_T = I_{B1} + I_{B2}$

In applications in which the signal source is floating, such as a thermocouple, one end of the source may be grounded directly or through a resistor.

GUARD OUTPUT

Pin 2 of the LH0036 is provided as a guard drive pin in those stringent applications which require very low leakage and minimum input capacitance. Pin 2 will always be biased at the input common mode voltage. The source impedance looking into pin 2 is approximately 15 kΩ. Proper use of the guard/shield pin is shown in Figure 13.

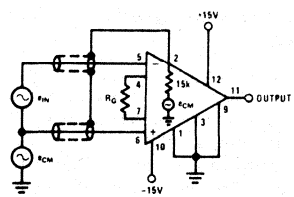


FIGURE 13. Use of Guard

For applications requiring a lower source impedance than 15 kΩ, a unity gain buffer, such as the LH0002 may be inserted between pin 2 and the input shields as shown in Figure 14.

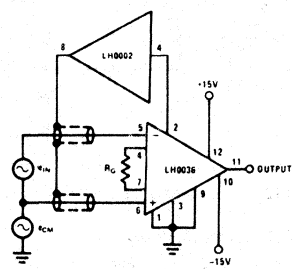


FIGURE 14. Guard Pin With Buffer

Definition of Terms

Bandwidth: The frequency at which the voltage gain is reduced to 0.707 of the low frequency (dc) value.

Closed Loop Gain, A_{VCL}: The ratio of the output voltage swing to the input voltage swing determined by $A_{VCL} = 1 + (50k/R_G)$. Where: R_G = Gain Set Resistor.

Common Mode Rejection Ratio: The ratio of input voltage range to the peak-to-peak change in offset voltage over this range.

Gain Equation Accuracy: The deviation of the actual closed loop gain from the predicted closed loop gain, $A_{VCL} = 1 + (50k/R_G)$ for the specified closed loop gain.

Input Bias Current: The current flowing at pin 5 and 6 under the specified operating conditions.

Input Offset Current: The difference between the input bias current at pins 5 and 6; i.e. $I_{OS} = |I_5 - I_6|$.

Input Stage Offset Voltage, V_{IOS}: The voltage which must be applied to the input pins to force the output to zero volts for $A_{VCL} = 100$.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage to produce zero output voltage. It can be measured by measuring the overall offset at unity gain and subtracting V_{IOS}.

$$V_{OOS} = \left[V_{OS}\Big|_{A_{VCL}=1}\right] - \left[V_{OS}\Big|_{A_{VCL}=1000}\right]$$

Overall Offset Voltage:

$$V_{OS} = V_{IOS} + \frac{V_{OOS}}{A_{VCL}}$$

Power Supply Rejection Ratio: The ratio of the change in offset voltage, V_{OS}, to the change in supply voltage producing it.

Resistor, R_B: An optional resistor placed between pin 3 of the LH0036 and ground (or V^-) to reduce the input bias current.

Resistor, R_{BW}: An optional resistor placed between pin 1 of the LH0036 and ground (or V^-) to reduce the bandwidth of the output stage.

Resistor, R_G: A gain setting resistor connected between pins 4 and 7 of the LH0036 in order to program the gain from 1 to 1000.

Settling Time: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

National Semiconductor

LH0037/LH0037C Low Cost Instrumentation Amplifier

General Description

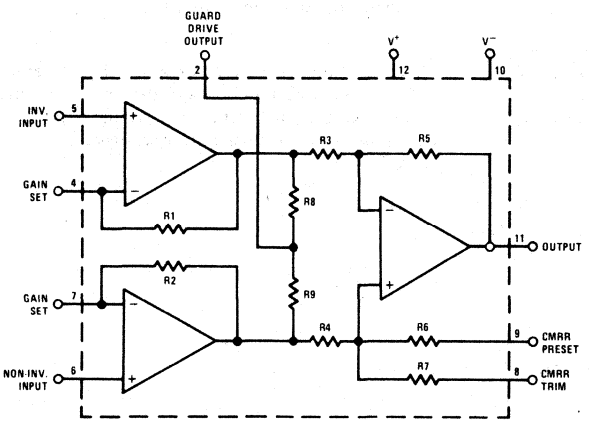
The LH0037/LH0037C is a true instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common-mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±5V and ±22V.

The LH0037 is specified for operation over the −55°C to +125°C temperature range and the LH0037C is specified for operation over the −25°C to +85°C temperature range.

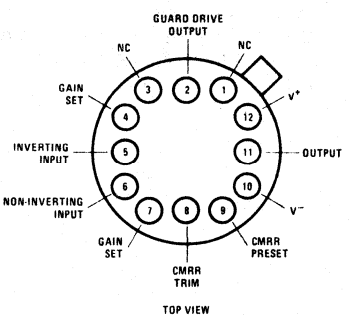
Features

- High input impedance — 300 MΩ
- High CMRR — 100 dB
- Single resistor gain adjust — 1 to 1000
- Low power — 250 mW
- Wide supply range — ±5V to ±22V
- Guard drive output

Equivalent Circuit and Connection Diagrams

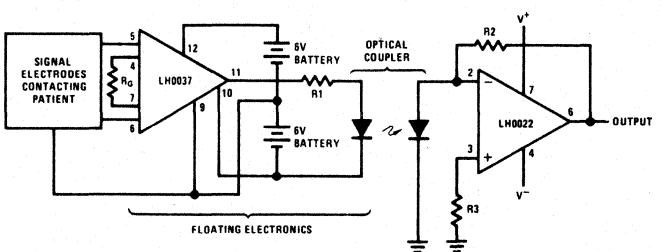


Metal Can Package



Order Number LH0037G or LH0037CG
See Package H12B

Typical Applications



Isolation Amplifier for Medical Telemetry

Absolute Maximum Ratings

Supply Voltage	±22V	Short Circuit Duration	Continuous
Differential Input Voltage	±30V	Operating Temperature Range	
Input Voltage Range	$\pm V_S$	LH0037	−55°C to +125°C
Shield Drive Voltage	$\pm V_S$	LH0037C	−25°C to +85°C
CMRR Preset Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
CMRR Trim Voltage	$\pm V_S$	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (Note 3)	1.5W		

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0037			LH0037C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{IOS})	R_S = 1.0 kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
	R_S = 1.0 kΩ			2.0			3.0	mV
Output Offset Voltage (V_{OOS})	R_S = 1.0 kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
	R_S = 1.0 kΩ			6.0			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0 kΩ		10			10		µV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15			15		µV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		2.5			6.0		mV
	A_V = 10		0.7			1.5		mV
	A_V = 100		0.52			1.05		mV
	A_V = 1000		0.502			1.005		mV
Input Bias Current (I_B)	T_A = 25°C		200	500		200	500	nA
				1.5			0.8	µA
Input Offset Current (I_{OS})	T_A = 25°C			100			250	nA
				200			250	
Small Signal Bandwidth	A_V = 1.0, R_L = 2 kΩ		350			350		kHz
	A_V = 10, R_L = 2 kΩ		35			35		kHz
	A_V = 100, R_L = 2 kΩ		3.5			3.5		kHz
	A_V = 1000, R_L = 2 kΩ		350			350		Hz
Full Power Bandwidth	V_{IN} = ±10V, R_L = 2 kΩ A_V = 1		5.0			5.0		kHz
Input Voltage Range	Differential	±12			±12			V
	Common Mode	±12			±12			V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000		±0.3	±1		±1.0	±3	%
PSRR	±5.0V ≤ V_S ≤ ±15V, A_V = 1.0		1.0	2.5		1.0	5	mV/V
	±5.0V < V_S < ±15V, A_V = 100		0.05	0.25		0.10	0.25	mV/V
CMRR	A_V = 1.0 DC to		1.0	2.5		2.5	5.0	mV/V
	A_V = 10 100 Hz		0.1	0.25		0.25	1.0	mV/V
	A_V = 100 ΔR_S = 1.0k		25	100		25	100	µV/V
Output Voltage	R_L = 2 kΩ	10	13		10	13		V
Output Resistance			0.5			0.5		Ω
Supply Current			4.5	8.4		4.5	8.4	mA
Slew Rate	ΔV_{IN} = ±10V, R_L = 2 kΩ, A_V = 1.0		0.5			0.5		V/µs
Settling Time	To ±10 mV, R_L = 2 kΩ ΔV_{OUT} = 1.0V							
	A_V = 1.0		3.8			3.8		µs
	A_V = 100		180			180		µs

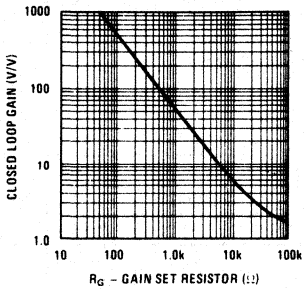
Note 1: Unless otherwise specified, all specifications apply for V_S = ±15V, pin 9 grounded, −25°C to +85°C for the LH0037C and −55°C to +125°C for the LH0037.

Note 2: All typical values are for T_A = 25°C.

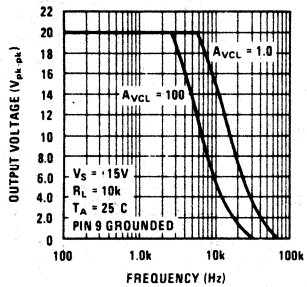
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

Typical Performance Characteristics

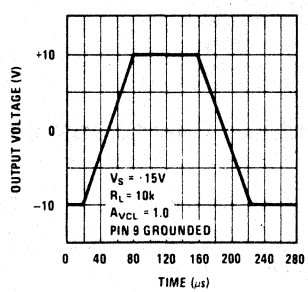
Closed Loop Voltage Gain



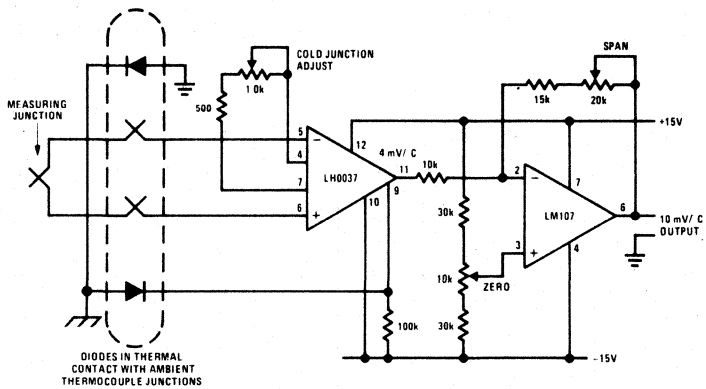
Output Voltage Swing vs Frequency



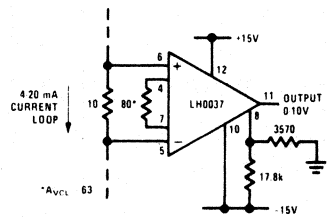
Large Signal Pulse Response



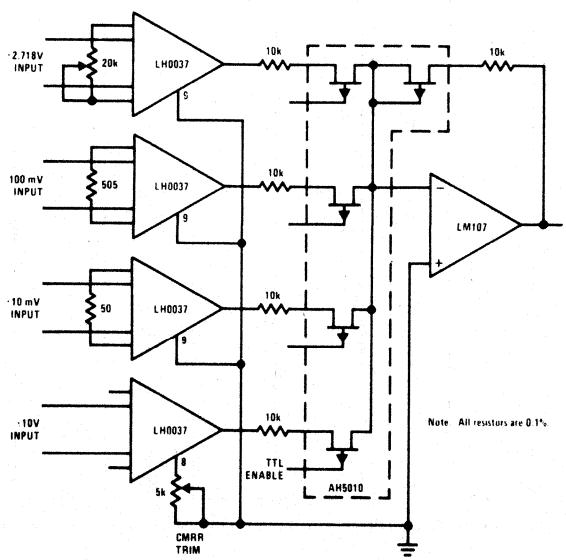
Typical Applications (Continued)



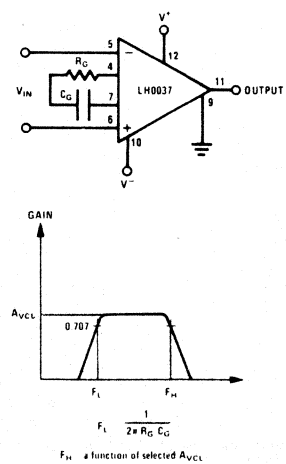
Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface



Pre MUX Signal Conditioning



High Pass Filter

National Semiconductor

LH0038/LH0038C True Instrumentation Amplifier

General Description

The LH0038/LH0038C is a precision true instrumentation amplifier (TIA) capable of amplifying very low level signals, such as thermocouple and low impedance strain guage outputs. Precision thin film gain setting resistors are included in the package to allow the user to set the closed-loop gain from 100 to 2000. Since the resistors are of a homogeneous single chip construction, they track almost perfectly so that temperature variations of closed loop gain are virtually eliminated.

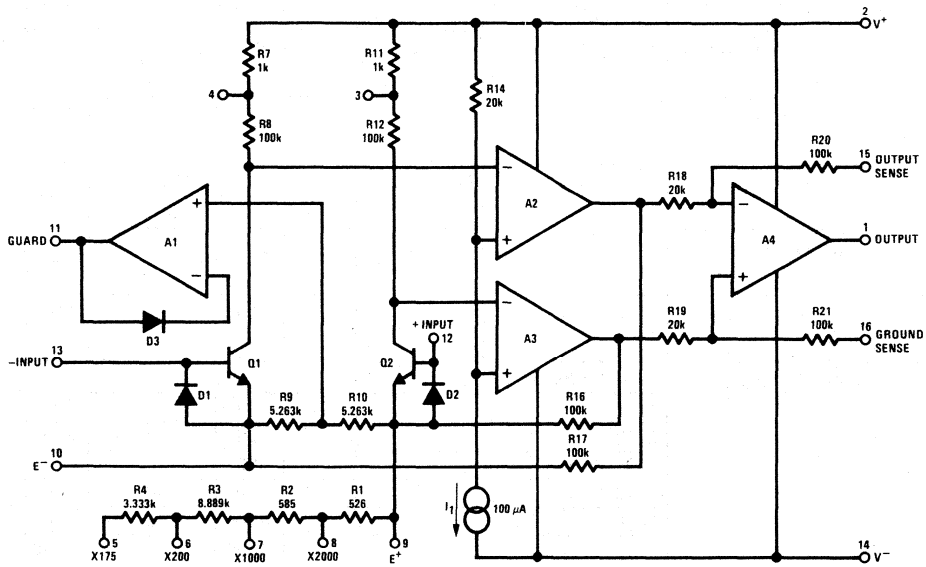
LH0038 exhibits excellent CMRR, PSRR, gain linearity, as well as extremely low input offset voltage, offset voltage drift and input noise voltage.

The devices are provided in a hermetically sealed 16-lead DIP. The LH0038 is guaranteed from −55°C to +125°C; whereas the LH0038C is guaranteed from −25°C to +85°C.

Features

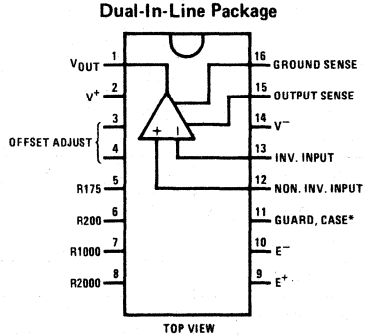
- Ultralow offset voltage 25 μV typ., 100 μV max
- Ultralow offset drift 0.25 μV/C max
- Ultralow input noise 0.2 μVp-p
- Pin strap gain options 100, 200, 400, 500, 1k, 2k
- Excellent PSRR and CMRR 120 dB

Simplified Schematic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LH0038CD or LH0038D
See NS Package D16D

*Guard output is connected to the case.

Absolute Maximum Ratings

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±1V
Input Voltage	$\pm V_S$
Power Dissipation (See Curve)	500 mW
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0038	−55°C to +125°C
LH0038C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 20 seconds)	300°C

DC Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS		LH0038			LH0038C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IOS}	Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$	$T_A = 25°C$		25	100		30	150	µV
						125			220	
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Tempco				0.1	0.25		0.2	1.0	µV/°C
V_{OOS}	Output Offset Voltage		$T_A = 25°C$		3	10		5	25	mV
						15			30	
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Tempco				25			25		µV/°C
I_B	Input Bias Current	$V_{CM} = 0V$	$T_A = 25°C$		50	100		50	100	nA
						200			200	
I_{OS}	Input Offset Current		$T_A = 25°C$		2	5		7	10	
						8			15	
$\Delta I_B/\Delta T$	Input Bias Current Tempco				500			500		pA/°C
A_{VCL}	Closed Loop Gain	Gain Pins Jumpered								V/V
		None			100			100		
		6–10			200			200		
		6–9, 10–5			400			400		
		6–10, 5–9			500			500		
		7–10			1000			1000		
		8–10			2000			2000		
	Closed Loop Gain Error	A_{VCL} = 100, 200			0.1	0.3		0.1	0.4	%
		A_{VCL} = 400, 500			0.2	0.3		0.2	0.6	
		A_{VCL} = 1000			0.3	0.5		0.5	1.0	
		A_{VCL} = 2000			1.0	2.0		1.5	3.0	
	Gain Temperature Coefficient	A_{VCL} = 1k			7			7		ppm/°C
	Gain Nonlinearity	$100 \leq A_{VCL} \leq 2k$			1			1		ppm
V_{INCM}	Common-Mode Input Voltage Range			±10	±12		±10	±12		V
V_O	Output Voltage	$R_L \geq 10\ k\Omega$		±10	±12		±10	±12		V
V_S	Supply Voltage Range			±5		±18	±5		±18	
	Guard Voltage Error	$-10V < V_{CM} < +10V$			±10	±100		±10	±100	mV

DC Electrical Characteristics (Note 2) (Continued)

PARAMETER		CONDITIONS		LH0038			LH0038C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±10V	A_{VCL} = 100	94	110		86	110		dB
			A_{VCL} = 1000	114	120		106	110		
PSRR	Power Supply Rejection Ratio	±5V ≤ ΔV_S ≤ ±15V	A_{VCL} = 100	94	110		94	110		
			A_{VCL} = 1000	110	120		100	110		
I_{OSC}	Output Short Circuit Current	T_A = 25°C		±2	±5	±10	±2	±5	±10	mA
I_S	Supply Current	T_A = 25°C			1.6	2.0		1.6	3.0	
R_{IN} DIFF	Input Resistance	A_{VCL} = 1000, T_A = 25°C			5			5		MΩ
R_{IN} CM	Common-Mode Input Resistance				1			1		GΩ
R_{OUT}	Output Resistance				1			1		mΩ

AC Electrical Characteristics V_S = ±15V, T_A = 25°C

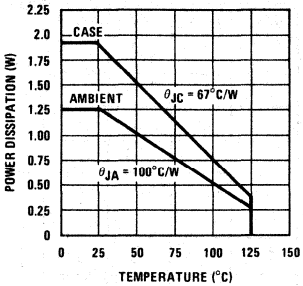
PARAMETER		COMMENT	CONDITIONS		TYP	UNITS
e_n	Equivalent Input Noise Voltage	*Figure 1*	R_S = 0, f = 0.1 to 10 Hz		0.2	μVp-p
$\overline{e_n}$	Equivalent Input Spot Noise Voltage	*Figure 1*	R_S = 100Ω	f = 10 Hz	6.5	nV/√Hz
				f = 100 Hz	6.0	
				f = 1 kHz	6.0	
				f = 10 kHz	6.0	
BW	Large Signal Bandwidth		V_{OUT} = ±10V		1.6	kHz
S_r	Slew Rate		V_{OUT} = ±10V		0.3	V/μs
t_s	Settling Time to 0.01%	*Figure 13*		20V Step	120	μs
				−10V Step	80	
				+10V Step	60	
t_r	Rise Time		ΔV_{OUT} = 100 mV	A_{VCL} = 100	6	μs
				A_{VCL} = 1000	13	
$\overline{i_n}$	Equivalent Input Spot Noise Current		R_S = 100 MΩ	f = 10 Hz	0.1	pA/√Hz

Note 1: The inputs are protected by diodes for overvoltage protection. Excessive currents will flow for differential voltages in excess of ±1V. Input current should be limited to less than 10 mA.

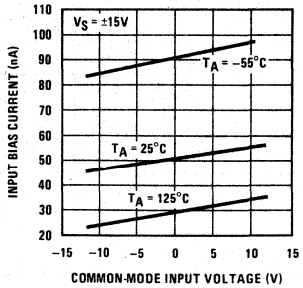
Note 2: Unless otherwise noted these specifications apply for V_S = ±15.0V, pin 15 connected to pin 1, pin 16 connected to ground, over the temperature range −55°C to +125°C for the LH0038 and −25°C to +85°C for LH0038C.

Typical Performance Characteristics

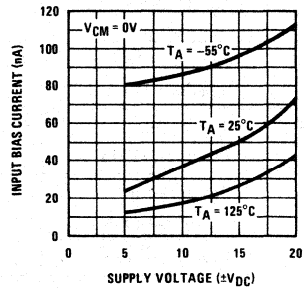
Power Dissipation



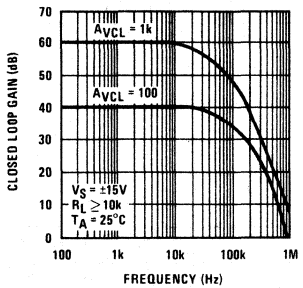
Input Bias Current



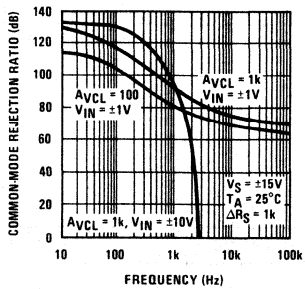
Input Bias Current



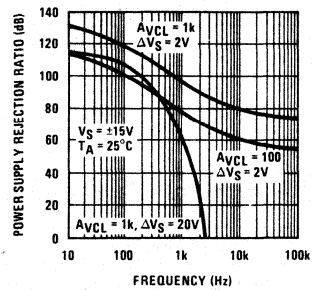
Closed Loop Frequency Response



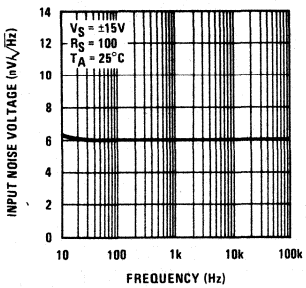
Common-Mode Rejection



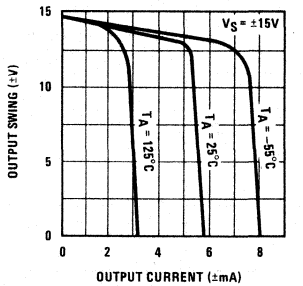
Power Supply Rejection



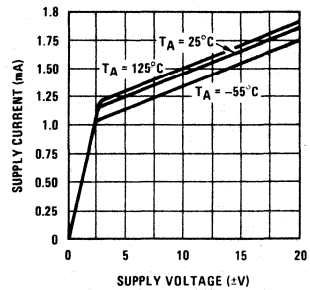
Input Noise Voltage (Includes Source Impedance)



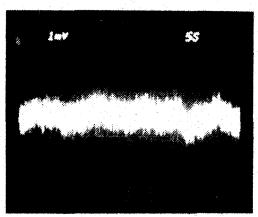
Output Swing



Supply Current

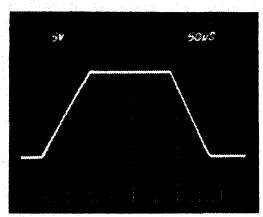


Wide Band Noise



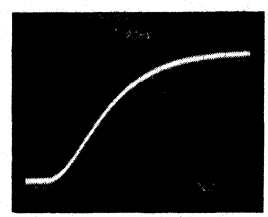
V_S = ±15V, R_S = 1kΩ, A_V = 10k, DUT = 1k
Vertical sensitivity: 0.1 μV/CM
Horizontal sensitivity: 5 sec/CM
Bandwidth: 0.1 Hz to 10 Hz

Pulse Response



V_S = ±15V
$R_L \geq$ 10kΩ
A_{VCL} = 1k

Rise Time



V_S = ±15V
$R_L \geq$ 10kΩ
A_{VCL} = 1k

Noise Test Circuit

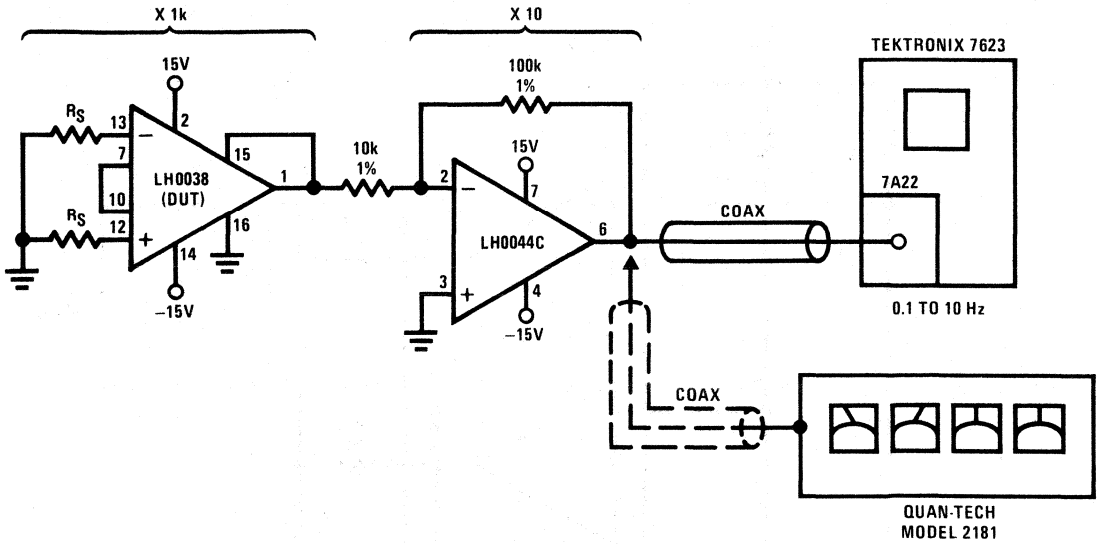


FIGURE 1.

Typical Application

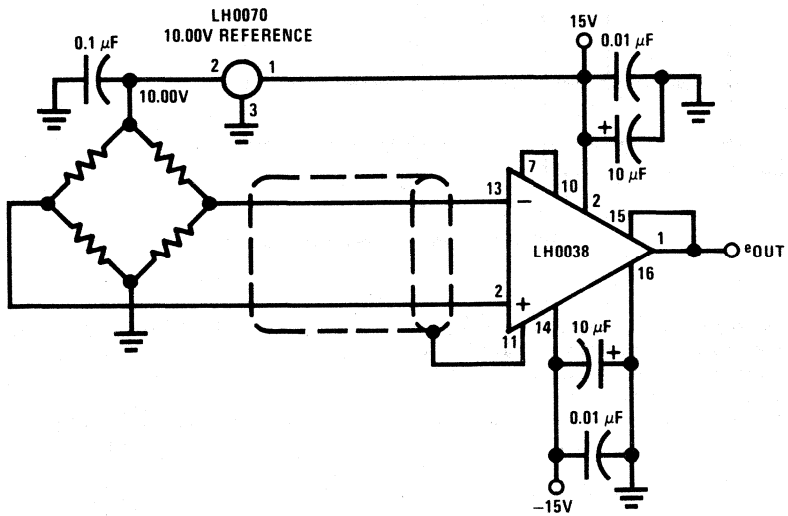


FIGURE 2. X1000 Bridge Amplifier

Applications Information

THEORY OF OPERATION

The LH0038 is a 3-stage, true instrumentation amplifier composed of a well matched transistor differential pair, Q1 and Q2, a common-mode loop amplifier, A2 and A3, and a differential to single ended amplifier, A4. A simplified schematic is shown in *Figure 3.*

Current source, I_A, establishes a voltage across R14 of approximately 2V, which results in a 2V drop across R8 and R12. This constant voltage forces the first stage current to be 20 μA per side. The action of A2 and A3 is such that 20 μA is maintained constant despite the presence of common-mode signals. The differential outputs of A2 and A3 are applied to differential amplifier, A4, which converts the signal to a single-ended output and provides a gain of 5. The total gain of the amplifier is, therefore, the fixed gain of 5 multiplied by the gain of the composite input stage.

Applications Information (Continued)

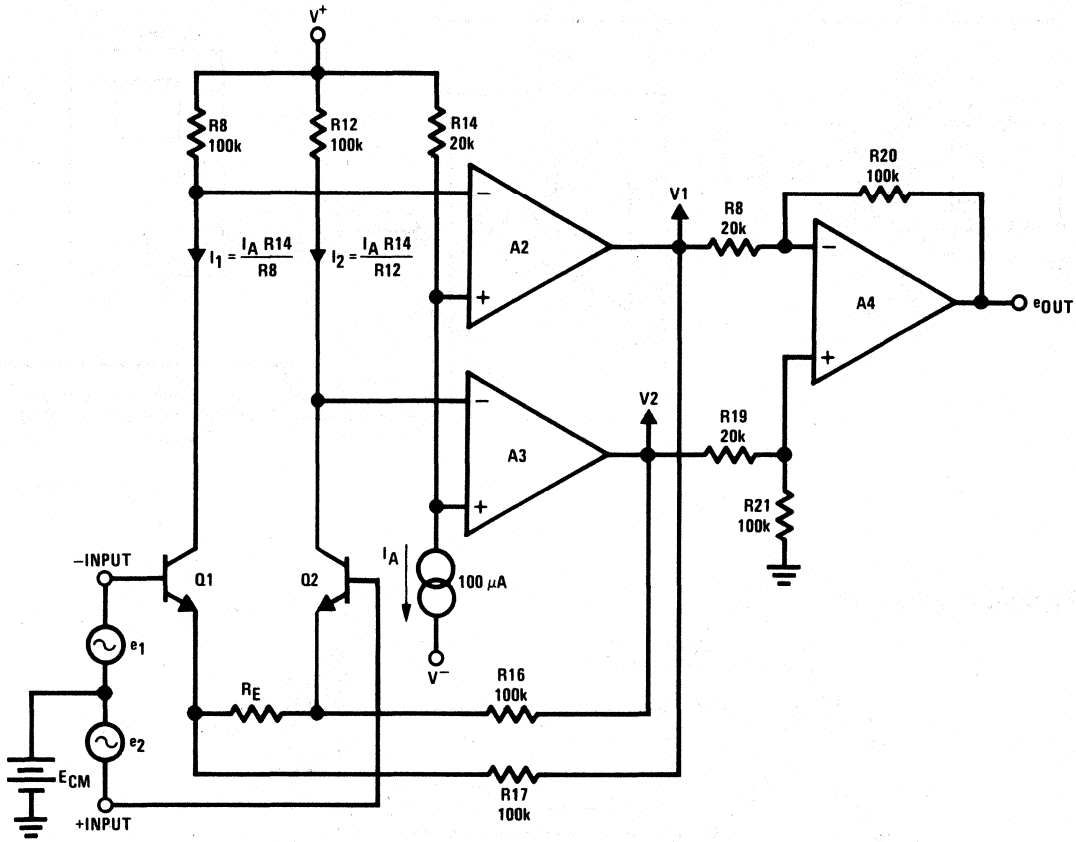


FIGURE 3. LH0038 Simplified Schematic

The closed loop gain of the composite amplifier may be better understood by referring to *Figure 3*. The Q1–A2 loop may be viewed as differential amplifier with the inverting input at the base and non-inverting input at the emitter. Combining small signal AC and large signal DC analysis =

$$v1 = e1\left(\frac{R17 + R_E}{R_E}\right) - e2\left(\frac{R17}{R_E}\right) + E_{CM} - V_{BE1} - I_1 R17 \quad (1)$$

By similar analysis:

$$v2 = e2\left(\frac{R16 + R_E}{R_E}\right) - e1\left(\frac{R16}{R_E}\right) + E_{CM} - V_{BE2} - I_2 R16 \quad (2)$$

For $I_1 \equiv I_2$, $R17 \equiv R16$, $V_{BE1} \equiv V_{BE2}$, subtracting equation (1) from (2) results in:

$$v2 - v1 = (e2 - e1)\left(\frac{R16 + R_E}{R_E}\right) + (e2 - e1)\left(\frac{R16}{R_E}\right) \quad (3)$$

$$\frac{v2 - v1}{e2 - e1} = \frac{2\,R16}{R_E} + 1 \quad (4)$$

Applications Information (Continued)

The differential input voltage (v2 − v1) is amplified by the closed loop gain of A4:

$$e_{OUT} = (A_{VCL4})\,(e2 - e1) \qquad (5)$$

where:

$$A_{VCL4} = \frac{R20}{R8}$$

$$= 5.00$$

$$\boxed{A_{VCL} = 5\left(\frac{2R16}{R_E} + 1\right)} \qquad (6)$$

As an example, with all gain pins open, R_E = 10.526 kΩ, and:

$$A_{VCL} = 5\left(\frac{(2)\,(100k)}{10.526k} + 1\right) \qquad (7)$$

$$= 100.0$$

All other closed loop gain configurations place a precision resistor in parallel with R_E(R9 + R10). For example, for a gain of 200, pin 6 is connected to pin 10 and the gain is predicted by:

$$A_{VCL} = 5.00\left[\frac{(2)\,(100k)}{(10.526k)\,\|\,(10.000k)} + 1\right] \qquad (8)$$

$$= (5.00)\,(40) = 200$$

CLOSED LOOP GAIN CONSIDERATIONS USING INTERNAL RESISTORS

Table I summarizes the primary gain configurations available with the LH0038. Obviously, other gains are possible. Using the internally supplied resistors has the advantage that R16, R17, and R_E all track thermally, minimizing the device's gain error as a function of temperature.

Gain adjustment by paralleling or series padding internally supplied resistors is generally discouraged since external resistors will generally not thermally track. It is recommended that the gain adjustment be done in a subsequent stage as shown in *Figure 4.*

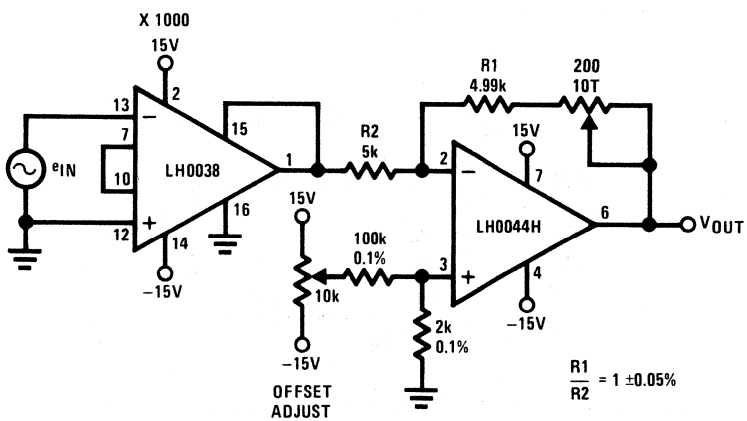


FIGURE 4. Recommended Gain Adjust Circuit

TABLE I. LH0038 INTERNAL GAIN CONFIGURATIONS

OVERALL GAIN	FIRST STAGE GAIN	PIN CONNECTIONS	EFFECTIVE R_E
100	20	All Gain Pins Open	10.5260 kΩ
200	40	Pin 6 to Pin 10	5.1281 kΩ
400	80	Pin 6 to Pin 9, Pin 10 to Pin 5	2.5316 kΩ
500	100	Pin 6 to Pin 10, Pin 9 to Pin 5	2.0202 kΩ
1000	200	Pin 7 to Pin 10	1.0050 kΩ
2000	400	Pin 8 to Pin 10	0.5013 kΩ

Applications Information (Continued)

GUARD DRIVE

The LH0038 is provided with a guard drive output, which will always be at the input common-mode voltage. The guard drive amplifier is short-circuit proof and is capable of driving several thousand pF without danger of latch-up or oscillation.

The guard drive tied to a shielded input cable will greatly reduce noise pick-up, and also improve AC CMRR by maintaining the shield at the common-mode voltage. *Figure 5* illustrates the proper use of the guard drive. The guard drive output is also connected to the case to provide electrostatic shielding to the system.

REMOTE OUTPUT SENSE

The feedback network of the LH0038 may be closed directly at the load in order to eliminate errors due to lead resistance. Also, a unity gain buffer; e.g. LH0002, may be included within the feedback loop to increase output current capability as shown in *Figure 7.*

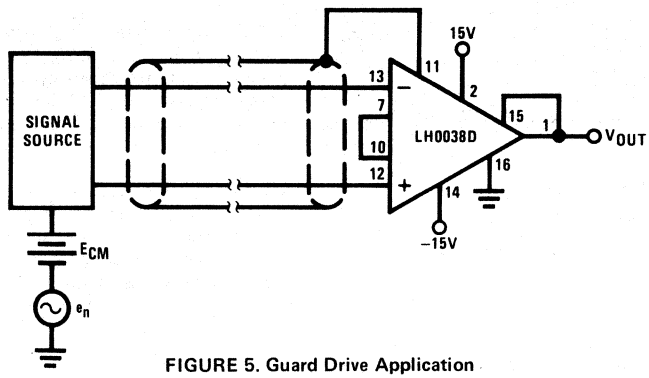


FIGURE 5. Guard Drive Application

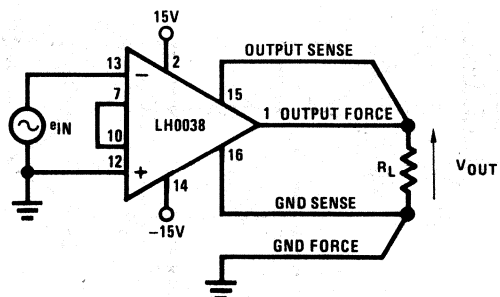


FIGURE 6. Remote Sense Connection

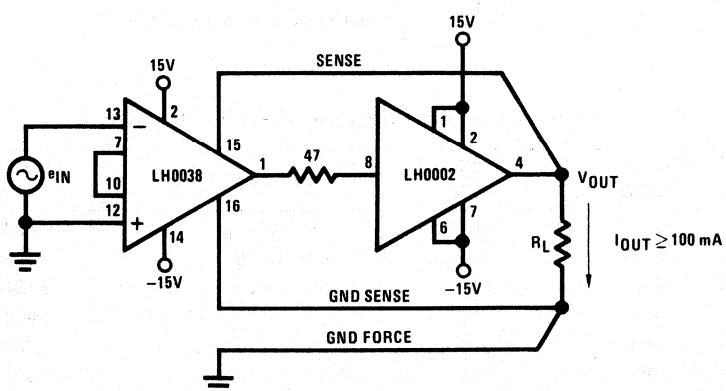


FIGURE 7. Output Buffer Connection

Applications Information (Continued)

OFFSET NULL

Offset of the LH0038 is trimmed by the factory to a very low value. The offset may be further trimmed using a 10 kΩ, 10 turn, 100 ppm/°C potentiometer as shown in *Figure 8.* However, a drift increase of 0.3 μV/°C will be caused for each 100 μV of offset adjusted. The recommended offset null is shown in *Figure 4* and is accomplished in the following stage.

BIAS CURRENT CONSIDERATIONS

The LH0038 exhibits bias current of approximately 50 nA per side, and requires a path to ground or supply. The practical limitation to the maximum resistance between the inputs and ground is dictated by negative common-mode range as shown in *Figure 9*. For example, for $V_{CM} = -10V$, $R_{CM} \leq 20\ M\Omega$.

The LH0038 input stage bias was optimized for minimum voltage noise so the input bias currents are higher than might otherwise be expected. Note, however, that the input currents are very well matched, resulting in an offset current value much lower than one might infer from the bias current. In order to take advantage of this low offset current, the source impedances at both inputs should be matched to minimize DC drift. Further, bias current is relatively constant with temperature (as opposed to an FET stage), so one can consider bias current compensation schemes such as shown in *Figure 10.* The danger with such techniques is that the offset current and noise contributed by the bias current compensator will dominate the system noise.

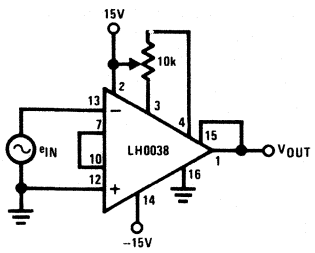


FIGURE 8. Offset Adjust Circuit
(See also *Figure 4*)

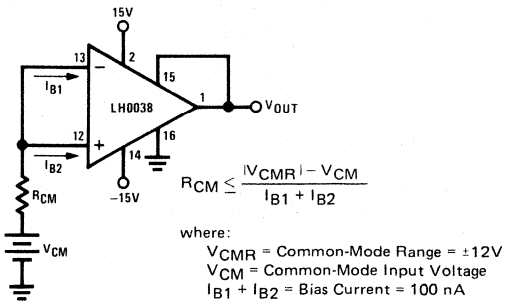


FIGURE 9. Bias Current Return

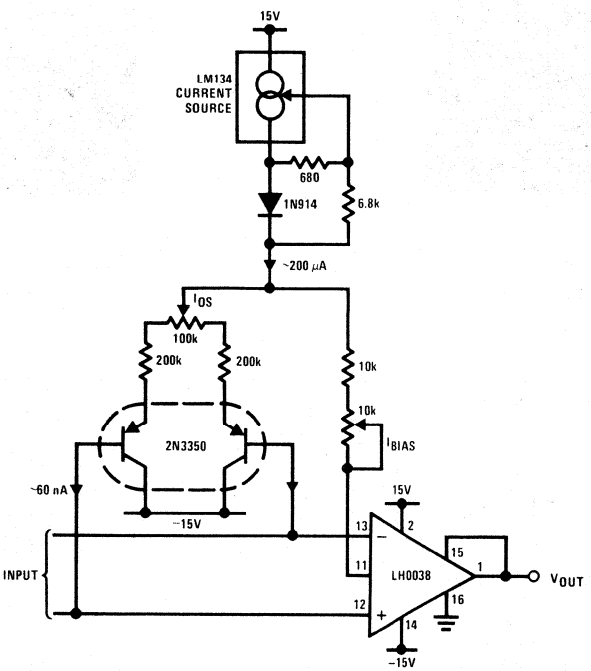


FIGURE 10. Bias Current Compensation

Applications Information (Continued)

SETTLING TIME

The LH0038 has been purposely over-compensated, and is therefore remarkably free from any undesirable transient response. Small signal settling time is governed by gain-bandwidth product; large signal settling time is dominated by slew rate.

Figure 11 shows an input voltage step of +10V to −10V applied, through a 1000 to 1 voltage divider, to the device configured for an inverting gain of 1000. The output of the device will therefore be equal to the negative of the input after the device is completely settled. By resistively subtracting the input before the divider from the device output, a pseudo summing node is generated. The voltage at this pseudo summing junction goes "off screen" on the photos, since in the first small time increment the input goes instantaneously to −10 mV and the output is still at +10V. About 130 μs after the input has gone negative, the output slews back in range and begins an exponential approach to the final value. *Figure 12* is the same set-up for a −10V to +10V input pulse. Note that there is no overshoot in either case. The test circuit is shown in *Figure 13*.

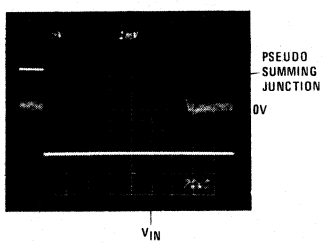
HIGH FREQUENCY CMRR

The LH0038 resistor ratios are carefully trimmed for optimum CMRR at DC through 60 Hz. Inevitably, this rejection will degrade at higher frequencies due to 2 separate effects: stray capacitance mismatch and slew rate limiting in the input stage. In most discrete instrumentation amplifier realizations, the stray capacitance mismatch dominates simply because the stray capacitances are relatively large (this can be trimmed out in a discrete amplifier). In a hybrid circuit such as the LH0038, stray capacitance is minimized, so the effects of mismatch are also minimized.

The response to a pulse or noise spike applied as a common-mode signal may be dominated by the slew characteristics of the input stage. Whenever the common-mode input slew rate exceeds 0.2 V/μs, the 2 input amplifiers will apply identical ramp signals to the final stage and cause its output to go to near 0V. Note that the amplifier is not really active under these conditions as normal mode signal variations will *not* be coupled to the output. Some time may be required for the amplifier to settle after a transient of this kind before the output can be considered representative of the input. Slew rate limiting will not normally be the limiting factor for sine wave common-mode signals as 0.2 V/μs corresponds to about 2 kHz (20 Vp-p).

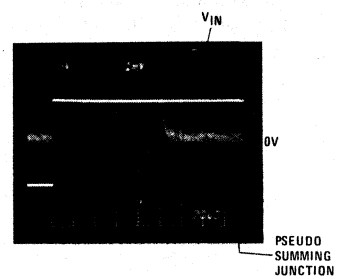
POWER SUPPLY DECOUPLING

Although the LH0038 exhibits in excess of 120 dB PSRR at DC, the figure degrades to 100 dB at 120 Hz. It is recommended that both V^+ and V^- leads be bypassed with 1 μF electrolytic in shunt with 0.01 μF ceramic disc no further than 1 inch from the device.



t_s, A_V = 100, V_{IN} = −20V

FIGURE 11. Settling Time



t_s, A_V = 100, V_{IN} = 20V

FIGURE 12. Settling Time

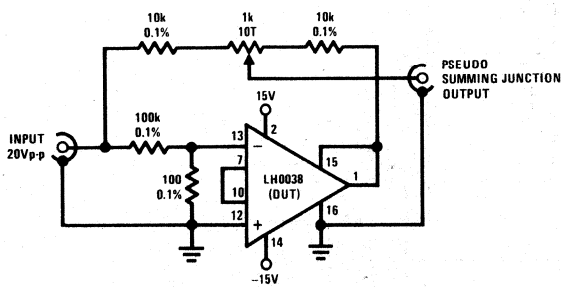


FIGURE 13. Settling Time Test Circuit

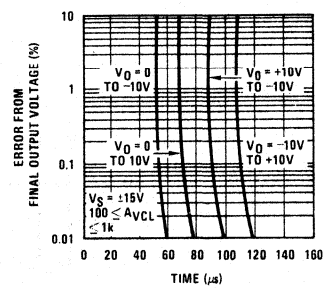


FIGURE 14. Settling Time

Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to 3 dB below the low frequency value.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the outputs of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{IOS} = \frac{(V_{OS})\,2k - (V_{OS})\,100}{1900}$$

Where:

$(V_{OS})2k$ = overall offset voltage for A_{VCL} = 2k.

$(V_{OS})100$ = overall offset voltage for A_{VCL} = 100.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end points expressed as a percent of full-scale (10V for operations on ±15V supply). Note that this is a more stringent specification than deviation from the best straight line and is double the number that would be specified if the percentage were based on a 20V (±10V) range.

Guard Voltage Error: The voltage difference between the guard drive output and the average of the 2 input voltages.

Input Bias Current, I_B: The average of the 2 input currents.

Input Common-Mode Voltage Range, V_{INCM}: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Offset Current, I_{OS}: The difference in the currents into the 2 input terminals when the output is at zero.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Overall Offset Voltage, V_{OS}: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input amplifier offset voltage effects, V_{IOS}, and output amplifier effects, V_{OOS}. It is given by:

$$V_{OS} = (A_{VCL})\,(V_{IOS}) - V_{OOS}$$

Where:

A_{VCL} = closed loop gain = 100 to 2k

V_{IOS} = input stage offset voltage

V_{OOS} = output stage offset voltage

Output Offset Voltage, V_{OOS}: The output voltage when the outputs of the input stage are forced to 0V. V_{OOS} may be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{OOS} = \frac{(20)\,(V_{OS})\,100 - (V_{OS})\,2k}{19}$$

Where:

$(V_{OS})\,100$ = overall offset voltage for A_{VCL} = 100

$(V_{OS})\,2k$ = overall offset voltage for A_{VCL}

Output Voltage, V_O: The peak output voltage swing, referred to zero.

Offset Voltage Temperature Drift, $\Delta V_{IOS}/\Delta T$: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection Ratio, PSRR: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Times, t_s: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate, S_r: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current, $\pm I_s$: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Supply Voltage Range: The range of voltages on the supply terminals for which the device is operational. Note that the specifications are not guaranteed over the full supply voltage range unless specifically stated.

Transient Response, t_r: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from DC to the frequency where the amplifier open loop gain rolls off to 1.

Closed Loop Gain, A_{VCL}: The ratio of output voltage to input voltage under the stated conditions of source resistance (R_S) and load resistance (R_L).

Voltage Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

National Semiconductor

LH0044 Series Precision Low Noise Operational Amplifiers

General Description

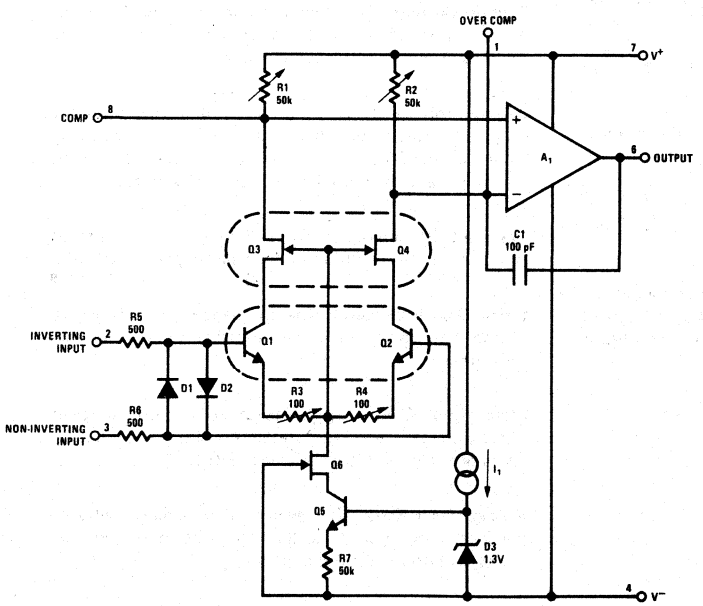
The LH0044 Series is a low noise, ultra-stable, high gain, precision operational amplifier family intended to replace either chopper-stabilized monolithic or modular amplifiers. The devices are particularly suited for differential mode, inverting, and non-inverting mode applications requiring very low initial offset, low offset drift, very high gain, high CMRR, and high PSRR. In addition, the LH0044 Series' low initial offset and offset drift eliminate costly and time consuming null adjustments at the systems level. The superior performance afforded by the LH0044 Series is made possible by advanced processing and testing techniques, as well as active laser trim of critical metal film resistors to minimize offset voltage and drift. Unique construction eliminates thermal feedback effects.

The LH0044 Series is an excellent choice for a wide range of precision applications including strain gauge bridges, thermocouple amplifiers, and ultrastable reference amplifiers. The LH0044 and LH0044A are guaranteed over the temperature range of −55°C to +125°C, and the LH0044AC, LH0044B, and LH0044C are guaranteed from −25°C to +85°C. The device is available in standard TO-5 op amp pin out and is compatible with LM108A, LM725, and LM741 type amplifiers.

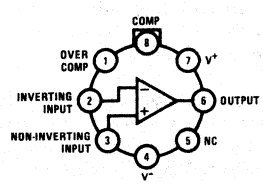
Features

- Low input offset voltage 25μV max
- Excellent long-term stability ±1μV/month max
- Low offset drift 0.5μV/°C max
- Very low noise 0.7μVp-p max 0.1 Hz to 10 Hz
- High CMRR and PSRR 120 dB min
- High open loop gain 120 dB min
- Wide common-mode range ±13V min
- Wide supply voltage range ±2V to ±20V

Equivalent Circuit and Connection Diagram



Metal Can Package



TOP VIEW

Case is electrically isolated

Note: Compensation is not normally required. However, for maximum stability, a 0.01μF capacitor should be placed between pins 7 and 8 when device is used below closed loop gains of 10.

Order Number LH0044H, LH0044AH, LH0044BH, LH0044CH or LH0044ACH
See Package H08B

Absolute Maximum Ratings

Supply Voltage	±20V	Operating Temperature Range	
Power Dissipation	600 mW	LH0044, LH0044A	−55°C to +125°C
Differential Input Voltage (Note 4)	±15V	LH0044AC, LH0044B, LH0044C	−25°C to +85°C
Input Voltage (Note 5)	±15V	Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Continuous	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0044A/LH0044AC			LH0044/LH0044B/LH0044C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S = 50\Omega$, $V_{CM} = 0V$		8	25		12	50	μV
	LH0044C Only						100	μV
Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$			50			150	μV
	LH0044A and LH0044B Only			75			75	μV
Average Input Offset Voltage Drift	$T_{MIN} \leq T_A \leq T_{MAX}$		0.1	0.5		0.2	1.0	μV/°C
	LH0044B Only						0.5	μV/°C
Long-Term Stability	(Note 2)		0.2	1		0.3	2	μV/month
Input Noise Voltage (Note 3)	BW = 0.1 Hz to 10 Hz, $R_S = 50\Omega$		0.35	0.7		0.35	0.8	μVp-p
	R_S = 10 kΩ Imbalance		0.50	0.9		0.50	1.0	μVp-p
Thermal Feedback Coefficient			0.005			0.005		μV/mW
Open Loop Voltage Gain	R_L = 10 kΩ	120	145		114	140		dB
Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	120	145		114	140		dB
Power Supply Rejection Ratio	$\pm 3V \leq V_S \leq \pm 18V$	120	145		114	140		dB
Input Voltage Range		±13	±13.8		±12	±13.5		V
Output Voltage Swing	R_L = 10 kΩ	±13	±13.7		±12	±13.5		V
Input Offset Current	$25°C \leq T_A \leq T_{MAX}$		1.0	2.5		1.5	5.0	nA
	$T_{MIN} \leq T_A < 25°C$			5.0			10.0	nA
Average Input Offset Current Drift			5	40		15	80	pA/°C
Input Bias Current	$25°C \leq T_A \leq T_{MAX}$		8.5	15		10	30	nA
	$T_{MIN} \leq T_A < 25°C$			50			100	nA
Average Input Bias Current Drift			50	300		100	600	pA/°C
Differential Input Impedance		5	10		2.5	8		MΩ
Common-Mode Input Impedance			2×10^{11}			2×10^{11}		Ω
Supply Current	$I_L = 0$		0.9	3.0		1.0	4.0	mA
Power Dissipation			27	90		30	120	mW

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm 15V$

PARAMETER	CONDITIONS	TYP	UNITS
Input Noise Voltage	R_S = 1 kΩ, f_O = 10 Hz	11	$nV/\sqrt{Hz}$
	R_S = 1 kΩ, f_O = 1 kHz	9	$nV/\sqrt{Hz}$
Slew Rate	$A_V = +1$, R_L = 10 kΩ, $V_{IN} = \pm 10V$	0.06	V/μs
Large Signal Bandwidth	$A_V = +1$, R_L = 10 kΩ, $V_{IN} = \pm 10V$	1	kHz
Overload Recovery Time	$A_V = +100$, $V_{IN} = -100$ mV, ΔV_{IN} = 200 mV	5	μs
Small Signal Bandwidth	$A_V = +1$, R_L = 10 kΩ	400	kHz
Small Signal Rise Time	$A_V = +1$, R_L = 10 kΩ, V_{IN} = 10 mV	2.5	μs
Overshoot	$A_V = +1$, R_L = 10 kΩ, V_{IN} = 10 mV, C_L = 100 pF	10	%

Note 1: All specifications apply for all device grades, at $V_S = \pm 15V$, and from T_{MIN} to T_{MAX} unless otherwise specified. T_{MIN} is −55°C and T_{MAX} is +125°C for the LH0044A and LH0044. T_{MIN} is −25°C and T_{MAX} is +85°C for the LH0044AC, LH0044B and LH0044C. Typicals are given for $T_A = 25°C$.

Note 2: This parameter is not 100% tested; however, 90% of the devices are guaranteed to meet this specification after one month of operation and after initial turn-on stabilization.

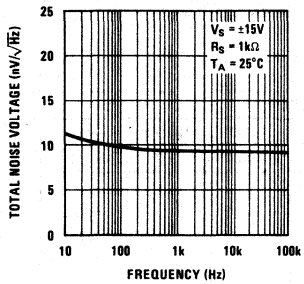
Note 3: Noise is 100% tested on the LH0044A, LH0044AC and LH0044B only. 90% of the LH0044 and LH0044C devices are guaranteed to meet this specification.

Note 4: The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow for differential input voltages in excess of 1V. Input current should be limited to less than 1 mA.

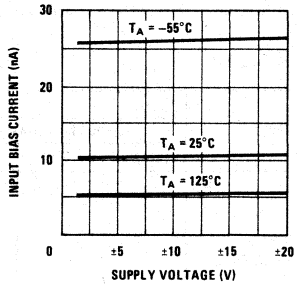
Note 5: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Typical Performance Characteristics

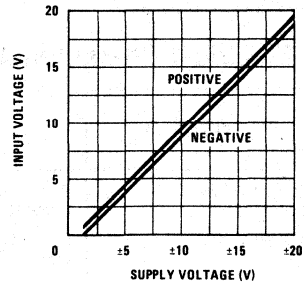
Total Input Noise Voltage vs Frequency



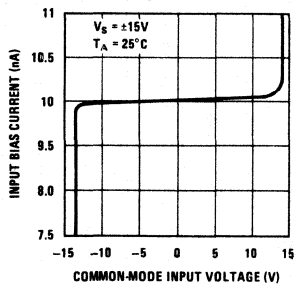
Input Bias Current



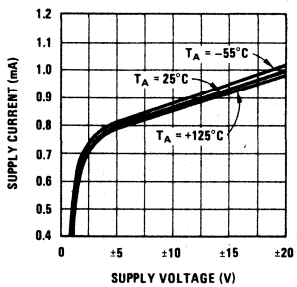
Input Voltage Range



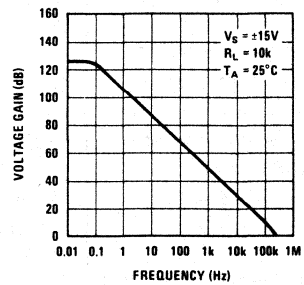
Input Bias Current vs Common-Mode Input Voltage



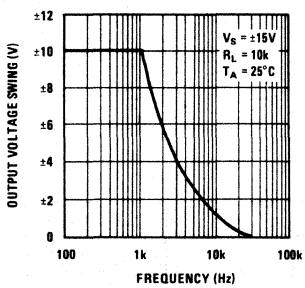
Supply Current vs Supply Voltage



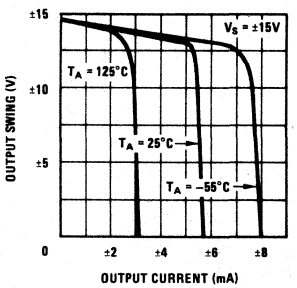
Open Loop Frequency Response



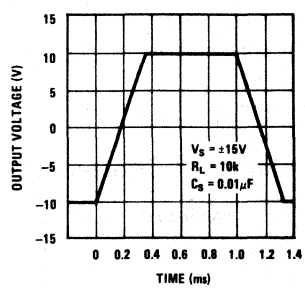
Large Signal Voltage Response



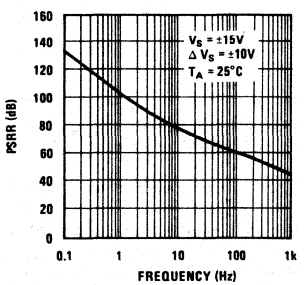
Output Swing



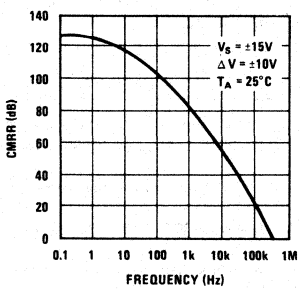
Large Signal Pulse Response



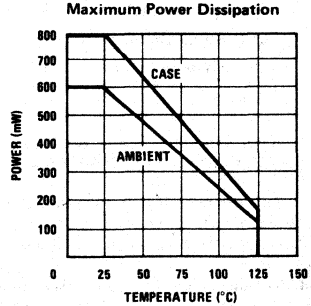
Power Supply Rejection Ratio vs Frequency



CMRR vs Frequency



Maximum Power Dissipation



Applications Information

LOW DRIFT CONSIDERATIONS

Achieving ultra-low drift in practical applications requires strict attention to board layout, thermocouple effects, and input guarding. For specific recommendations refer to AN-63 and AN-79.

A point worth stressing with regard to low drift specifications is testing of the LH0044. Simply stated—it is virtually impossible to test the device using a thermoprobe or other form of local heating. A one degree centigrade temperature gradient can account for tens of microvolts of virtual offset (or drift). The test circuit of *Figure 1* is recommended for use in a stabilized oven or continuously stirred oil bath with the entire circuit inside the oven or bath. Isothermal layout of the resistors is advised in order to minimize thermocouple induced EMF's.

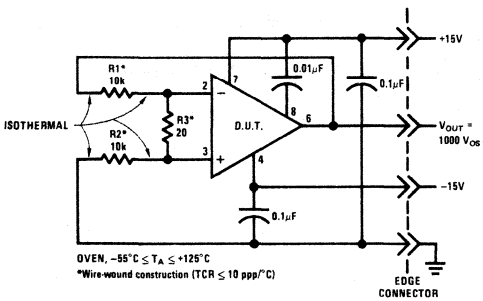


FIGURE 1. LH0044 Temperature Test Circuit

OVER COMPENSATION

The LH0044 may be overcompensated in order to minimize noise bandwidth by paralleling the internal 100 pF capacitor with an external capacitor connected between pins 1 and 6. Unity gain frequency may be predicted by:

$$f = \frac{4 \times 10^{-5}}{100\ pF + C_{ext}\ pF}\ (Hz)$$

COMPENSATION

For closed loop gains in excess of 10, no external components are required for frequency stability. However, for gains of 10 or less, a 0.01μF disc capacitor is recommended between pin 7 (V^+) and pin 8 (Comp). An improvement in ac PSRR will also be realized by use of the 0.01μF capacitor.

OFFSET NULL

In general, further nulling of LH0044 is neither necessary nor recommended. For most applications the specified initial offset is sufficient.

However, for those applications requiring additional null, an obvious temptation might be to place a pot between pins 1 and 8 with the wiper returned to V^+. This technique will usually result in reduced gain and increased offset drift due to mismatch in the TCR of the pot and R1 and R2. The technique is, therefore, not generally recommended.

The recommended technique for offset nulling the LH0044 is shown in *Figure 2.* Null is accomplished in A_2 and all errors are divided by the closed loop gain of the LH0044. Additional offset and drift incurred due to use of A_2 is less than 1μV/V for V^+ and V^- changes and 0.01μV/°C drift for the values shown in *Figure 2.*

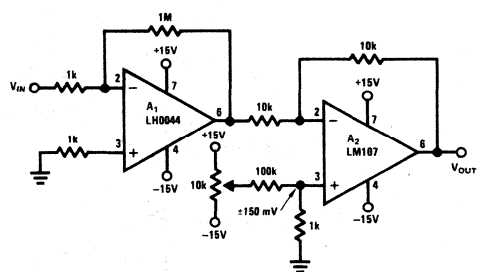
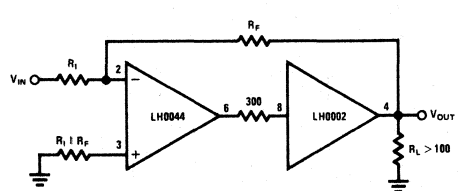
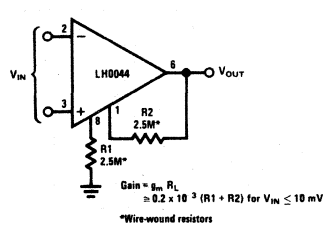


FIGURE 2. LH0044 Null Technique

Typical Applications

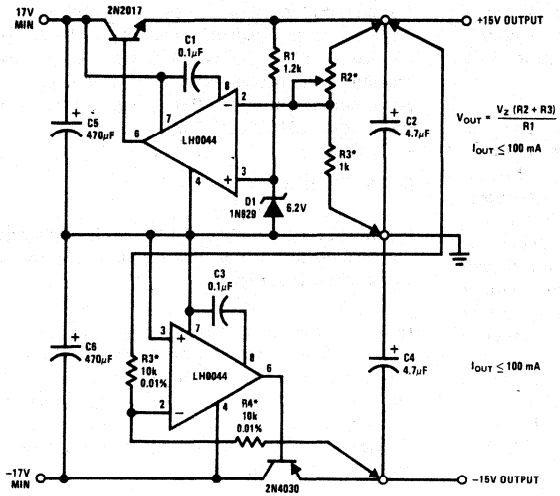


Buffered Output for Heavy Loads



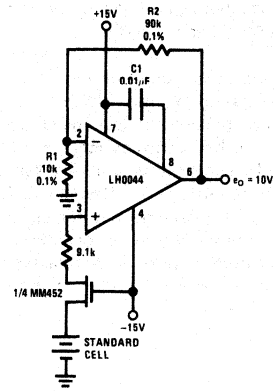
X1000 Instrumentation Amp

Typical Applications (Continued)

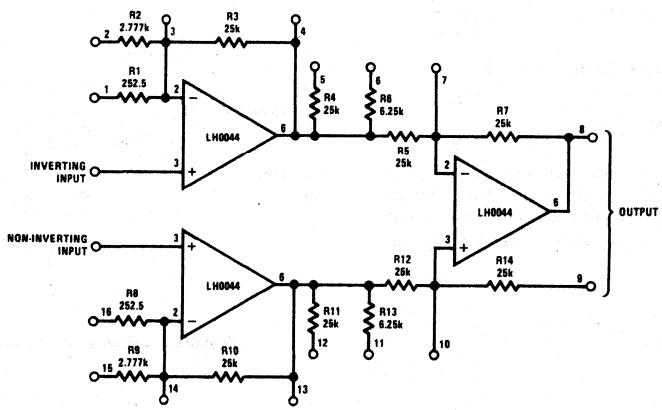


*Wire-wound for minimum drift.
Line and load regulation ≤ 0.005%

Precision Dual Tracking Regulator



10V Reference Supply

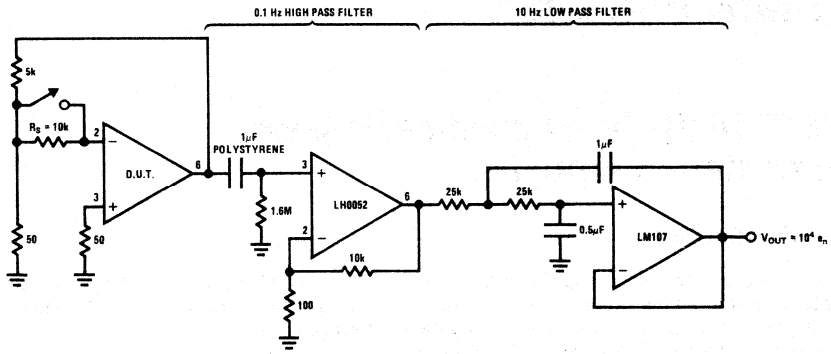


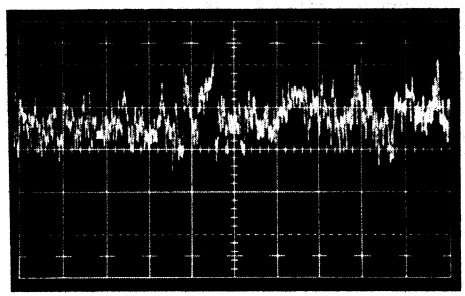
All resistors are part of National's RA201 resistor array.

OVERALL GAIN	INPUT STAGE GAIN	OUTPUT STAGE GAIN	JUMPER PINS ON RA201
X1	X1	X1	–
X2	X1	X2	5 to 7, 12 to 10
X5	X1	X5	6 to 7, 11 to 10
X10	X10	X1	2 to 15
X20	X10	X2	2 to 15, 5 to 7, 12 to 10
X50	X10	X5	2 to 15, 6 to 7, 11 to 10
X100	X100	X1	1 to 16
X200	X100	X2	1 to 16, 5 to 7, 12 to 10
X500	X100	X5	1 to 16, 6 to 7, 11 to 10
X995	X199	X5	1 to 14, 6 to 7, 11 to 10

Precision Instrumentation Amplifier

Noise Test Circuit





National Semiconductor

LH0084C Digitally-Programmable-Gain Instrumentation Amplifier

General Description

The LH0084C is a self-contained, high speed, high accuracy, digitally-programmable-gain instrumentation amplifier. It consists of paired FET-input variable-gain voltage-follower input stages followed by a differential-to-single-ended output stage. The input stage is programmable in accurate gain steps of 1, 2, 5, or 10 controlled by the logic levels of a 2-bit TTL-compatible digital input word. For additional flexibility, the output stage is pin-strappable to fixed gains of 1, 4, or 10 for an overall gain range of 1 to 100.

Applications include increased dynamic range A-to-D converters, test systems, and post multiplexer amplifier for data acquisition systems.

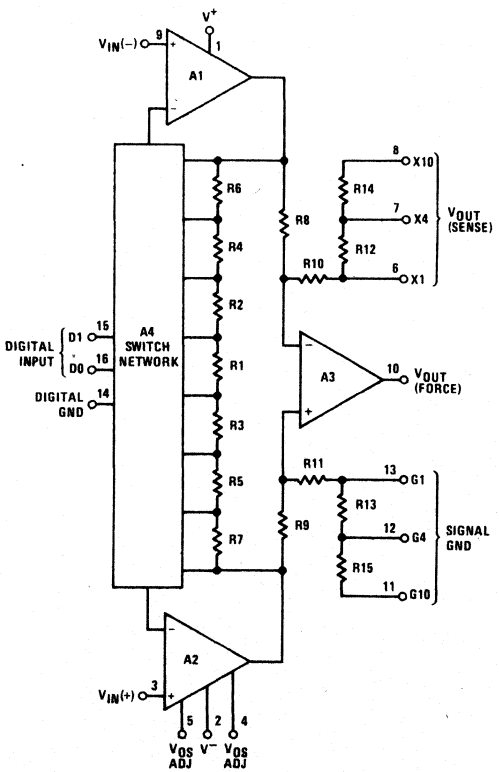
The device exhibits high input impedance, low offset voltage, high CMRR and PSRR, high speed, and excellent gain accuracy and gain non-linearity.

The LH0084C is guaranteed from −25°C to +85°C and is provided in a hermetically sealed 16-lead dual-in-line metal package.

Features

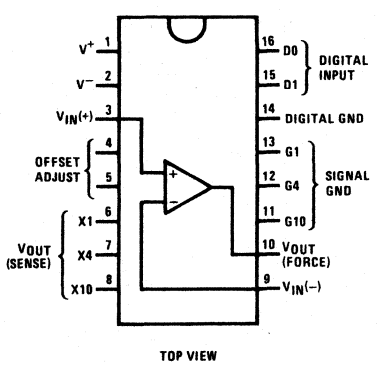
■ Excellent gain accuracy and gain non-linearity	0.1% max 0.002% typ
■ Extremely low gain drift	1 ppm/°C typ 10 ppm/°C max
■ High input impedance	$10^{11}\Omega$ typ
■ High CMRR and PSRR	70 dB min
■ TTL compatible digital inputs	
■ High speed, settling to 0.1%	4 μs max

Simplified Schematic



Connection Diagram

Dual-In-Line Package



TOP VIEW

Case is electrically isolated

Order Number LH0084CD
See NS Package D16D

Absolute Maximum Ratings

Supply Voltage (Note 1)	± 18V	Output Short Circuit Duration	Continuous
Analog Input Voltage (Note 2)	± 15V	Operating Temperature Range	−25°C to +85°C
Differential Input Voltage (Note 2)	± 30V	Storage Temperature	−65°C to +150°C
Digital Input Voltage	−4V, +18V	Lead Temperature (Soldering, 20 seconds)	+300°C
Power Dissipation (See Curve)	2.5W		

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

Parameter		Conditions		LH0084C Min	LH0084C Typ	LH0084C Max	Units
V_{IOS}	Input Offset Voltage		$T_j = 25°C$		0.3	10	mV
						13	
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Change with Temperature	$R_S = 100\Omega$, $V_{CM} = 0$			20		µV/°C
V_{OOS}	Output Offset Voltage	Note 3	$T_j = 25°C$		0.6	10	mV
						13	
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Change with Temperature				35		µV/°C
I_B	Input Bias Current (Note 3)		$T_j = 25°C$		150	500	pA
						100	nA
I_{OS}	Input Offset Current		$T_j = 25°C$		50	200	pA
						50	nA
R_{IN}	Input Resistance	Differential			10^{11}		Ω
		Common-Mode			10^{11}		
V_{IN}	Input Voltage Range			± 10	± 11.5		V
A_V	Voltage Gain	See Table I			1 2 5 10 20 50 100		V/V
	Gain Error	$A_V = 1, 2, 5, 10$	$T_A = 25°C$		0.02	0.1	%
		$A_V = 10, 20, 50, 100$			0.03	0.2	
		$A_V = 1, 2, 5, 10$			0.02	0.2	
		$A_V = 10, 20, 50, 100$			0.03	0.3	
	Gain Nonlinearity		$T_A = 25°C$		0.002		
					0.005		
$\Delta A_V/\Delta T$	Gain Temperature Coefficient				1	10	ppm/°C
CMMR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	$A_V = 1$	70	80		dB
			$A_V = 10$	76	94		
			$A_V = 100$	80	94		
PSRR	Power Supply Rejection Ratio	$\pm 8V \le V_S \le \pm 18V$	$A_V = 1$	70	84		
			$A_V = 10$	76	92		
			$A_V = 100$	80	104		
V_O	Output Voltage Swing	$R_L \ge 10\ k\Omega$		± 10	± 12		V

DC Electrical Characteristics (Continued) $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

Parameter		Conditions		LH0084C Min	LH0084C Typ	LH0084C Max	Units
I_O	Output Short-Circuit Current	$T_A = 25°C$		±5	±18	±30	mA
				±2		±30	
r_O	Output Resistance				0.05		Ω
V_{IL}	Digital "0" Input Voltage					0.7	V
V_{IH}	Digital "1" Input Voltage			2.0			
I_{IL}	Digital "0" Input Current	$V_{IN} = 0.4V$			1.5	40	μA
I_{IH}	Digital "1" Input Current	$V_{IN} = 2.4V$			0.01		
V_S	Supply Voltage Range			±8		±18	V
$I_{S(+)}$	Positive Supply Current	$V_S \le \pm 18V$			12.8	26	mA
$I_{S(-)}$	Negative Supply Current				8.2	14	
P_D	Power Dissipation	$V_S = \pm 15V$			315	600	mW

AC Electrical Characteristics (Note 5) $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10\ k\Omega$

Parameter		Conditions		Min	Typ	Max	Units
BW	Bandwidth (*Figure 1*)	Small Signal, −3 dB	$A_V = 1$		3250		kHz
			$A_V = 10$		500		
			$A_V = 100$		350		
		Small Signal, −1%	$A_V = 1$		300		
			$A_V = 10$		75		
			$A_V = 100$		55		
PBW	Power Bandwidth	$V_o = \pm 10V$			200		
SR	Slew Rate			10	13		V/μs
t_S	Settling Time (*Figure 2*) ±0.1%	$\Delta V_o = \pm 20V$	$A_V = 1$		2.3	3.0	μs
			$A_V = 10$		2.7	3.5	
			$A_V = 100$		3.1	4.0	
	Gain Switching Time				3.5		
E_N	Equivalent Input Noise Voltage (*Figure 3*)	BW = 0.1 Hz-10 Hz	$A_V = 100$		7		μVp-p
		BW = 10 Hz-10 kHz			1.4		μVrms
I_N	Equivalent Input Noise Current (*Figure 3*)	BW = 10 Hz-10 kHz			30		pArms

Note 1: Improper supply power-on sequence may damage the device. See Power Supply Connection section under Applications Information.

Note 2: For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

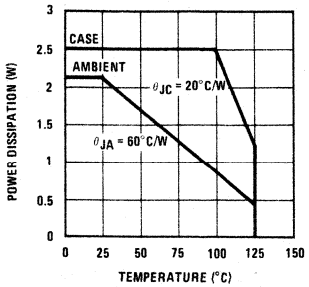
Note 3: Due to limited production test time, these parameters are specified at junction temperature, T_J. In normal operation the junction temperature rises above the ambient temperature, T_A, as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

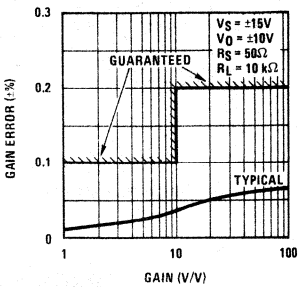
Note 5: The AC parameters are not 100% tested, but an estimated 90% of all devices meet these limits.

Typical Performance Characteristics

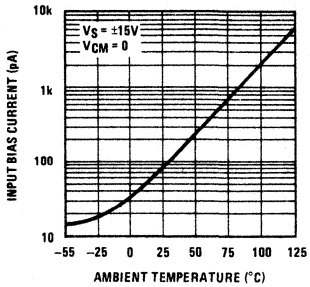
Power Dissipation



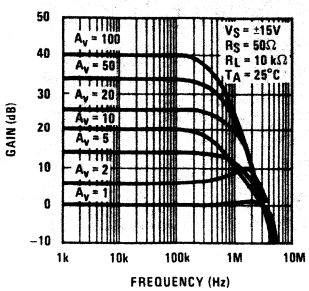
Gain Accuracy



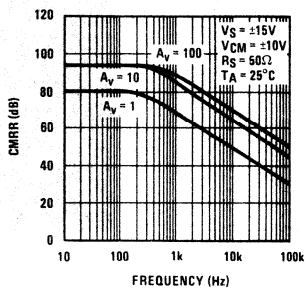
Input Bias Current



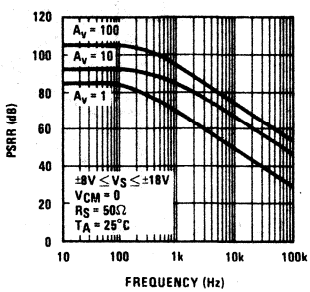
Small Signal Frequency Response



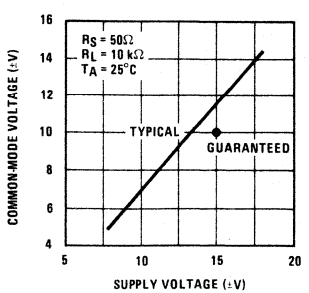
Common-Mode Rejection



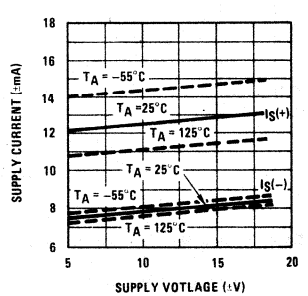
Power Supply Rejection



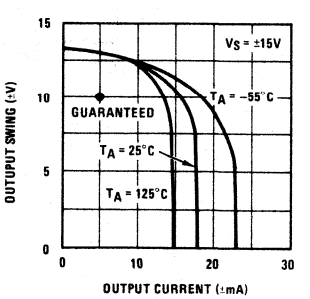
Input Common-Mode Range



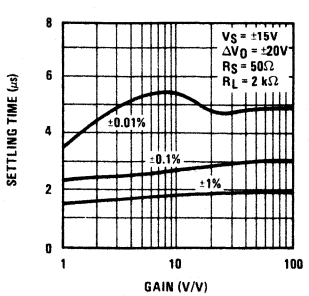
Supply Current



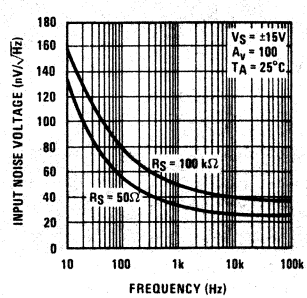
Output Swing



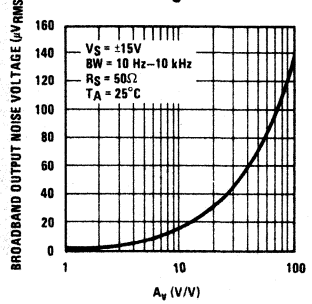
Settling Time



Equivalent Input Noise Voltage (Includes Source-Resistance Noise)



Broadband Output Noise Voltage



AC Test Circuits

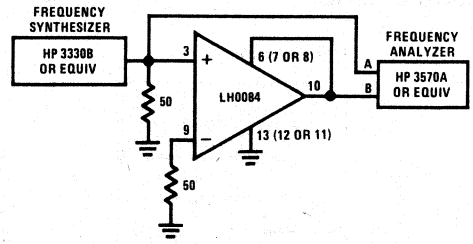


FIGURE 1. Frequency Response Measurement Circuit

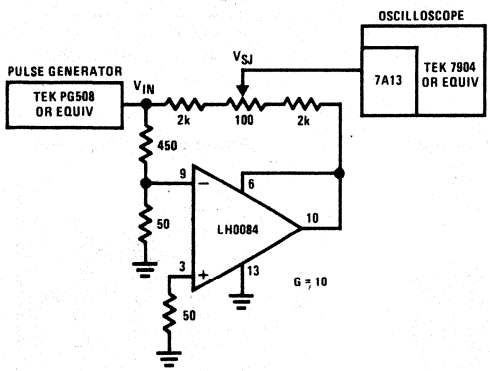
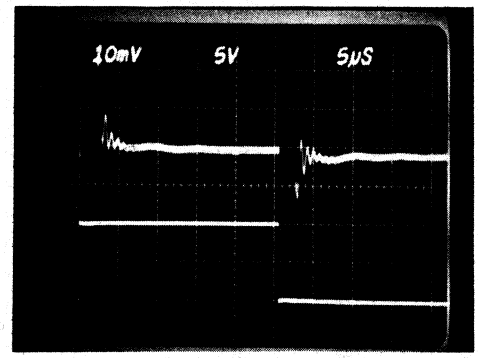


FIGURE 2. Settling Time Measurement Circuit

Settling Time



$A_V = 10$ Input Stage

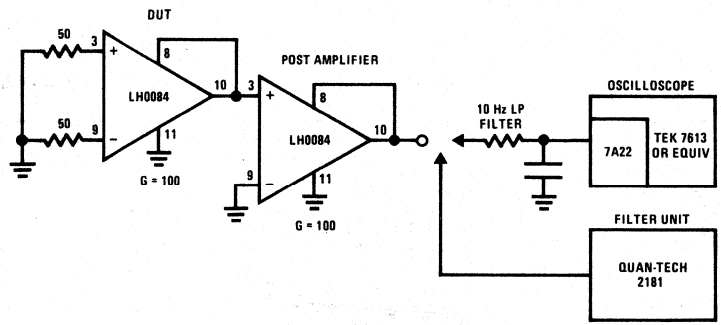
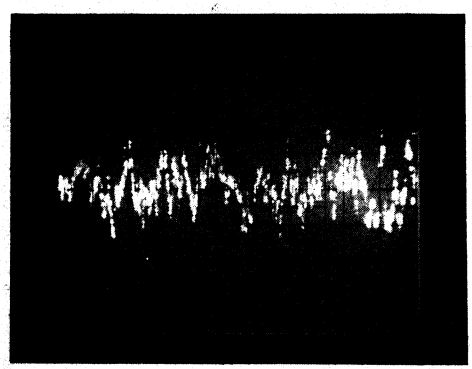


FIGURE 3. Noise Measurement Circuit

Wideband Noise



$R_S = 50\Omega$ Bandwidth 0.1 Hz to 10 Hz
1μV/Division Vertical 5 Seconds/Division Horizontal

Applications Information

THEORY OF OPERATION

The LH0084 is a digitally-programmable-gain true-instrumentation amplifier composed of a variable-gain voltage-follower input stage (A1 and A2), followed by a differential output stage (A3). The schematic is shown in *Figure 4.*

The input stage contains matched high-speed FET-input op amps (A1 and A2). A high-stability temperature-compensated resistor network (R1 through R7) controls feedback ratios at the inverting inputs of op amps A1 and A2 via FET switches S1A-S4A and S1B-S4B. Since the FET switches are in series with the op amp input impedance their resistance match and temperature drift do not degrade the gain accuracy of the instrumentation amplifier. The FET switches are controlled through a 1-of-4 decoder and switch driver, by the logic levels applied at the digital input terminals D1 and D0 and set the gain of the input stage as shown in Table I.

If, for example, D1 is High (≥2.0V) and D0 is Low (≤0.7V), FET switch pair S3A and S3B will be closed (and all remaining switches open). The input stage gain, $A_{V(1)}$, can then be shown to be:

$$A_{V(1)} = \frac{V2 - V1}{V_{IN}(+) - V_{IN}(-)}$$

$$= 1 + \frac{R4 + R5 + R6 + R7}{R1 + R2 + R3} \qquad (1)$$

$$= 1 + \frac{6k + 6k + 10k + 10k}{4k + 2k + 2k}$$

$$= 5$$

Schematic Diagram

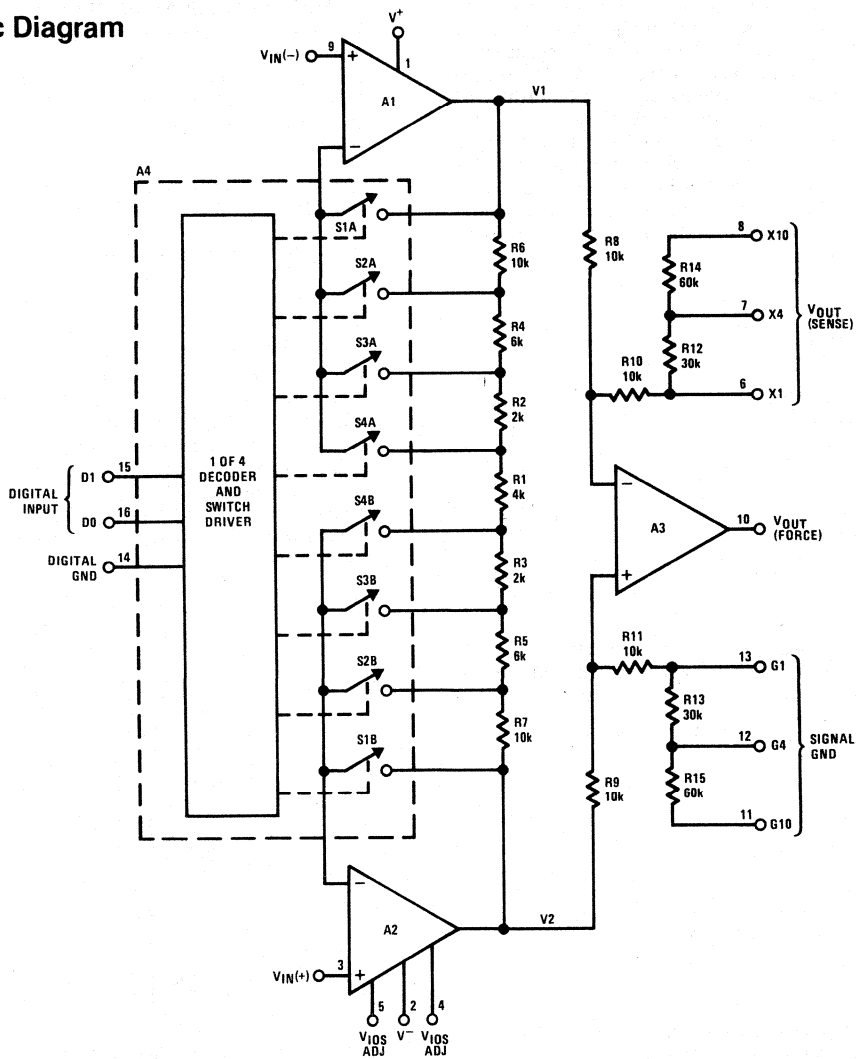


FIGURE 4

Applications Information (Continued)

TABLE I. GAIN TRUTH TABLE AND CONNECTION TABLE

Digital Inputs		1st Stage Gain	Pin Connections	2nd Stage Gain	Overall Gain
D1	D0	$A_{V(1)}$		$A_{V(2)}$	A_V
0	0	1	6-10, 13-GND	1	1
0	1	2			2
1	0	5			5
1	1	10			10
0	0	1	7-10, 12-GND	4	4
0	1	2			8
1	0	5			20
1	1	10			40
0	0	1	8-10, 11-GND	10	10
0	1	2			20
1	0	5			50
1	1	10			100

The output stage, consisting of op amp A3 and resistors R8 through R15, converts the voltage difference at the output of the input stage, V2 minus V1, to a single-ended output. For increased flexibility of the LH0084, the output stage gain is pin-strappable by selecting R10, R10 + R12, or R10 + R12 + R14 as feedback resistor for A3. The ratios of these resistors to the differential stage input resistor R3 are kept very accurate to maintain the excellent overall gain accuracy of the device. The output stage gain, $A_{V(2)}$, is equal to the feedback resistance divided by the input resistance. Thus with, for example, Pin 7 wired to Pin 10, that gain would be:

$$A_{V(2)} = \frac{V_{OUT}}{V2 - V1}$$

$$= \frac{R10 + R12}{R8} \qquad (2)$$

$$= \frac{10k + 30k}{10k}$$

$$= 4$$

To preserve the high common-mode rejection ratio of the output stage, the ground sense resistor, R11, R11 + R13 or R11 + R13 + R15, must match the feedback resistor used.

The overall gain of the LH0084 is therefore:

$$A_V = \frac{V_{OUT}}{V_{IN}(+) - V_{IN}(-)}$$

$$= \frac{V2 - V1}{V_{IN}(+) - V_{IN}(-)} \cdot \frac{V_{OUT}}{V2 - V1} \qquad (3)$$

$$= A_{V(1)} \cdot A_{V(2)}$$

The different gains available are in the range of 1 through 100 and are summarized in Table I.

POWER SUPPLY CONNECTIONS

Proper power supply connections are shown in *Figure 5*. The power supplies should be bypassed to ground as close as possible to device supply pins. For optimum high speed performance V^+ and V^- should be decoupled with a 0.01 μF ceramic disc in parallel with a 1 μF electrolytic capacitor.

The two ground pins, analog and digital grounds, should be connected together as close to the device as possible, preferably with a ground plane underneath the device. If this is not possible, the grounds should be connected together locally with back-to-back diodes and hard-wired together off-board. If a ground reference offset is used, it must be low impedance compared to the ground sense resistance to avoid CMRR degradation.

Care must be taken in the supply power-on sequence. The LH0084 may suffer irreversible damage if the V^+ supply is applied prior to the powering on of the V^- supply. In most applications using dual tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V^- pin as shown in *Figure 5*.

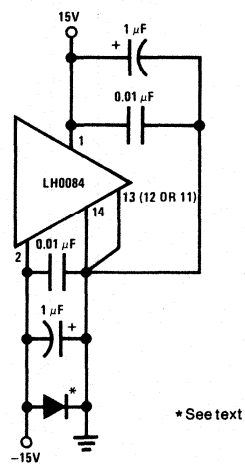


FIGURE 5. Power Supply Connections

Applications Information (Continued)

SIGNAL CONNECTIONS

The input signals should be connected as shown in *Figure 6.* To minimize errors, $R_S(+)$, $R_S(-)$ and R_{CM} should be kept as small as possible.

The output connections are also shown in *Figure 6.* The feedback leads should be kept short as should the ground sense in order to minimize lead resistance and parasitic capacitance.

OFFSET AND GAIN ADJUSTMENTS

Special care must be taken when using external offset adjustment. Since the LH0084 is a 2-stage amplifier with each stage contributing offset errors, and the amplifier presumably is used at several different gains, it is important to realize that the offsets of both the 1st and the 2nd stages must be nulled to maintain zero offset referred to output (RTO) at all gain settings.

In general, it is recommended that the input stage offset (V_{IOS}) be adjusted with a potentiometer as shown in *Figure 7.* The output stage offset (V_{OOS}) is ideally adjusted at a subsequent gain stage (i.e. sample-and-hold or A-to-D converter), but if this is impractical, it may also be done as shown in *Figure 7.*

Recommended offset adjust procedure is as follows: Initially set both pots to center positions and short both inputs of the LH0084 to ground.

a) Set the input stage gain to 1 (pull D1 and D0 low). Measure the output voltage, V_{OUT1}.

b) Set the input stage gain to 10 (pull D1 and D0 high). Measure the new output voltage, V_{OUT2}.

c) Calculate the portion of V_{OUT2} contributed by the output stage offset per the equation:

$$V_{OOS} = \frac{1}{9}(10 \cdot V_{OUT1} - V_{OUT2}) \qquad (4)$$

d) While maintaining an input stage gain of 10, adjust the input offset voltage (V_{IOS}) potentiometer until the output voltage is equal to the voltage calculated in Equation (4).

e) Change the input back to a gain of 1 and adjust the output offset voltage (V_{OOS}) potentiometer until the output voltage is zero.

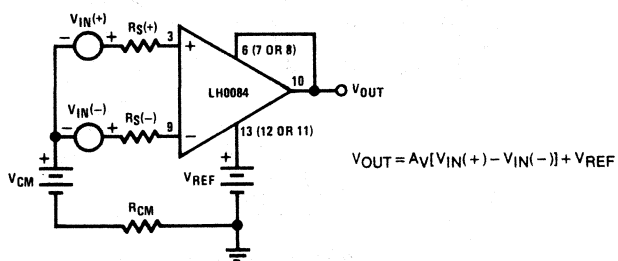


FIGURE 6. Signal Connections

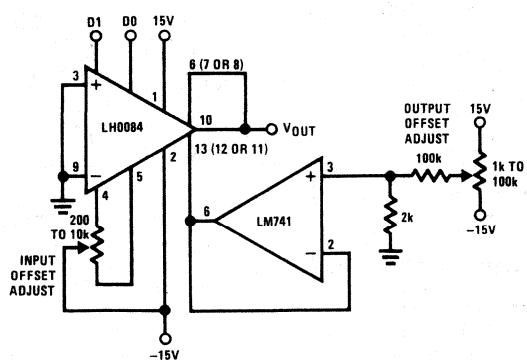


FIGURE 7. Offset Adjust Circuit

Applications Information (Continued)

An alternate offset adjust scheme is shown in *Figure 8*. The offset should be rezeroed after each time the gain is changed or when the op amp integrator drift warrants a new zero pulse. An additional advantage of this adjustment technique is that it can also be used to cancel out offset voltage drift and common-mode voltage error contributions.

External gain adjustment is generally discouraged since gain accuracy can be optimized for one gain setting only. If gain adjustment is required, however, it should be done at a subsequent gain stage.

LOGIC CONNECTIONS

The digital inputs D1 and D0 are referenced to the digital ground. The device interfaces directly to TTL and, with pull-down resistors, to CMOS.

Interfacing with microprocessors will usually require a latch. A circuit using full 6-bit wide address decode and write strobe is shown in *Figure 9*.

REMOTE OUTPUT SENSE

The feedback resistors of the LH0084 can be connected directly at the load in order to eliminate errors due to lead resistance (*Figure 10*).

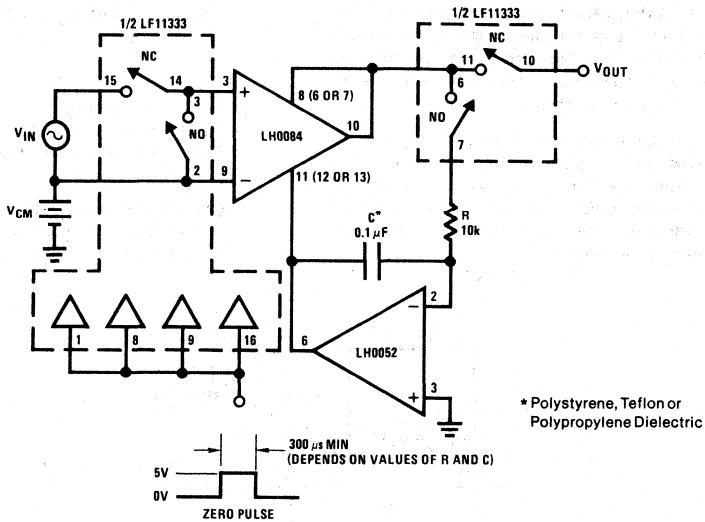


FIGURE 8. Auto Zero Circuit

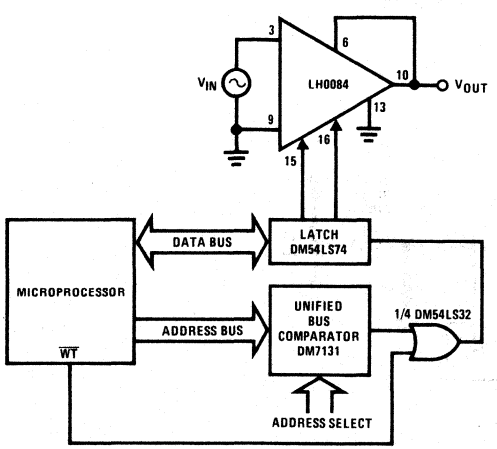


FIGURE 9. Typical Microprocessor Interface

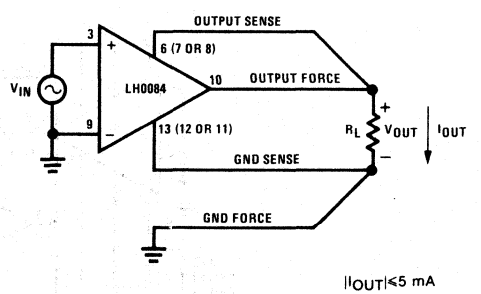


FIGURE 10. Remote Sense Connection

Applications Information (Continued)

Also a unity gain buffer, such as the LH0033, may be included in the feedback loop for increased current drive capability as shown in *Figure 11.*

The output sense feature can also be used in other ways such as output offset, *Figure 12*, or current source output, *Figure 13.*

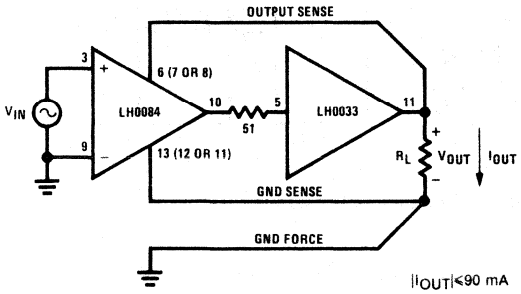


FIGURE 11. Buffered Output Connection

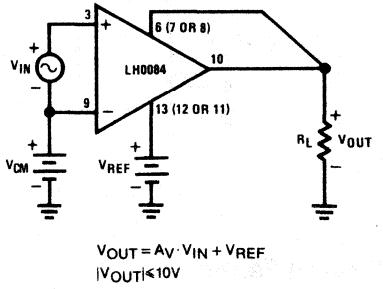


FIGURE 12. Output Offset Connection

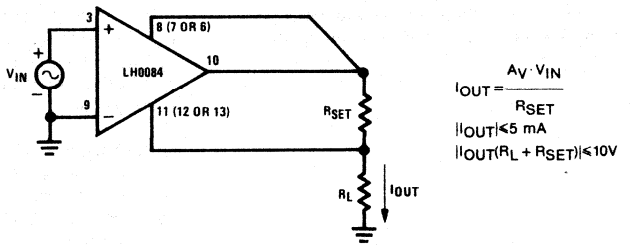


FIGURE 13. Output Current Source Connection

Applications

The LH0084 is ideal for application in increased dynamic range A-to-D converters, test systems, process control, and multi-channel data acquisition systems. *Figure 14* shows the device used in a typical data acquisition system.

A software offset and gain error correction scheme is shown in *Figure 15.* By first selecting a multiplexer input connected to analog ground, and then selecting a channel connected to a reference of known value, the overall system gain and offset errors can be calculated. For all subsequent readings, offset and gain corrections can be made mathematically by solving a simple first-order equation in software.

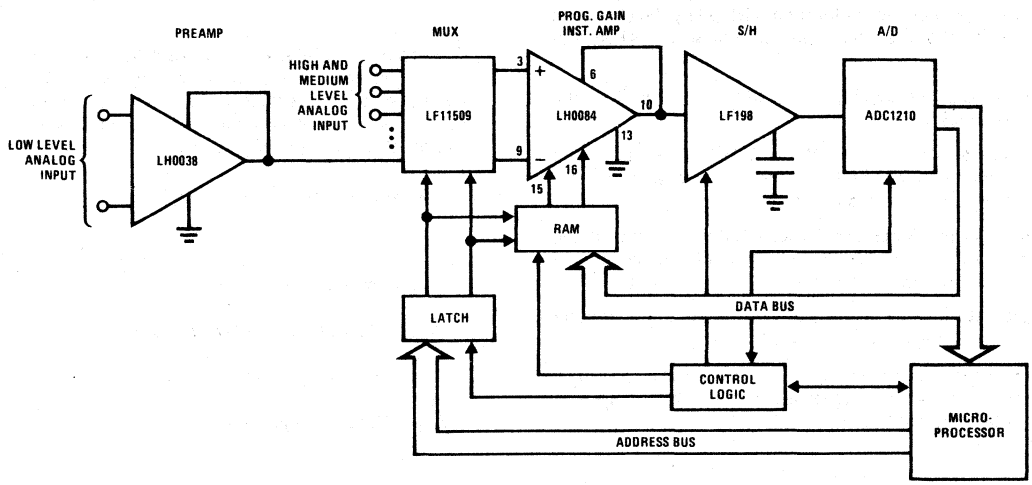


FIGURE 14. Typical Data Acquisition System

Applications (Continued)

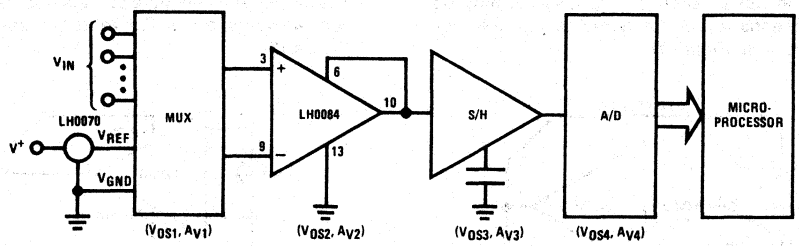


FIGURE 15. Software System Offset and Gain Calibration Circuit

Definition of Terms

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the output of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and using the following equation:

$$V_{IOS} = \frac{1}{9}\left(V_{OS}\Big|_{A_V=10} - V_{OS}\Big|_{A_V=1}\right)$$

where:

$V_{OS}\Big|_{A_V=10}$ = Overall offset (RTO) for $A_V = 10$

$V_{OS}\Big|_{A_V=1}$ = Overall offset (RTO) for $A_V = 1$

Input Offset Current, I_{OS}: The difference in the currents into the 2 analog input terminals at 0V.

Input Bias Current, I_B: The average of the currents into the 2 analog input terminals at 0V.

Input Resistance, R_{IN}: Common-mode input resistance is the change in input voltage range divided by the change in input bias current with both analog inputs at the same voltage. Differential input resistance is the change in input voltage at one input terminal divided by the change in input current at the other input terminal which is kept still at 0V.

Input Voltage Range, V_{IN}: The voltage range for which the device is operational.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the change in input offset voltage over this range.

Power Supply Rejection Ratio, PSRR: The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

Voltage Gain, A_V: The ratio of output voltage change to the input voltage change producing it.

Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full-scale (10V for operation with ±15V supply). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage for the output to be forced to 0V. V_{OOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and applying the following equation:

$$V_{OOS} = \frac{1}{9}\left(10 \cdot V_{OS}\Big|_{A_V=1} - V_{OS}\Big|_{A_V=10}\right)$$

where:

$V_{OS}\Big|_{A_V=1}$ = Overall offset (RTO) for $A_V = 1$

$V_{OS}\Big|_{A_V=10}$ = Overall offset (RTO) for $A_V = 10$

Offset Voltage (Referred to Output), $V_{OS(RTO)}$: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input offset voltage, V_{IOS}, and output offset voltage, V_{OOS}, and is a function of amplifier gain. The overall offset voltage is given by:

$$V_{OS(RTO)} = A_{V(2)}(A_{V(1)}\, V_{IOS} + V_{OOS})$$

where:

V_{IOS} = Input offset voltage

V_{OOS} = Output stage offset voltage

$A_{V(1)}$ = Input stage gain

$A_{V(2)}$ = Output stage gain

Definition of Terms (Continued)

Output Voltage Swing, V_O: The peak output voltage swing referenced to ground into specified load.

Output Short-Circuit Current, I_O: The current supplied by the device with the output connected directly to ground.

Output Resistance, r_o: The ratio of change in output voltage to change in output current around zero output.

Supply Voltage Range, V_S: The supply voltage range for which the device is operational.

Supply Current, I_S: The current required from the supply to operate the device with zero load and with the analog as well as the digital inputs at 0V.

Power Dissipation, P_D: The power dissipated in the device with zero load and with the analog as well as the digital inputs at 0V.

Digital "1" Input Voltage, V_{IH}: Minimum voltage required at the digital input to guarantee a high logic state.

Digital "0" Input Voltage, V_{IL}: Maximum voltage required at the digital input to guarantee a low logic state.

Digital "1" Input Current, I_{IH}: The current into a digital input at specified logic level.

Digital "0" Input Current, I_{IL}: The current into a digital input at specified logic level.

Average Input Offset Voltage Drift, $\Delta V_{IOS}/\Delta T$: The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Output Offset Voltage Drift, $\Delta V_{OOS}/\Delta T$: The ratio of output offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Gain Temperature Coefficient, $\Delta A_V/\Delta T$: The ratio of change in gain from 25°C to either temperature extreme divided by the temperature range.

Small Signal Bandwidth, BW: The frequency at which the device gain changes from the low frequency gain by a specified amount.

Power Bandwidth, PBW: Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion.

Slew Rate, SR: The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

Settling Time, t_s: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Gain Switching Time: The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

Equivalent Input Noise Voltage, E_N: The rms or peak noise voltage referred to the input (RTI) over a specified frequency band.

Equivalent Input Noise Current, I_N: The rms or peak noise current referred to the input (RTI) over a specified frequency band.

National Semiconductor

LM10/LM10B(L)/LM10C(L) Op Amp and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV. Some other characteristics of the LM10 are

- input-offset voltage 2.0 mV (max)
- input-offset current 0.7 nA (max)
- input-bias current 20 nA (max)
- reference regulation 0.1% (max)
- offset-voltage drift 2μV/°C
- reference drift 0.002%/°C

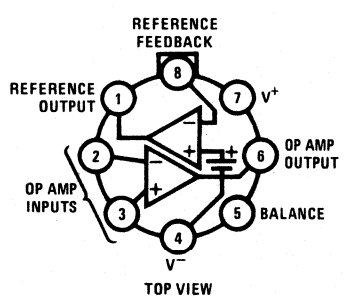
The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

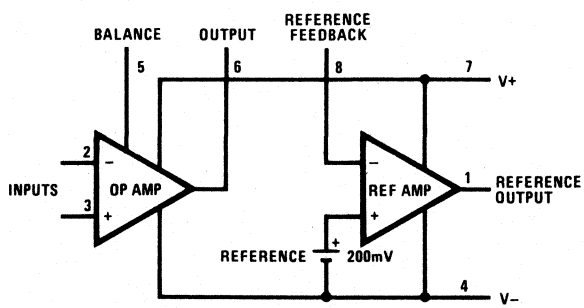
This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Connection and Functional Diagrams

Metal Can Package (H)



Order Number LM10H, LM10BH, LM10CH, LM10BLH or LM10CLH
See NS Package H08A



Absolute Maximum Ratings

	LM10/LM10B/LM10C	LM10BL/LM10CL
Total supply voltage	45V	7V
Differential input voltage (note 1)	±40V	±7V
Power dissipation (note 2)	internally limited	
Output short-circuit duration (note 3)	indefinite	
Storage-temperature range	−55°C to +150°C	
Lead temperature (soldering, 10s)	300°C	

Electrical Characteristics ($T_J = 25°C$, $T_{MIN} \leq T_J \leq T_{MAX}$, note 4)

(Boldface type refers to limits over temperature range.)

PARAMETER	CONDITIONS	LM10/LM10B			LM10C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input offset voltage			0.3	2.0 **3.0**		0.5	4.0 **5.0**	mV mV
Input offset current (note 5)			0.25	0.7 **1.5**		0.4	2.0 **3.0**	nA nA
Input bias current			10	20 **30**		12	30 **40**	nA nA
Input resistance		250 **150**	500		150 **115**	400		kΩ kΩ
Large signal voltage ga..	V_S = ±20V, I_{OUT} = 0 V_{OUT} = ±19.95V	120 **80**	400		80 **50**	400		V/mV V/mV
	V_S = ±20V, V_{OUT} = ±19.4V I_{OUT} = ±20 mA (**±15 mA**)	50 **20**	130		25 **15**	130		V/mV V/mV
	V_S = ±0.6V (**0.65V**), I_{OUT} = ±2 mA V_{OUT} = ±0.4V (**±0.3V**), V_{CM} = −0.4V	1.5 **0.5**	3.0		1.0 **0.75**	3.0		V/mV V/mV
Shunt gain (note 6)	1.2V (**1.3V**) ≤ V_{OUT} ≤ 40V, R_L = 1.1 kΩ 0.1 mA ≤ I_{OUT} ≤ 5 mA	14 **6**	33		10 **6**	33		V/mV V/mV
	1.5V ≤ V^+ ≤ 40V, R_L = 250Ω 0.1 mA ≤ I_{OUT} ≤ 20 mA	8 **4**	25		6 **4**	25		V/mV V/mV
Common-mode rejection	−20V ≤ V_{CM} ≤ 19.15V (**19V**) V_S = ±20V	93 **87**	102		90 **87**	102		dB dB
Supply-voltage rejection	−0.2V ≥ V^- ≥ −39V V^+ = 1.0V (**1.1V**)	90 **84**	96		87 **84**	96		dB dB
	1.0V (**1.1V**) ≤ V^+ ≤ 39.8V V^- = −0.2V	96 **90**	106		93 **90**	106		dB dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift	T_C < 100°C		60			90		pA/°C
Line regulation	1.2V (**1.3V**) ≤ V_S ≤ 40V 0 ≤ I_{REF} ≤ 1.0 mA, V_{REF} = 200 mV		0.001	0.003 **0.006**		0.001	0.008 **0.01**	%/V %/V
Load regulation	0 ≤ I_{REF} ≤ 1.0 mA $V^+ - V_{REF} \geq$ 1.0V (**1.1V**)		0.01	0.1 **0.15**		0.01	0.15 **0.2**	% %
Amplifier gain	0.2V ≤ V_{REF} ≤ 35V	50 **23**	75		25 **15**	70		V/mV V/mV
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			270	400 **500**		300	500 **570**	μA μA
Supply current change	1.2V (**1.3V**) ≤ V_S ≤ 40V		15	**75**		15	**75**	μA

Electrical Characteristics ($T_J = 25°C$, $T_{MIN} \leq T_J \leq T_{MAX}$, note 4)

(Boldface type refers to limits over temperature range.)

PARAMETER	CONDITIONS	LM10BL			LM10CL			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input offset voltage			0.3	2.0		0.5	4.0	mV
				3.0			**5.0**	mV
Input offset current			0.1	0.7		0.2	2.0	nA
(note 5)				**1.5**			**3.0**	nA
Input bias current			10	20		12	30	nA
				30			**40**	nA
Input resistance		250	500		150	400		kΩ
		150			**115**			kΩ
Large signal voltage gain	$V_S = \pm 3.25V$, $I_{OUT} = 0$	60	300		40	300		V/mV
	$V_{OUT} = \pm 3.2V$	**40**			**25**			V/mV
	$V_S = \pm 3.25V$, $I_{OUT} = 10$ mA	10	25		5	25		V/mV
	$V_{OUT} = \pm 2.75V$	4			3			V/mV
	$V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA	1.5	3.0		1.0	3.0		V/mV
	$V_{OUT} = \pm 0.4V$ **(±0.3V)**, $V_{CM} = -0.4V$	**0.5**			**0.75**			V/mV
Shunt gain (note 6)	$1.5V \leq V^+ \leq 6.5V$, $R_L = 500\Omega$	8	30		6	30		V/mV
	$0.1 \text{ mA} \leq I_{OUT} \leq 10$ mA	4			4			V/mV
Common-mode rejection	$-3.25V \leq V_{CM} \leq 2.4V$ **(2.25V)**	89	102		80	102		dB
	$V_S = \pm 3.25V$	**83**						dB
Supply-voltage rejection	$-0.2V \geq V^- \geq -5.4V$	86	96		80	96		dB
	$V^+ = 1.0V$ **(1.2V)**	**80**						dB
	1.0V **(1.1V)** $\leq V^+ \leq 6.3V$	94	106		80	106		dB
	$V^- = 0.2V$	**88**						dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift			60			90		pA/°C
Line regulation	1.2V **(1.3V)** $\leq V_S \leq 6.5V$		0.001	0.01		0.001	0.02	%/V
	$0 \leq I_{REF} \leq 0.5$ mA, $V_{REF} = 200$ mV			**0.02**			**0.03**	%/V
Load regulation	$0 \leq I_{REF} \leq 0.5$ mA		0.01	0.1		0.01	0.15	%
	$V^+ - V_{REF} \geq 1.0V$ **(1.1V)**			**0.15**			**0.2**	%
Amplifier gain	$0.2V \leq V_{REF} \leq 5.5V$	30	70		20	70		V/mV
		20			**15**			V/mV
Feedback sense voltage		195	200	205	190	200	210	mV
		194		**206**	**189**		**211**	mV
Feedback current			20	50		22	75	nA
				65			**90**	nA
Reference drift			0.002			0.003		%/°C
Supply current			260	400		280	500	μA
				500			**570**	μA

Note 1: The input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.

Note 2: The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

Note 3: Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

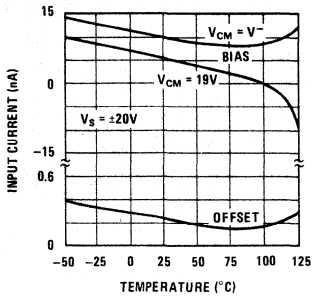
Note 4: These specifications apply for $V^- \leq V_{CM} \leq V^+ - 0.85V$ **(1.0V)**, 1.2V **(1.3V)** $< V_S \leq V_{MAX}$, $V_{REF} = 0.2V$ and $0 \leq I_{REF} \leq 1.0$ mA, unless otherwise specified: $V_{MAX} = 40V$ for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation**; this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \cong 20$ ms), die heating ($\tau_2 \cong 0.2$s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

Note 5: For $T_J > 90°C$, I_{OS} may exceed 1.5 nA for $V_{CM} = V^-$. With $T_J = 125°C$ and $V^- \leq V_{CM} \leq V^- + 0.1V$, $I_{OS} \leq 5$ nA.

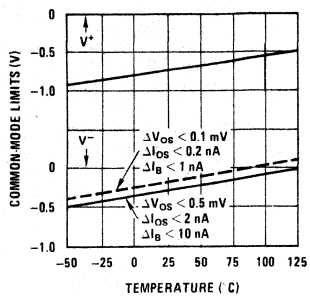
Note 6: This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Typical Performance Characteristics (Op Amp)

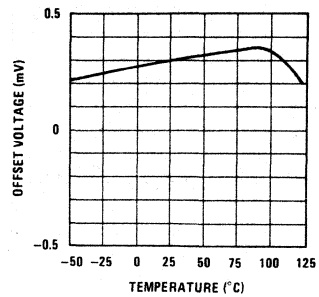
input current



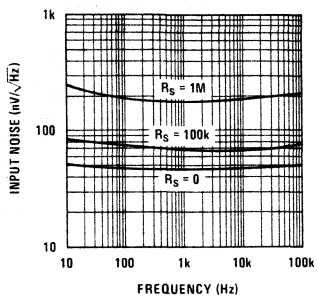
common mode limits



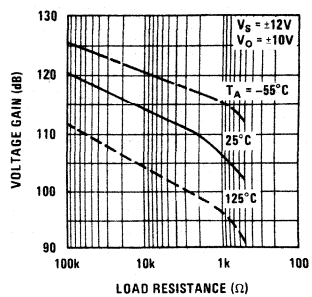
offset voltage drift



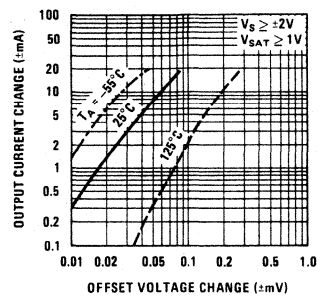
input noise voltage



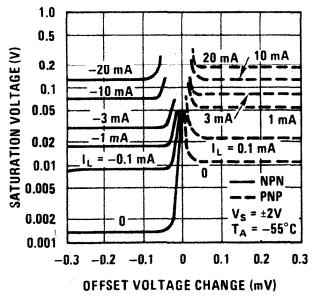
dc voltage gain



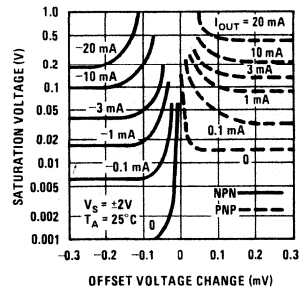
transconductance



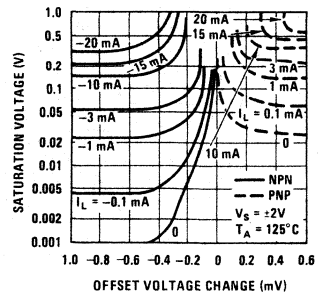
output saturation characteristics



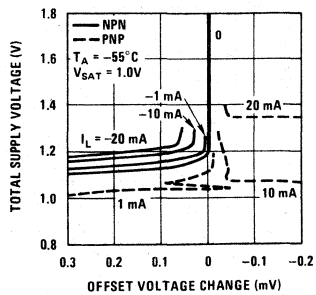
output saturation characteristics



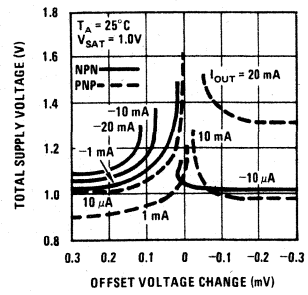
output saturation characteristics



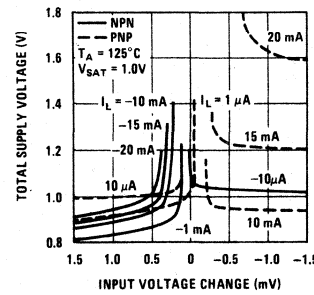
minimum supply voltage



minimum supply voltage

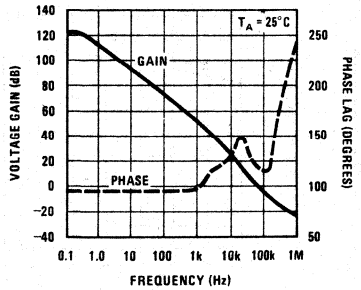


minimum supply voltage

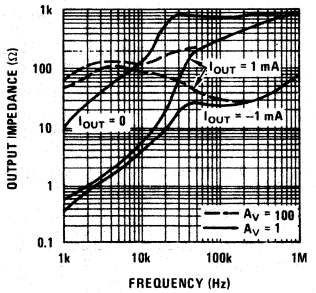


Typical Performance Characteristics (Op Amp)

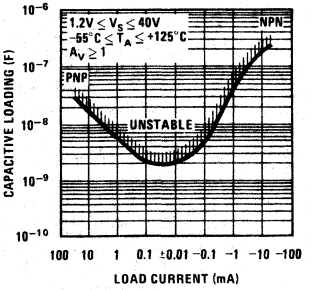
frequency response



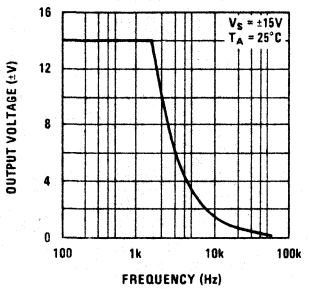
output impedance



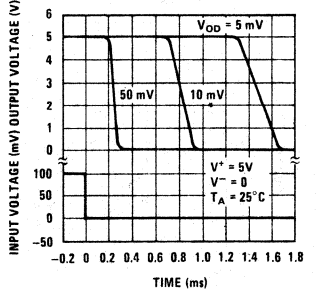
typical stability range



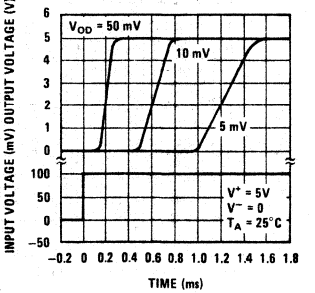
large signal response



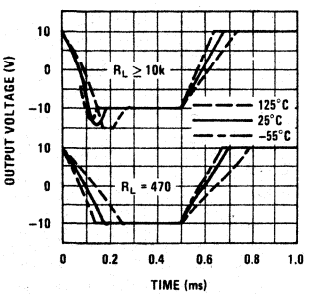
comparator response time for various input overdrives



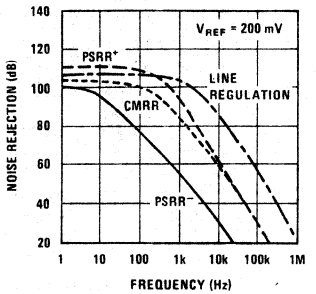
comparator response time for various input overdrives



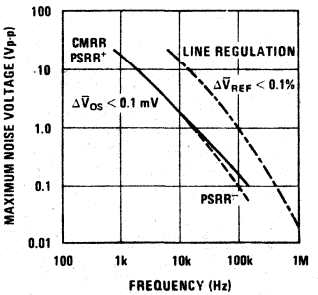
follower pulse response



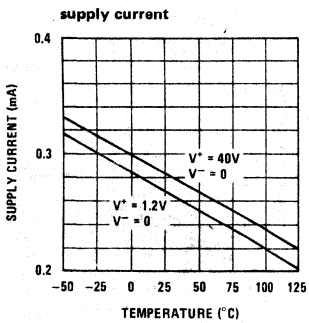
noise rejection



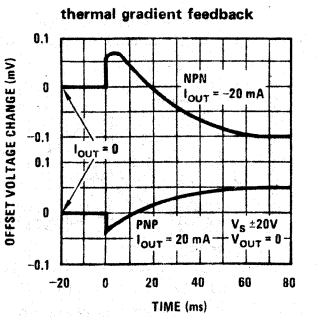
rejection slew limiting



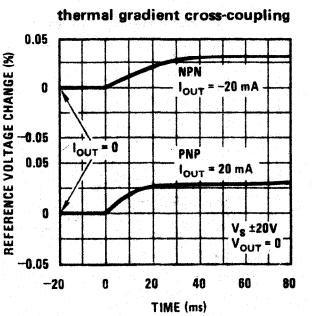
supply current



thermal gradient feedback

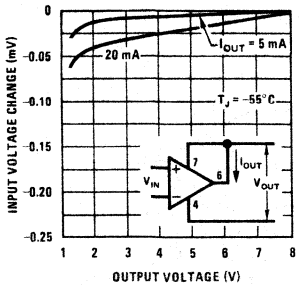


thermal gradient cross-coupling

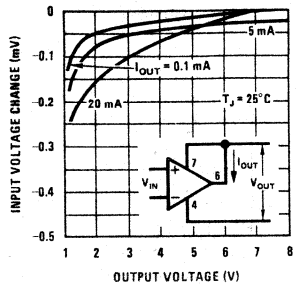


Typical Performance Characteristics (Op Amp)

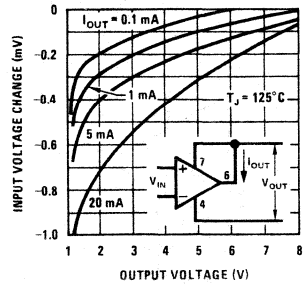
shunt gain



shunt gain

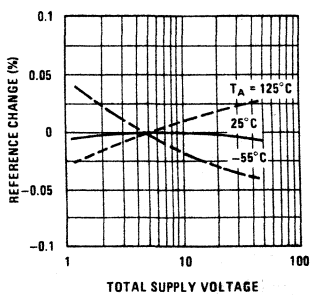


shunt gain

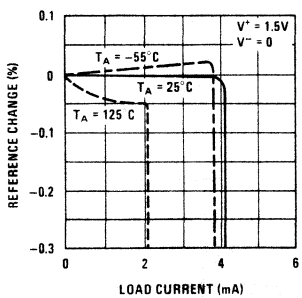


Typical Performance Characteristics (Reference)

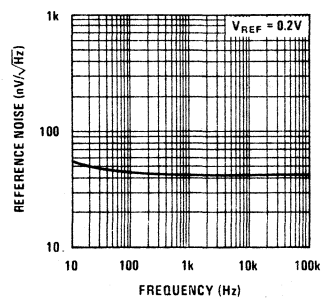
line regulation



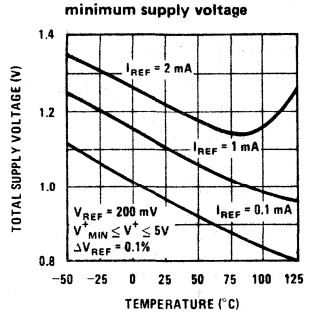
load regulation



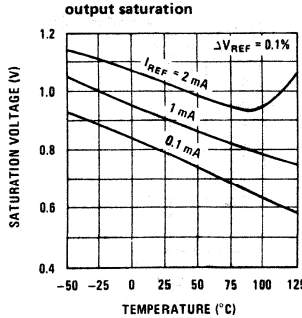
reference noise voltage



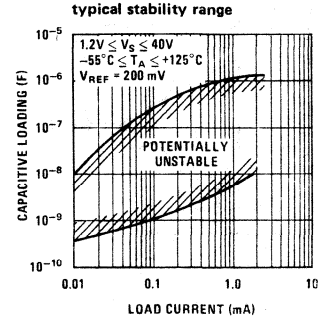
minimum supply voltage



output saturation



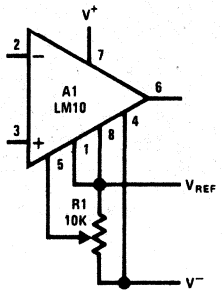
typical stability range



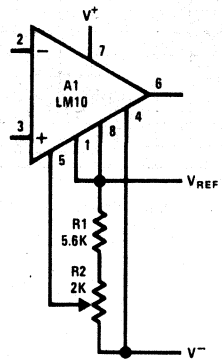
Typical Applications††

op amp offset adjustment

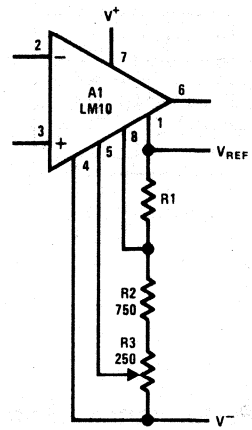
standard



limited range

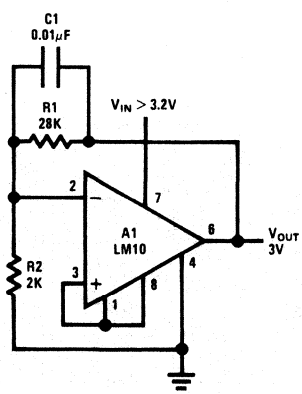


limited range with boosted reference

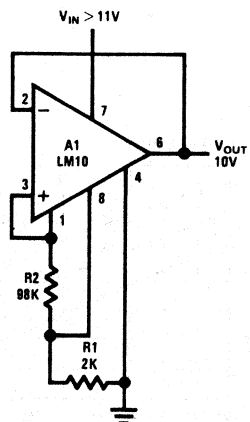


positive regulators†

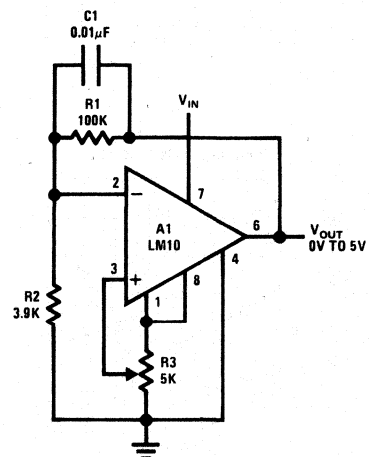
low voltage



best regulation



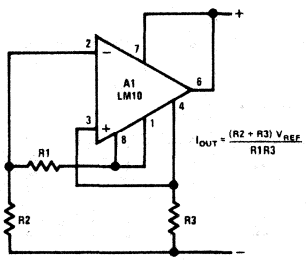
zero output



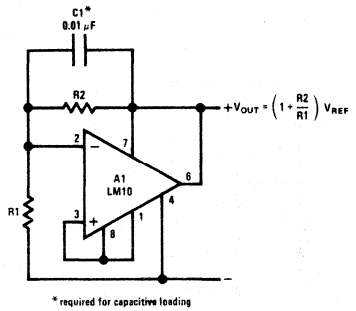
†Use only electrolytic output capacitors.
††Circuit descriptions available in application note AN-211.

Typical Applications ††

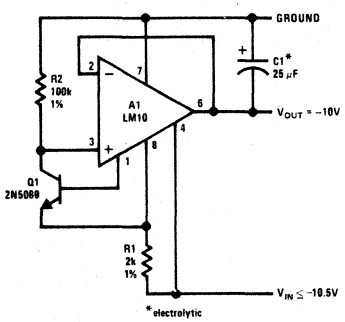
current regulator



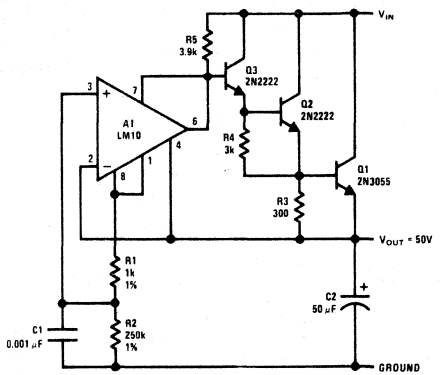
shunt regulator



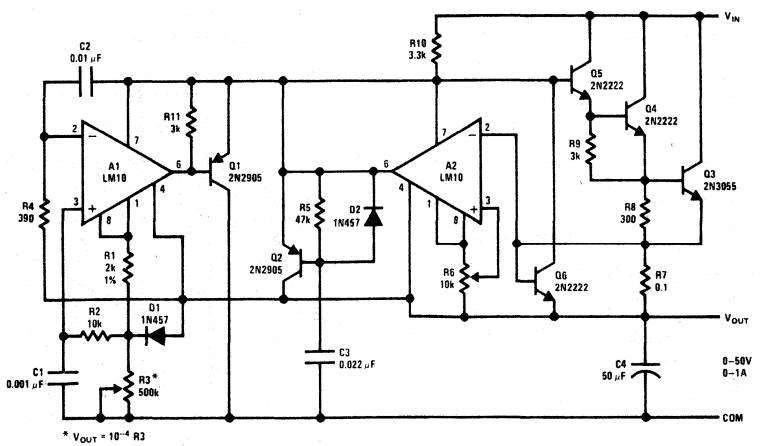
negative regulator



precision regulator



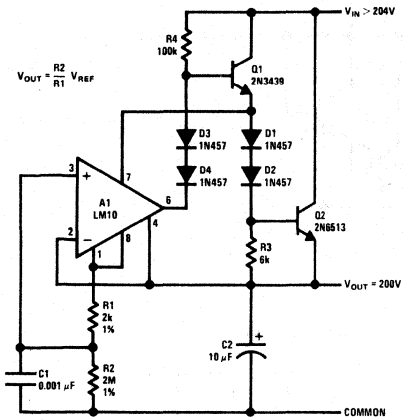
laboratory power supply



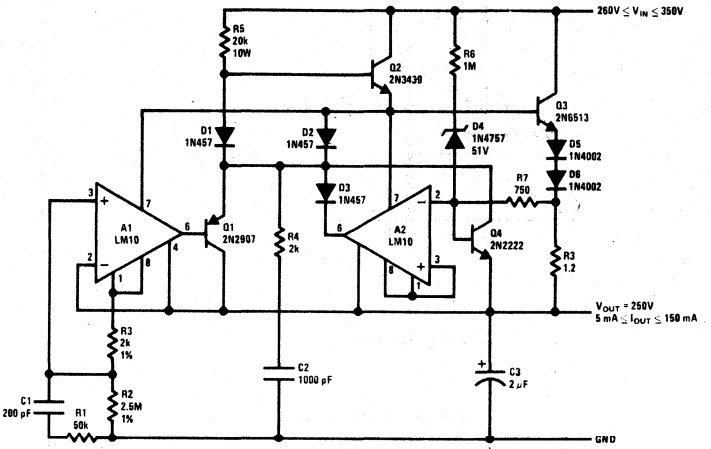
††Circuit descriptions available in application note AN-211.

Typical Applications ††

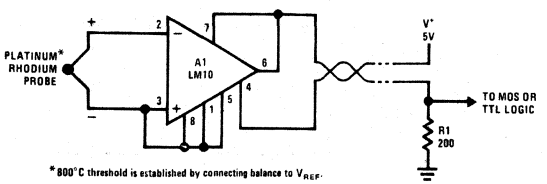
hv regulator



protected hv regulator

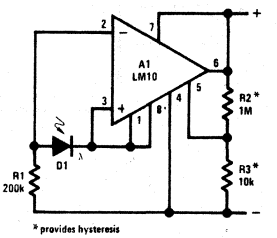


flame detector



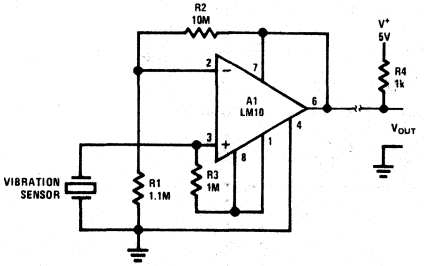
*800°C threshold is established by connecting balance to V_{REF}.

light level sensor

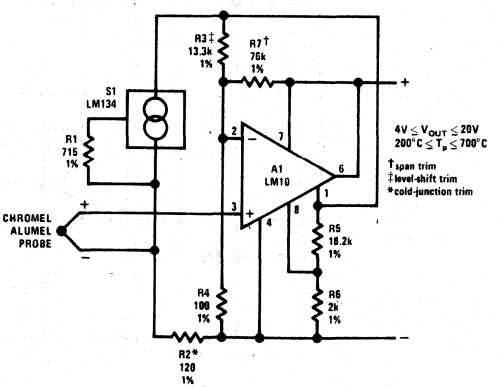


*provides hysteresis

remote amplifier



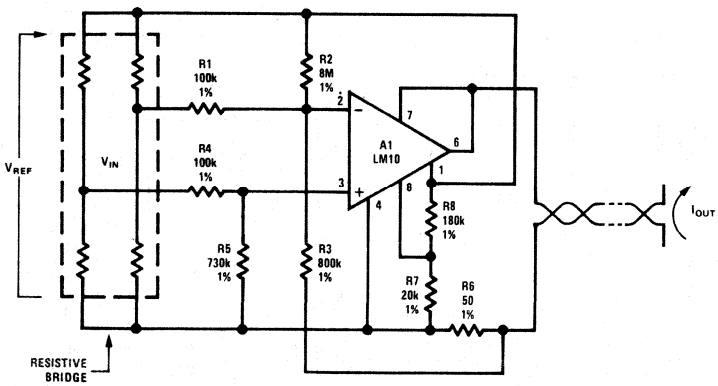
remote thermocouple amplifier



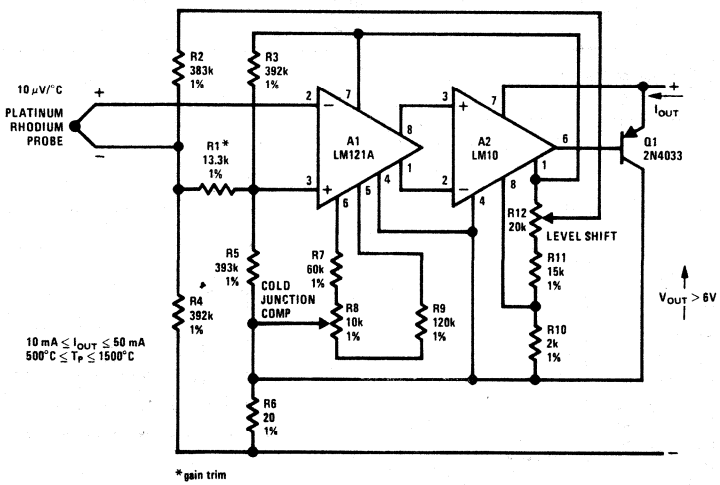
††Circuit descriptions available in application note AN-211.

Typical Applications ††

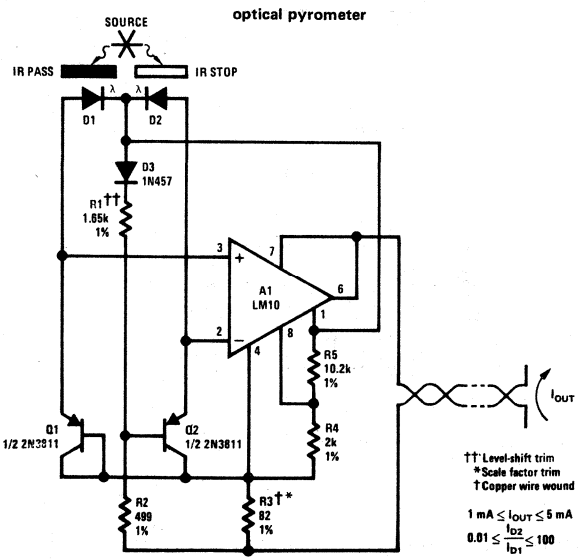
transmitter for bridge sensor



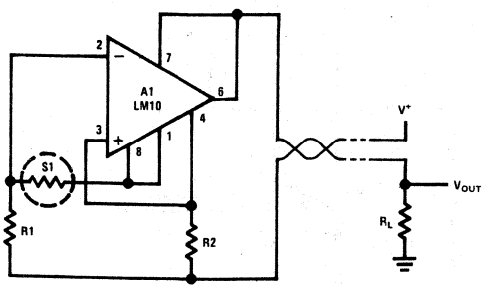
precision thermocouple transmitter



optical pyrometer



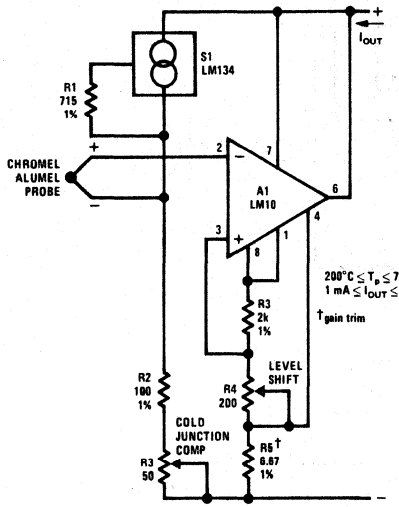
resistance thermometer transmitter



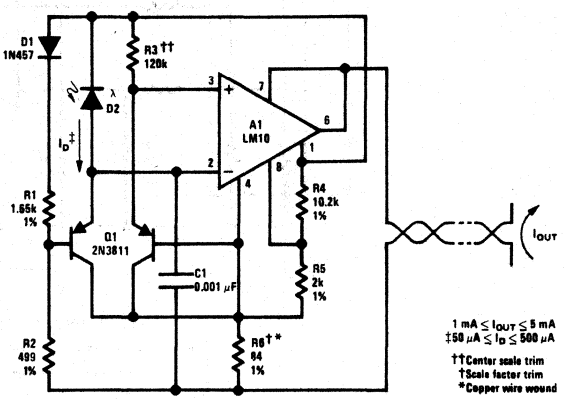
††Circuit descriptions available in application note AN-211.

Typical Applications ††

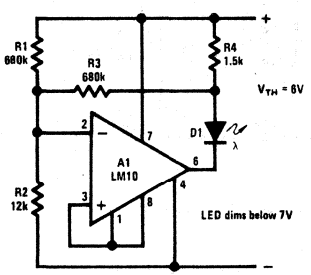
thermocouple transmitter



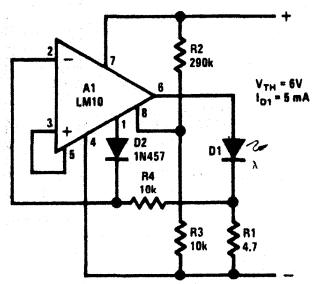
logarithmic light sensor



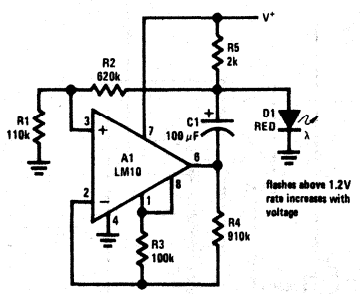
battery-level indicator



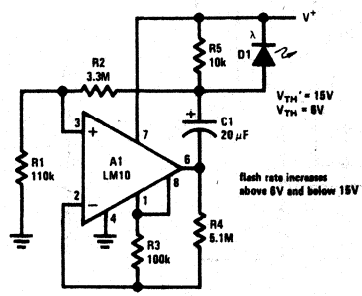
battery-threshold indicator



single-cell voltage monitor



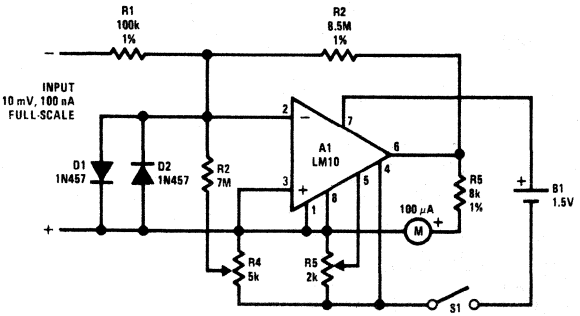
double-ended voltage monitor



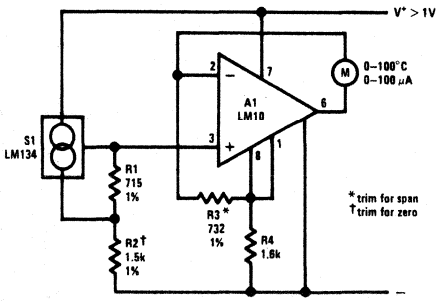
††Circuit descriptions available in application note AN-211.

Typical Applications ††

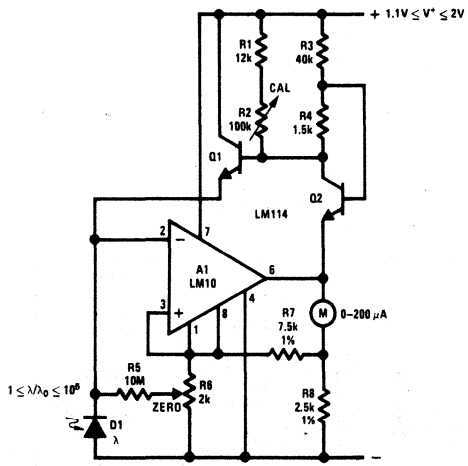
meter amplifier



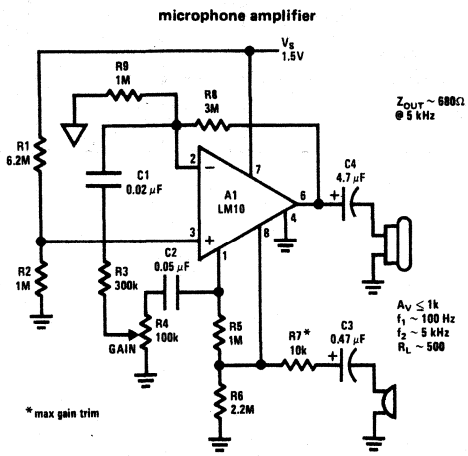
thermometer



light meter



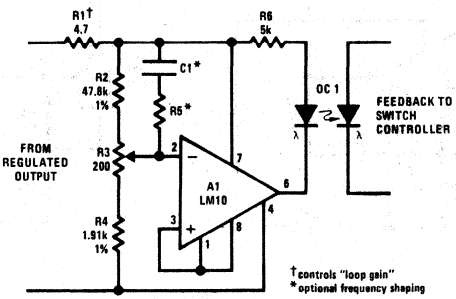
microphone amplifier



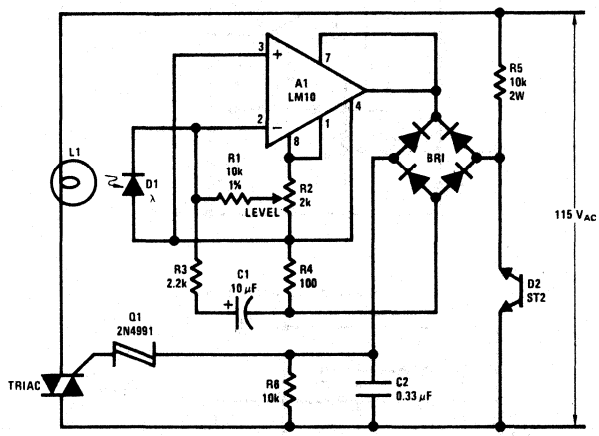
††Circuit descriptions available in application note AN-211.

Typical Applications ††

isolated voltage sensor



light-level controller

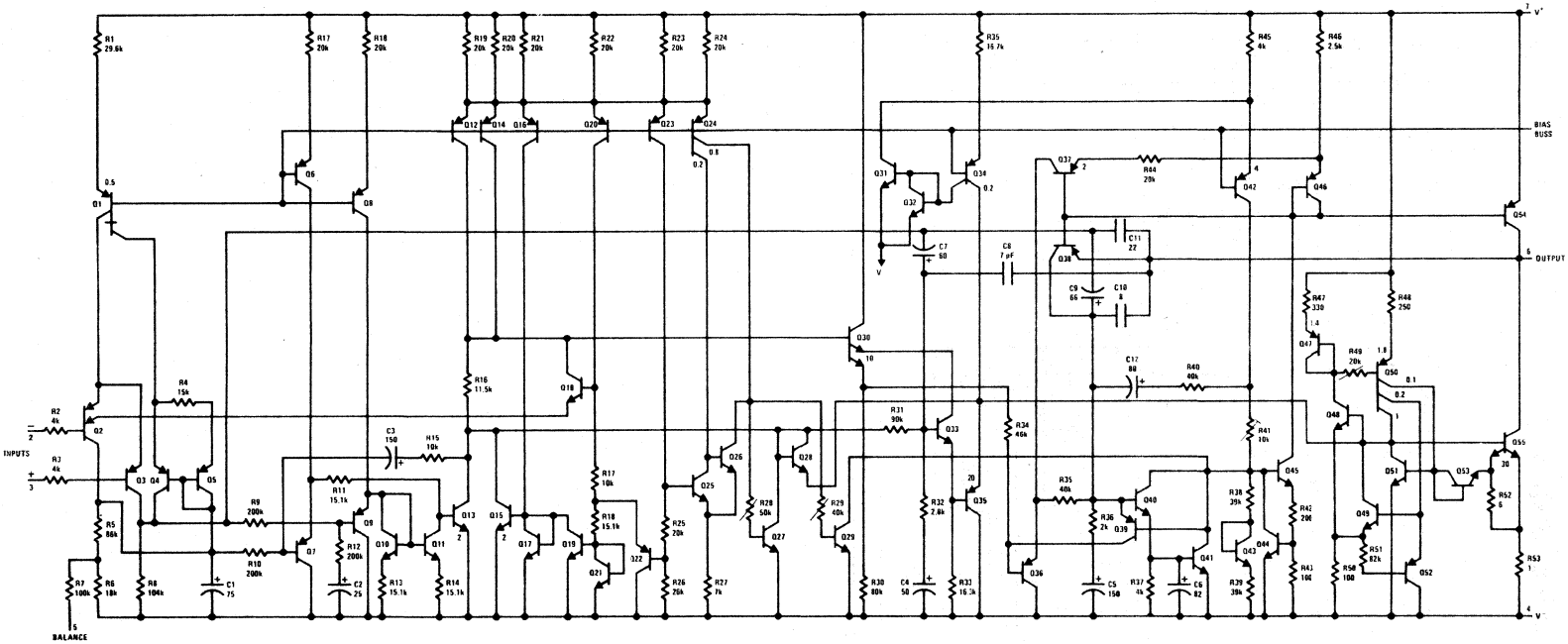


††Circuit descriptions available in application note AN-211.

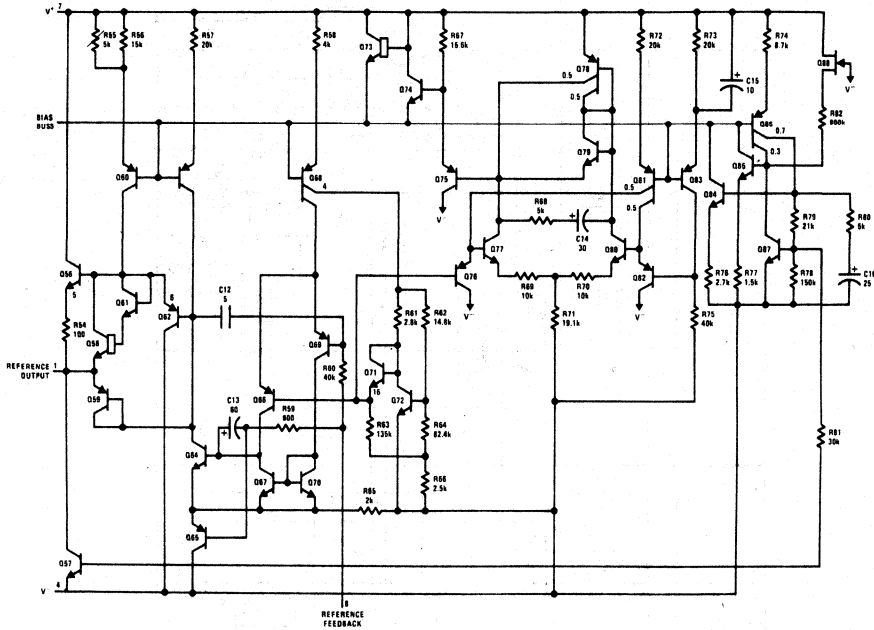
Application Hints

With heavy amplifier loading to V^-, resistance drops in the V^- lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

Operational Amplifier Schematic



Reference and Internal Regulator



Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

National Semiconductor

LM11/LM11C/LM11CL Operational Amplifiers

General Description

The LM11 is a precision dc amplifier combining the best features of existing bipolar and FET op amps. It is similar to the LM108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been improved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and its low drift makes compensation practical. Offset current is almost unmeasureable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm up time in critical applications.

Typical characteristics for 25°C (**−55°C** to **125°C**) are:

- offset voltage: 100 μV (**200 μV**)
- bias current: 25 pA (**65 pA**)
- offset current: 0.5 pA (**3 pA**)
- temperature drift: **1 μV/°C**
- long-term stability: 10 μV/year

The LM11 is internally compensated, but external compensation can be added for improved frequency stability, particularly with capacitive loads. Offset voltage balancing is also provided, with the balance range determined by a low-resistance potentiometer.

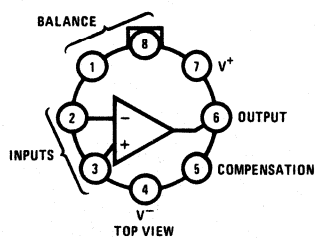
Otherwise, the device is the electrical equivalent of the LM108, except that the negative common-mode limit is 0.6V less, performance is specified down to ± 2.5V and the guaranteed output drive has been increased to ± 2 mA. The input noise is somewhat higher, but amplifier noise is obscured by resistor noise with higher source resistances.

This monolithic IC has obvious applications as electrometer amplifiers, charge integrators, analog memories, low frequency active filters or for frequency shaping in slow servo loops. It can be substituted for existing circuits to provide improved performance or eliminate trimming operations. The greater precision can also be used to extend the dynamic range of logarithmic amplifiers, light meters and solid-state particle detectors.

The LM11 is manufactured with standard bipolar processing using super-gain transistors.

Connection Diagrams

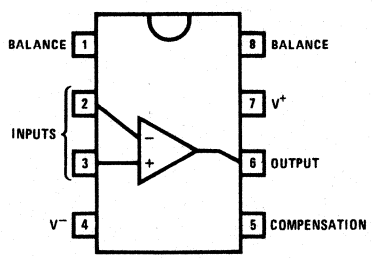
metal can*



TOP VIEW

Order Number LM11H, LM11CH, or LM11CLH
See NS Package H08C

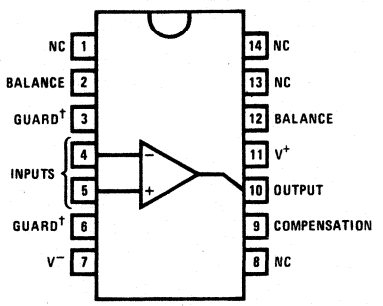
mini-DIP



TOP VIEW

Order Number LM11CN or LM11CLN
See NS Package N08B

dual-in-line package



TOP VIEW

Order Number LM11D, LM11CD, or LM11CLD
See NS Package D14E
Order Number LM11CN-14 or LM11CLN-14
See NS Package N14A

* case connected to V⁻

† guard pins have no internal connection

pin connections shown on schematic diagram and for typical applications are for metal can or mini-DIP.

Absolute Maximum Ratings

total supply voltage	40V
input current (note 1)	± 10 mA
power dissipation (note 2)	500 mW
output short-circuit duration (note 3)	indefinite
storage temperature range	− 65 °C to 150 °C
lead temperature (soldering, 10 seconds)	300 °C

Electrical Characteristics ($T_J = 25\,°C$, $T_{MIN} \leq T_J \leq T_{MAX}$, note 4)

(Boldface type refers to limits over temperature range.)

parameter	conditions	LM11 typ	LM11 lim	LM11C typ	LM11C lim	LM11CL typ	LM11CL lim	units
input offset voltage	note 4	0.1	0.3	0.2	0.6	0.5	5	mV
			0.6		**0.8**		**6**	mV
input offset current	note 4	0.5	10	1	10	4	25	pA
			30		**20**		**50**	pA
input bias current	note 4	25	50	40	100	70	200	pA
			150		**150**		**300**	pA
input resistance	note 4	10^{11}		10^{11}		10^{11}		Ω
offset voltage drift	note 4	1	**3**	2	**5**	3		μV/°C
offset current drift	$T_{MIN} \leq T_J \leq T_{MAX}$	20		10		50		fA/°C
bias current drift	$T_{MIN} \leq T_J \leq T_{MAX}$	0.5	**1.5**	0.8	**3**	1.4		pA/°C
large signal voltage gain	$V_S \pm 15V$, $I_{OUT} = \pm 2$ mA	300	100	300	100	300	25	V/mV
	$V_{OUT} = \pm 12V$ ($\pm 11.5V$)		**50**		**50**		**15**	V/mV
	$V_S = \pm 15V$, $I_{OUT} = \pm 0.5$ mA	1200	250	1200	250	800	50	V/mV
	$V_{OUT} \pm 12V$		**100**		**100**		**30**	V/mV
common-mode rejection	$-13V$ ($-12.5V$) $\leq V_{CM} \leq 14V$	130	110	130	110	110	96	dB
	$V_S = \pm 15V$		**100**		**100**		**90**	dB
supply-voltage rejection	$\pm 2.5V \leq V_S \leq \pm 20V$	118	100	118	100	100	84	dB
			96		**96**		**80**	dB
supply current	note 4	0.3	0.6	0.3	0.8	0.3	0.8	mA
			0.8		**1**		**1**	mA
output short-circuit current	$T_J = 150\,°C$		± 15					mA

note 1: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch up initiated by supply reversals.

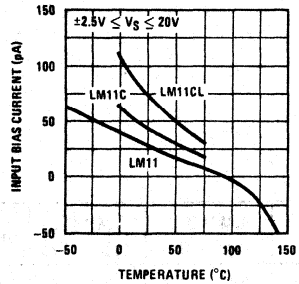
note 2: The maximum operating-junction temperature is 150 °C for the LM11 and 85 °C for the LM11C(L). Devices must be derated based on package thermal resistance (see physical dimensions).

note 3: Current limiting protects the output when it is shorted to ground or any voltage less than the supplies. With continuous overloads, package dissipation must be taken into account and heat sinking provided when necessary.

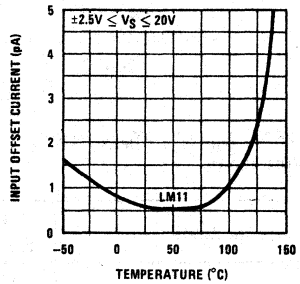
note 4: These specifications apply for $V^- + 2V$ (**2.5V**) $\leq V_{CM} \leq V^+ - 1V$ and $\pm 2.5V \leq V_S \leq \pm 20V$, unless otherwise specified. Normal typeface indicates 25 °C limits. **Boldface type indicates limits for full-temperature range operation.** This is $-55\,°C \leq T_J \leq 125\,°C$ for the LM11 and $0\,°C \leq T_J \leq 70\,°C$ for the LM11C(L).

Typical Characteristics

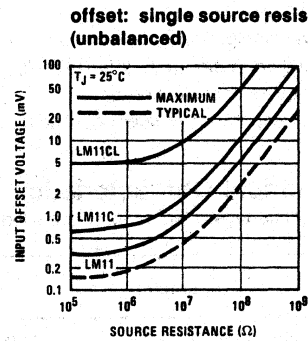
Input bias current



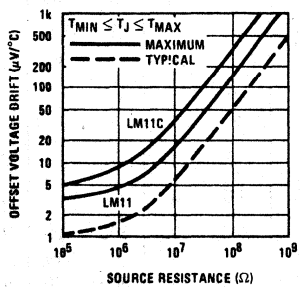
input offset current



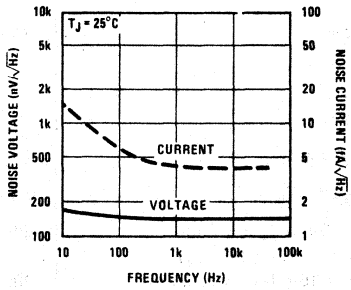
offset: single source resistor (unbalanced)



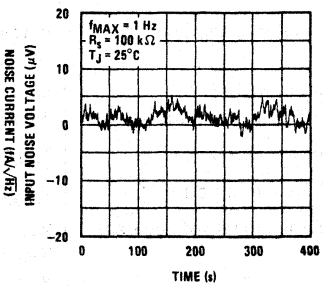
drift: single source resistor (unbalanced)



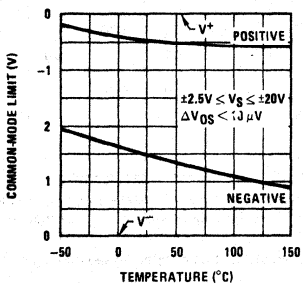
input noise



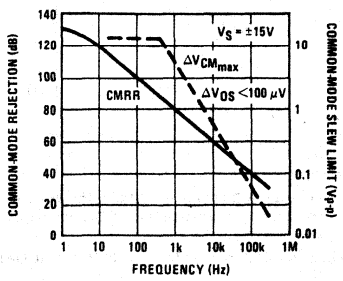
input noise



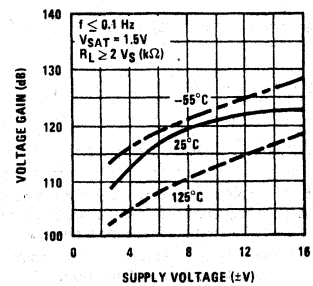
common-mode limits



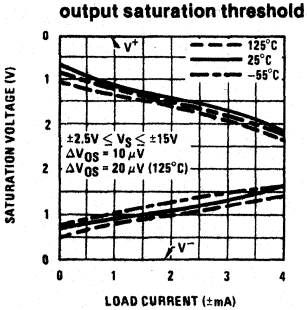
common-mode rejection



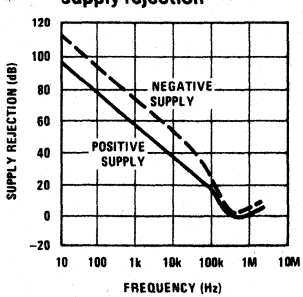
large signal voltage gain



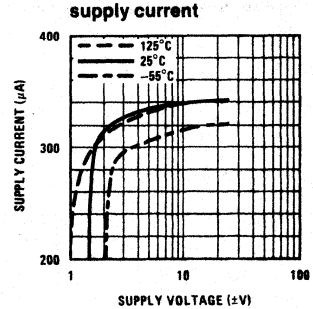
output saturation threshold



supply rejection

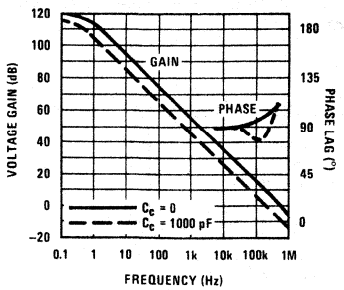


supply current

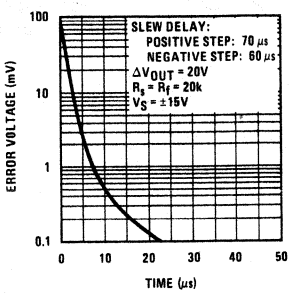


Typical Characteristics (Continued)

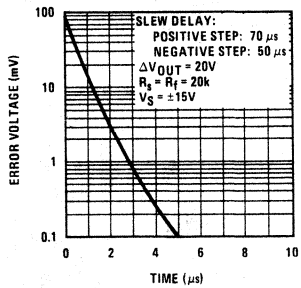
open loop response



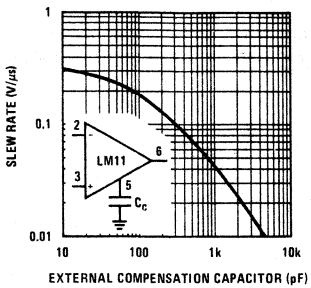
follower final settling time



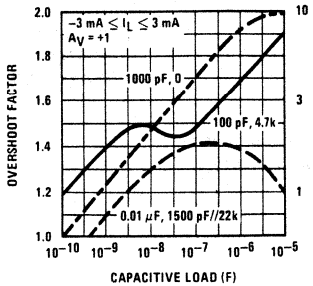
inverter final settling time



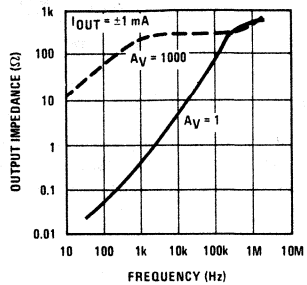
slew rate



stability with over-compensation



closed loop output impedance



Application Hints

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. For critical applications, dual-in-line packages are available that include input guard pins. With the ceramic package, the floating metal lid is best connected to the guard. This might be accomplished with a dab of conductive paint.

Electrostatic shielding of high impedance circuitry is advisable.

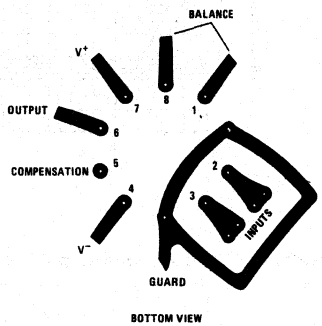
Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients. The most troublesome thermocouples are the junction of the IC package and the printed circuit board (35 µV/°C for copper-kovar) and internal resistor connections. Problems can be avoided by keeping low level circuitry away from heat generating elements. Mounting the IC directly to the PC board while keeping package leads short and the input leads close together can also help.

With the LM11 there is a temptation to remove the bias-current-compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than about 3V. The potential problem involves reversal of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the output current of the second supply is not limited to about 100 mA or if there is much more than 1 µF bypass on the supply buss.

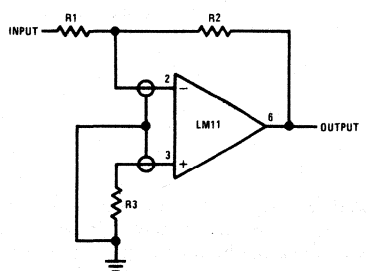
Just disconnecting one supply will generally involve reversal because of loading to the other supply both within the IC and in external circuitry. Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LM11.

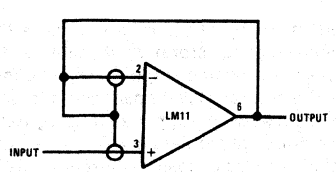
input guarding

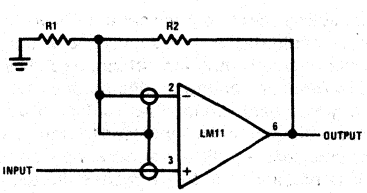
Input guarding can drastically reduce surface leakage. Layout for metal can is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.



Guard ring is connected to low impedance point at same potential as sensitive input leads. Connections for various op amp configurations are shown here.

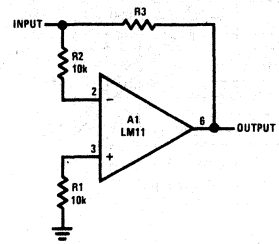




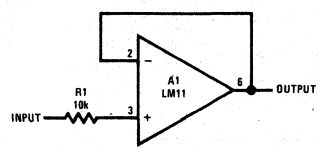


input protection

Current is limited by R2 even when input is connected to voltage source outside common mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.

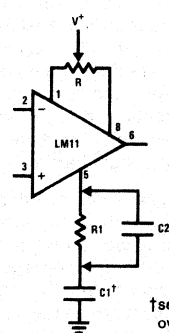


Input resistor controls current when input exceeds supply voltages, when power for op amp is turned off or when output is shorted.



balancing and over-compensation

Over-compensation will improve stability with capacitive loading (see curves). Offset voltage adjustment range is determined by balance potentiometer resistance as indicated in the table.

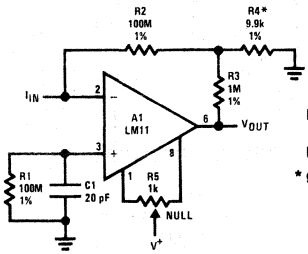


†see stability with over-compensation curve

min. adj range	R
±5 mV	100 kΩ
±2	10k
±1	3k
±0.8	3k
±0.4	1k

resistance multiplication

Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.

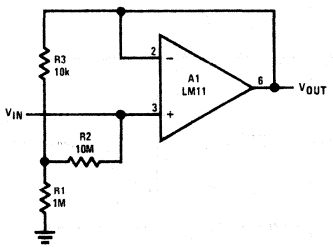


$$R_f = R2\left(1 + \frac{R3}{R4}\right)$$

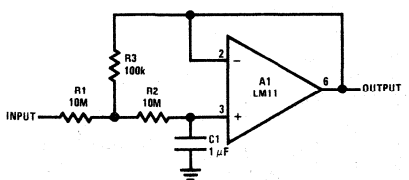
R2>> R3 // R4

* gain trim

Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not great because the op amp offset is low.



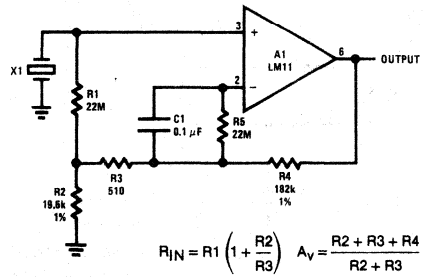
This circuit multiplies RC time constant to 1000 seconds and provides low output impedance.



$$\tau = \frac{R1\,C}{R3}(R2 + R3)$$

$$\Delta V_{OUT} = \frac{R1 + R3}{R3}(I_B R2 + V_{OS})$$

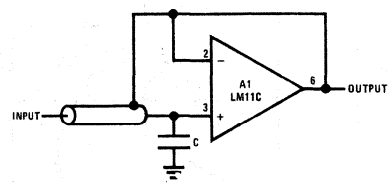
A high-input-impedance ac amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.



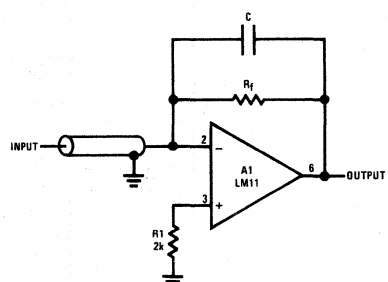
$$R_{IN} = R1\left(1 + \frac{R2}{R3}\right) \quad A_V = \frac{R2 + R3 + R4}{R2 + R3}$$

cable bootstrapping

Bootstrapping input shield for a follower reduces cable capacitance, leakage and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.

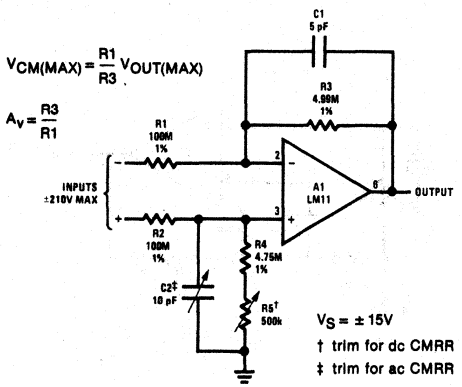


With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

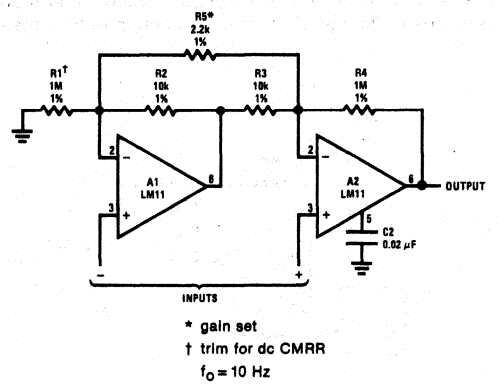


differential amplifiers

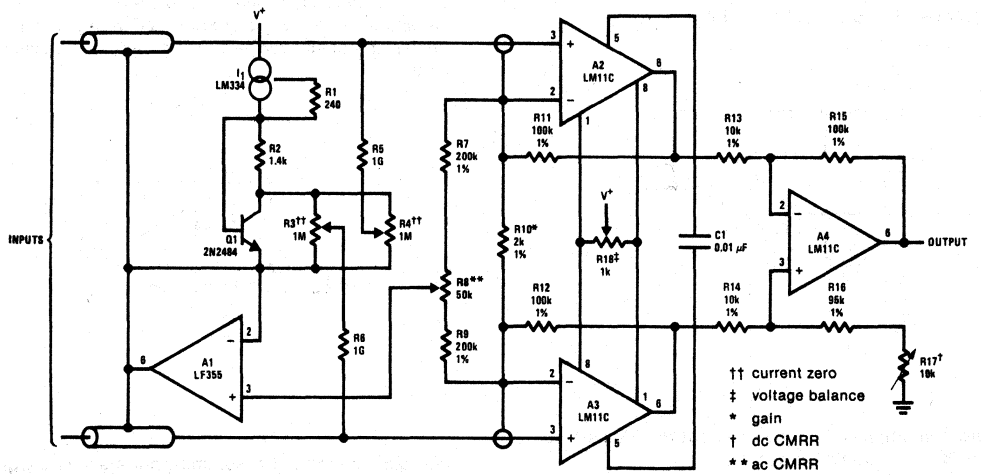
This differential amplifier handles high input voltages. Resistor mismatches and stray capacitors should be balanced out for best common-mode rejection.



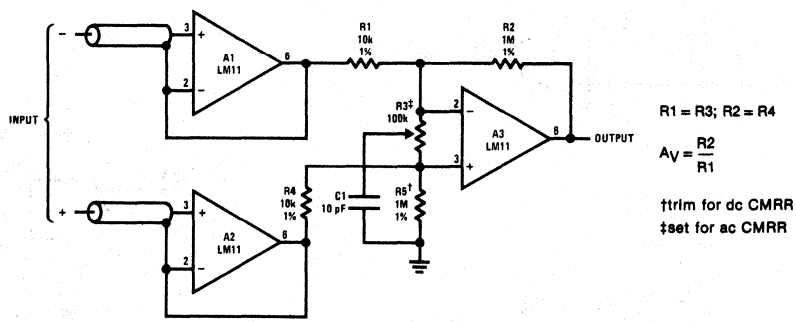
Two op-amp instrumentation amplifier has poor ac common mode rejection. This can be improved at the expense of differential bandwidth with C2.



High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.

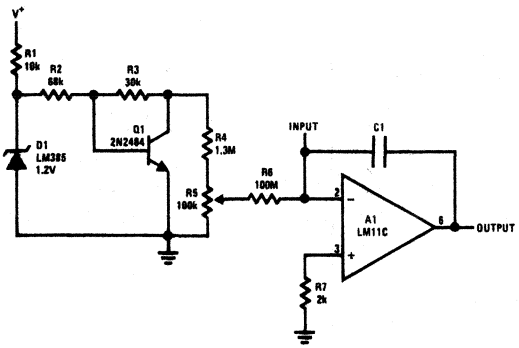


For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A3 must also have low drift.

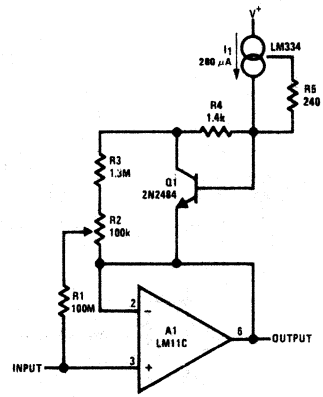


bias current compensation

Precise bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.

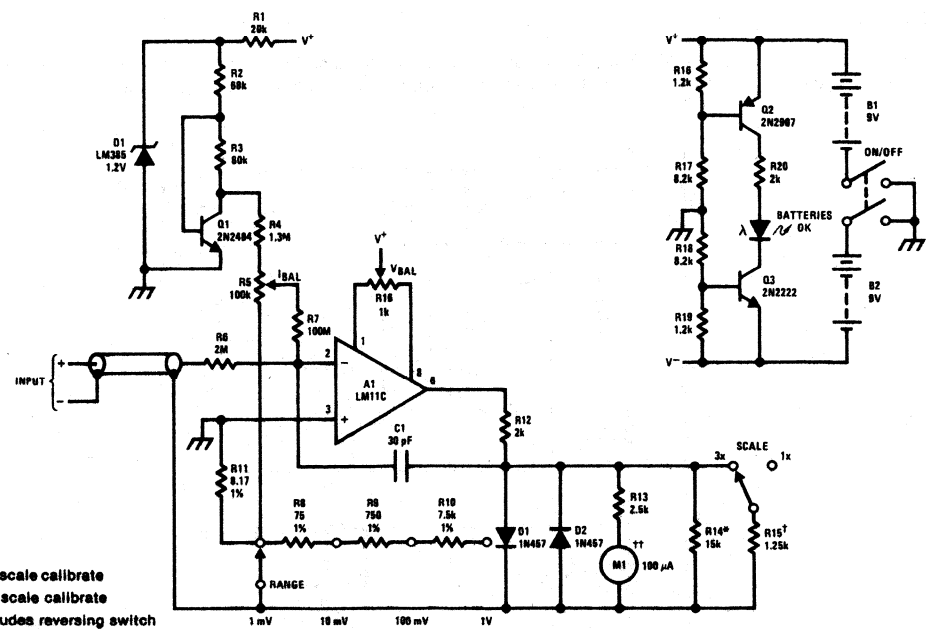


This circuit shows how bias current compensation can be used on a voltage follower.



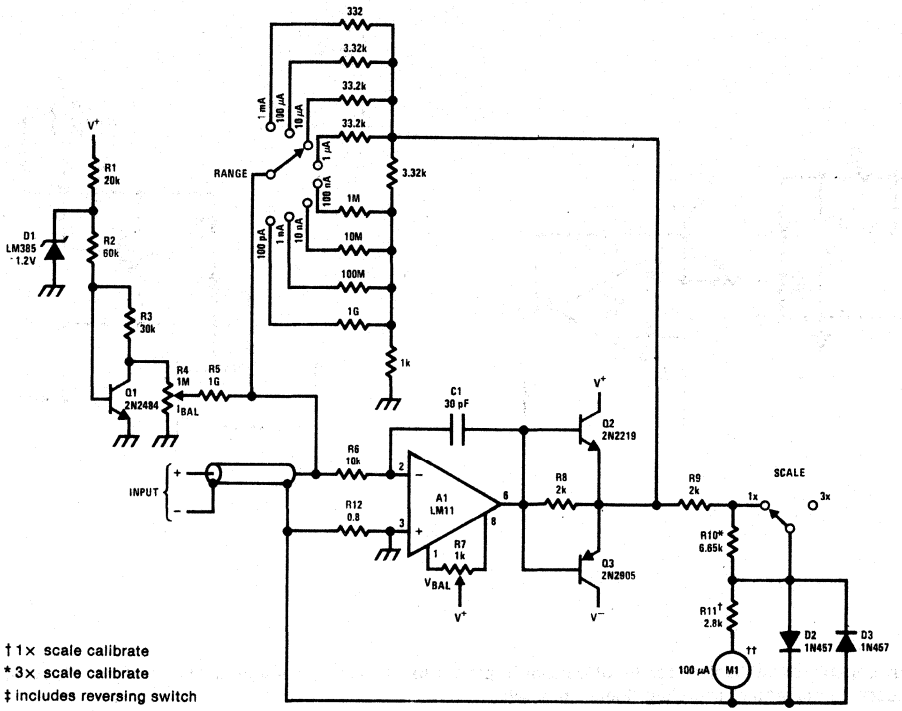
voltmeter

High input impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full scale. Reference could be used to make direct reading linear ohmmeter.



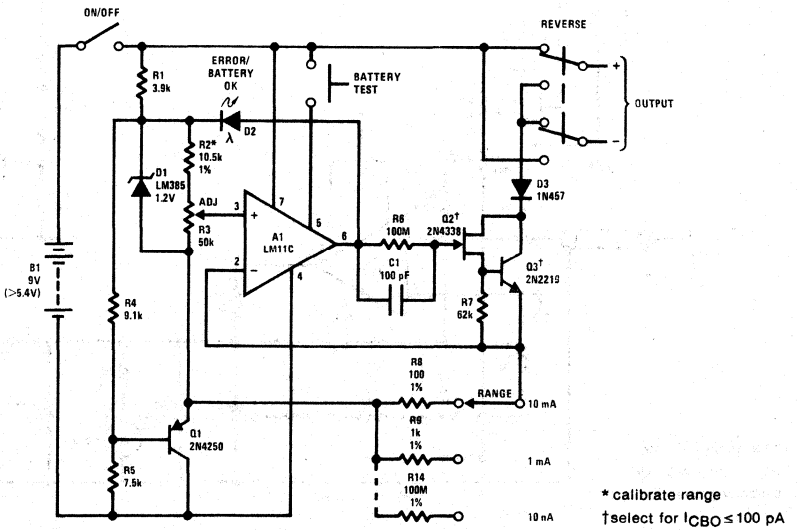
ammeter

Current meter ranges from 100 pA to 3 mA full scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.



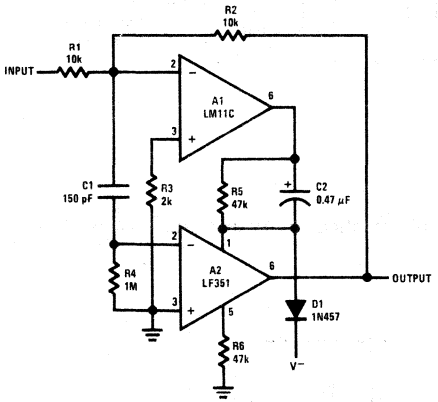
current source

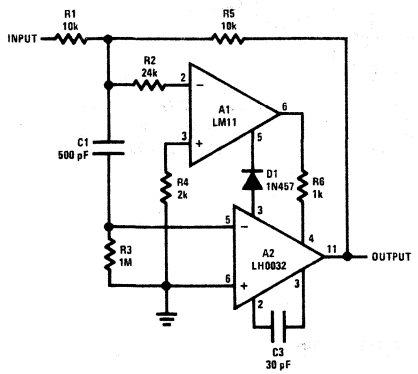
Precision current source has 10 μA to 10 mA ranges with output compliance of 30V to −5V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates saturation.



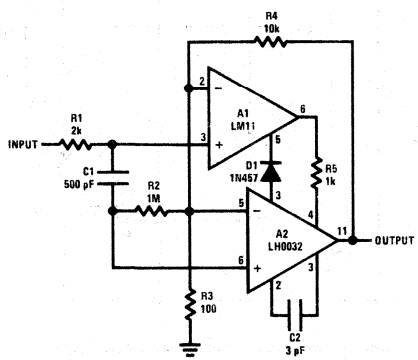
fast amplifiers

These inverters have bias current and offset voltage of LM11 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 μs. Overload-recovery delay can be eliminated by direct coupling the FET amplifier to summing node.

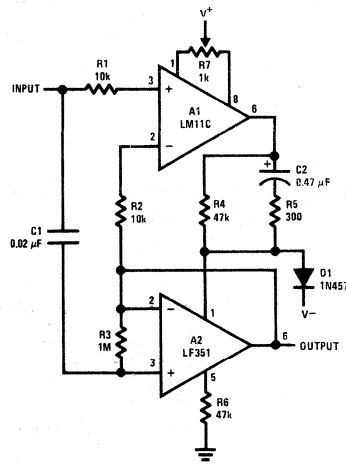




This 100× amplifier has small and large signal bandwidth of 1 MHz. The LM11 greatly reduces offset voltage, bias current and gain error. Eliminating long recovery delay for greater than 100% overload requires direct coupling of A2 to input.

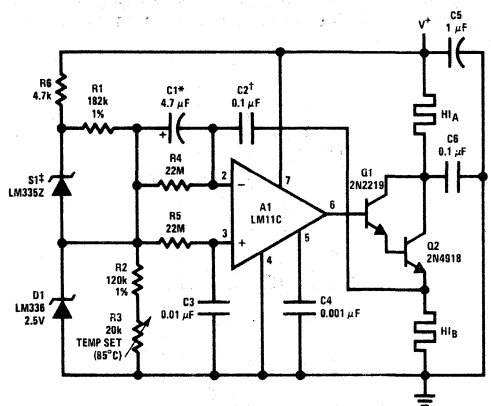


Follower has 10 μs setting to 1 mV, but signal repetition frequency should not exceed 10 kHz if the FET amplifier is ac coupled to input. The circuit does not behave well if common-mode range is exceeded.



heater control

Proportional control crystal oven heater uses lead/lag compensation for fast settling. Time constant is changed with R4 and compensating resistor R5. If Q2 is inside oven, a regulated supply is recommended for 0.1°C control.



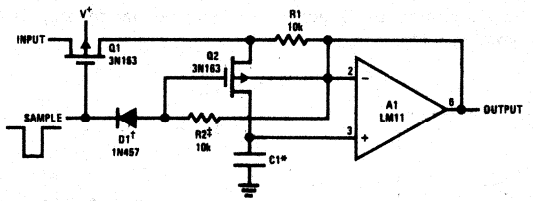
* solid tantalum

† mylar

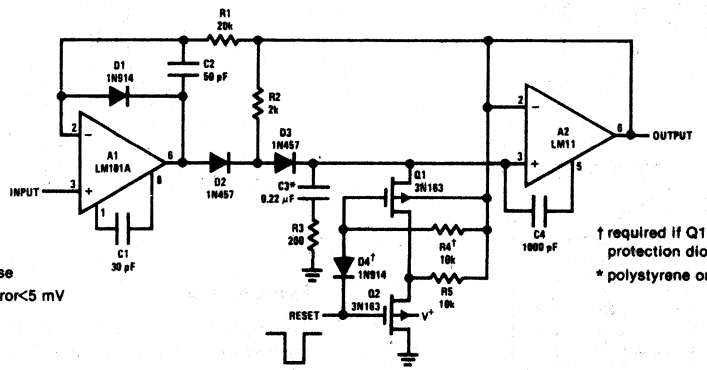
‡ close thermal coupling between sensor and oven shell is recommended.

leakage isolation

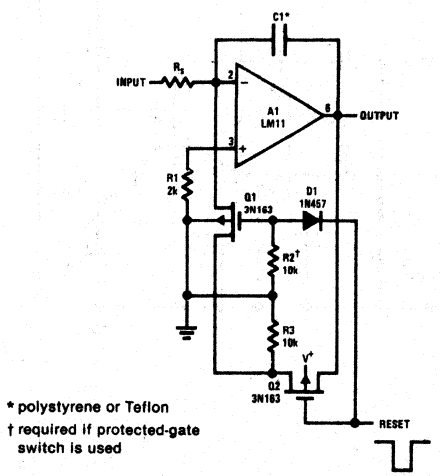
Switch leakage in this sample and hold does not reach storage capacitor.



A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.

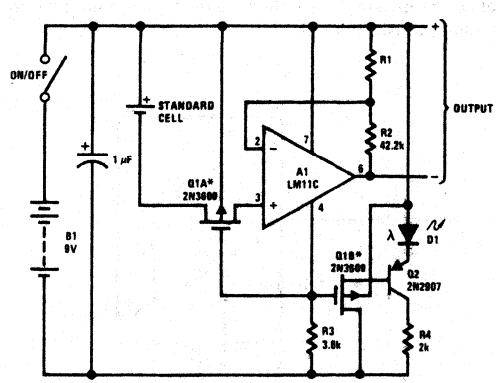


Reset is provided for this integrater and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.



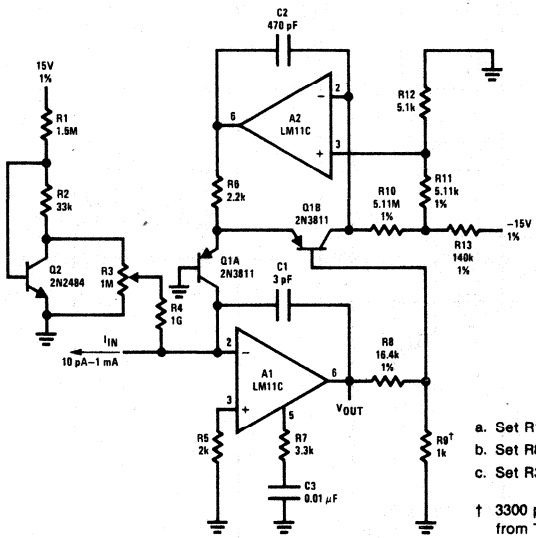
standard-cell buffer

Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.



logarithmic amplifiers

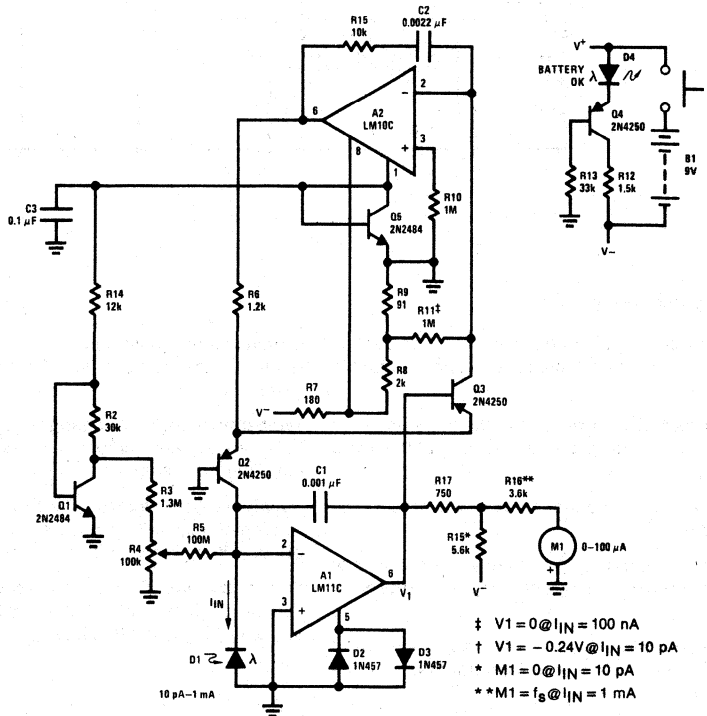
Unusual frequency compensation gives this logarithmic converter a 100 μs time constant from 1 mA down to 100 μA, increasing from 200 μs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to 100°C. Scale factor is 1V/decade and temperature compensated.



a. Set R11 for $V_{OUT} = 0$ at $I_{IN} = 100\ \mu A$
b. Set R8 for $V_{OUT} = 3V$ at $I_{IN} = 100\ \mu A$
c. Set R3 for $V_{OUT} = -4V$ at $I_{IN} = 10$ pA

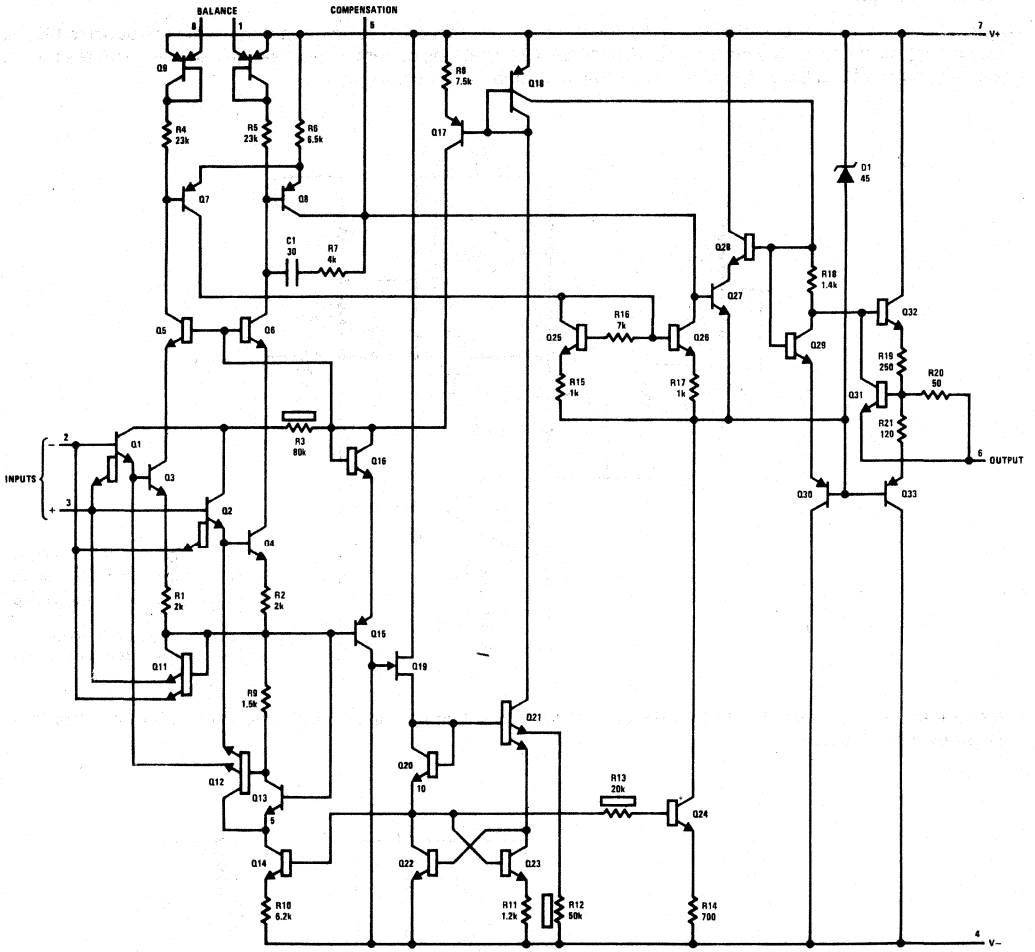
† 3300 ppM/°C. Type Q209 available from Tel Labs, Inc., Manchester, N.H.

Light meter has eight-decade range. Bias current compensation can give input current resolution of better than ±2 pA over 15°C to 55°C.



‡ $V1 = 0 @ I_{IN} = 100$ nA
† $V1 = -0.24V @ I_{IN} = 10$ pA
* $M1 = 0 @ I_{IN} = 10$ pA
** $M1 = f_S @ I_{IN} = 1$ mA

Schematic Diagram



Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Temperature drift: The change of a parameter measured at 25 °C and either temperature extreme divided by the temperature change.

Supply-voltage rejection: The ratio of the specified supply-voltage change (either or both supplies) to the change in offset voltage between the extremes.

Supply current: The current required from the power source to operate the amplifier with the output unloaded and operating in the linear range.

National Semiconductor

LM146/LM246/LM346 Programmable Quad Operational Amplifiers

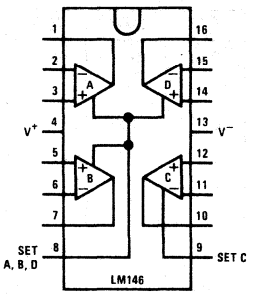
General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features (I_{SET} = 10 μA)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current — 350 μA amplifier
- Guaranteed gain bandwidth product — 0.8 MHz min
- Large DC voltage gain — 120 dB
- Low noise voltage — 28 nV/√Hz
- Wide power supply range — ±1.5V to ±22V
- Class AB output stage—no crossover distortion
- Ideal pin out for Biquad active filters
- Input bias currents are temperature compensated

Connection Diagrams (Dual-In-Line Packages, Top Views)



Order Number LM146J, LM246J or LM346J
See NS Package J16A

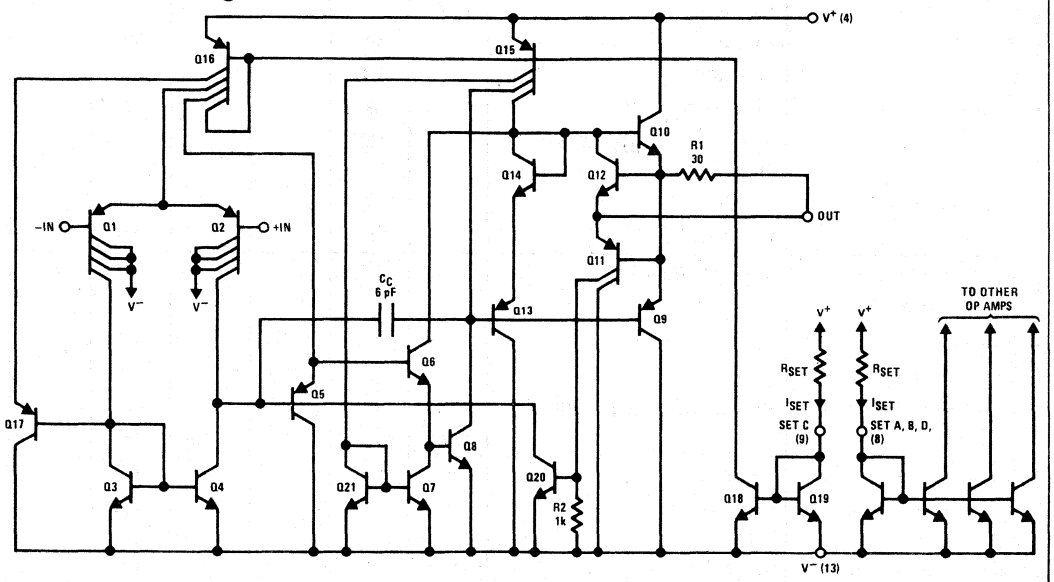
Order Number LM246N or LM346N
See NS Package N16A

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current ≃ 50 nA (I_{SET}/10 μA)
I_{SET} = Current into pin 8, pin 9 (see schematic-diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Schematic Diagram



Absolute Maximum Ratings (Note 1)

	LM146	LM246	LM346
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage (Note 1)	±30V	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW	500 mW
Output Short-Circuit Duration (Note 3)	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Maximum Junction Temperature	150°C	110°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C
Thermal Resistance (θ_{jA}), (Note 2)			
Cavity DIP (D) (J) P_d	900 mW	900 mW	900 mW
θ_{jA}	90°C/W	90°C/W	90°C/W
Molded DIP (N) P_d			500 mW
θ_{jA}			140°C/W

DC Electrical Characteristics (V_S = ±15V, I_{SET} = 10 μA, Note 4)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{CM} = 0V, $R_S \leq$ 50 Ω, T_A = 25°C		0.5	5		0.5	6	mV
Input Offset Current	V_{CM} = 0V, T_A = 25°C		2	20		2	100	nA
Input Bias Current	V_{CM} = 0V, T_A = 25°C		50	100		50	250	nA
Supply Current (4 Op Amps)	T_A = 25°C		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V, T_A = 25°C	100	1000		50	1000		V/mV
Input CM Range	T_A = 25°C	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq$ 10 kΩ, T_A = 25°C	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq$ 10 kΩ, T_A = 25°C	80	100		74	100		dB
Output Voltage Swing	$R_L \geq$ 10 kΩ, T_A = 25°C	±12	±14		±12	±14		V
Short-Circuit Current	T_A = 25°C	5	20	30	5	20	30	mA
Gain Bandwidth Product	T_A = 25°C	0.8	1.2		0.5	1.2		MHz
Phase Margin	T_A = 25°C		60			60		Deg
Slew Rate	T_A = 25°C		0.4			0.4		V/μs
Input Noise Voltage	f = 1 kHz, T_A = 25°C		28			28		$nV/\sqrt{Hz}$
Channel Separation	R_L = 10 kΩ, ΔV_{OUT} = 0V to ±12V, T_A = 25°C		120			120		dB
Input Resistance	T_A = 25°C		1.0			1.0		MΩ
Input Capacitance	T_A = 25°C		2.0			2.0		pF
Input Offset Voltage	V_{CM} = 0V, $R_S \leq$ 50 Ω		0.5	6		0.5	7.5	mV
Input Offset Current	V_{CM} = 0V		2	25		2	100	nA
Input Bias Current	V_{CM} = 0V		50	100		50	250	nA
Supply Current (4 Op Amps)			1.5	2.0		1.5	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V	50	1000		25	1000		V/mV
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq$ 50 Ω	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq$ 50 Ω	76	100		74	100		dB
Output Voltage Swing	$R_L \geq$ 10 kΩ	±12	±14		±12	±14		V

DC Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 1\ \mu A$)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input Bias Current	$V_{CM} = 0V$, $T_A = 25°C$		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	$T_A = 25°C$		140	250		140	300	μA
Gain Bandwidth Product	$T_A = 25°C$	80	100		50	100		kHz

DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10\ \mu A$)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input CM Range	$T_A = 25°C$	±0.7			±0.7			V
CM Rejection Ratio	$R_S \leq 50\ \Omega$, $T_A = 25°C$		80			80		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	±0.6			±0.6			V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

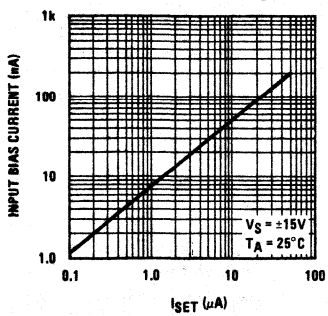
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

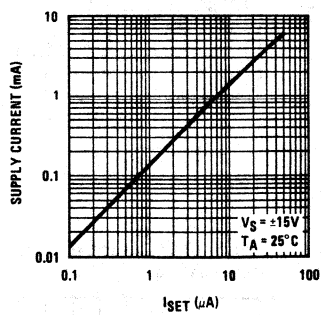
Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

Typical Performance Characteristics

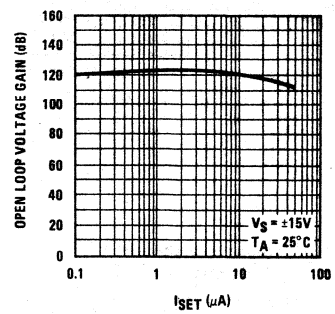
Input Bias Current vs I_{SET}



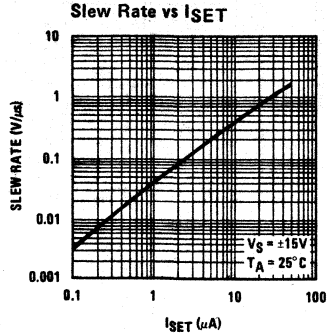
Supply Current vs I_{SET}



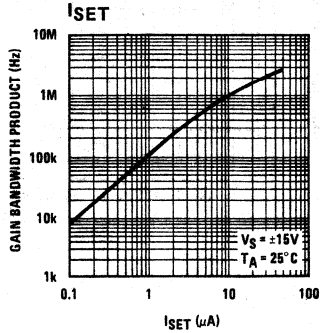
Open Loop Voltage Gain vs I_{SET}



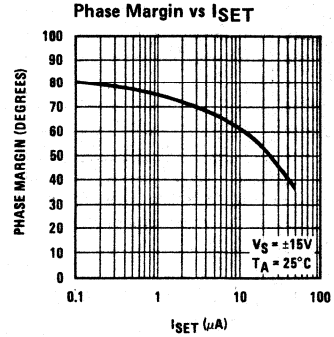
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}

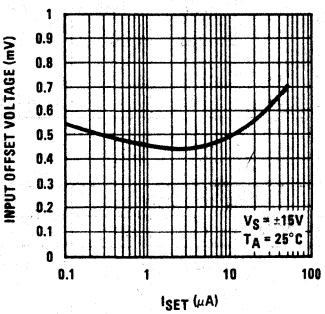


Phase Margin vs I_{SET}

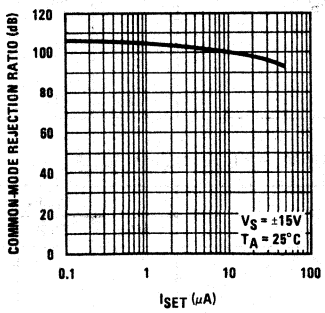


Typical Performance Characteristics (Continued)

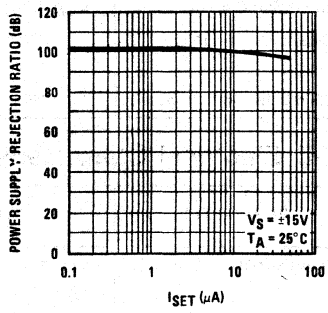
Input Offset Voltage vs I_{SET}



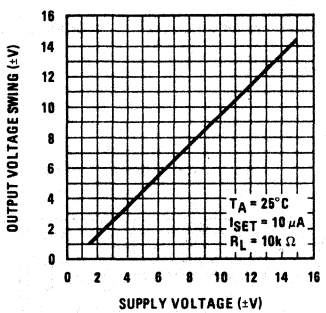
Common-Mode Rejection Ratio vs I_{SET}



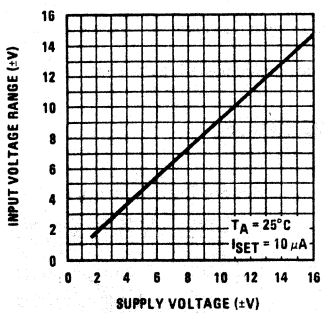
Power Supply Rejection Ratio vs I_{SET}



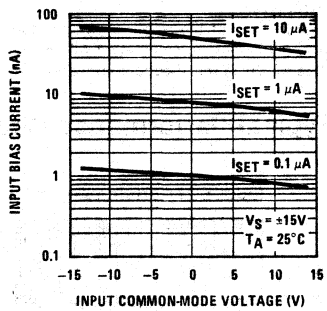
Output Voltage Swing vs Supply Voltage



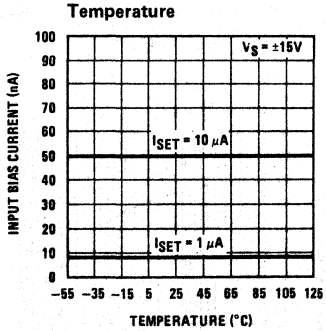
Input Voltage Range vs Supply Voltage



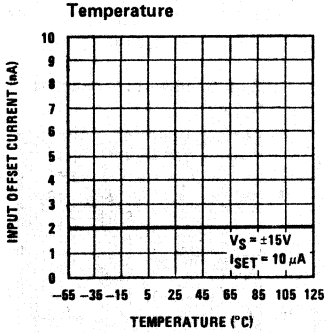
Input Bias Current vs Input Common-Mode Voltage



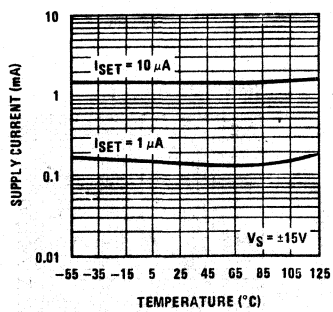
Input Bias Current vs Temperature



Input Offset Current vs Temperature

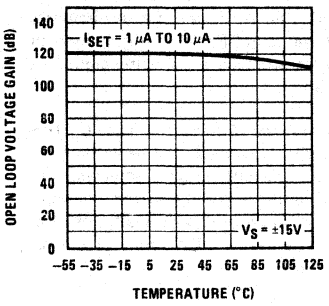


Supply Current vs Temperature

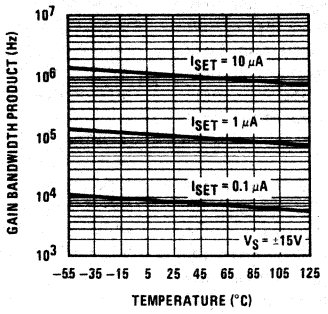


Typical Performance Characteristics (Continued)

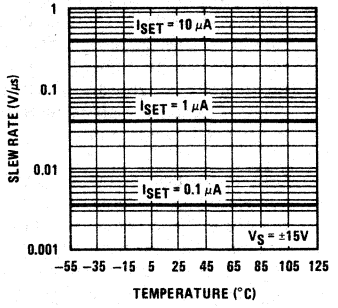
Open Loop Voltage Gain vs Temperature



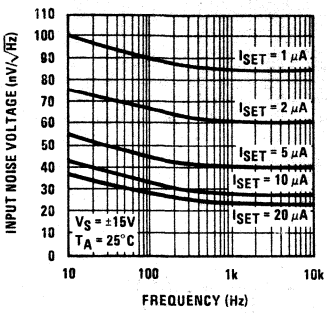
Gain Bandwidth Product vs Temperature



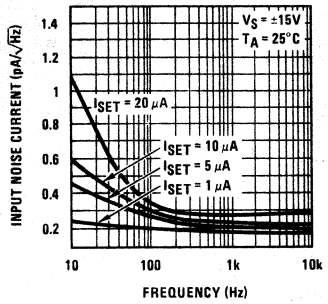
Slew Rate vs Temperature



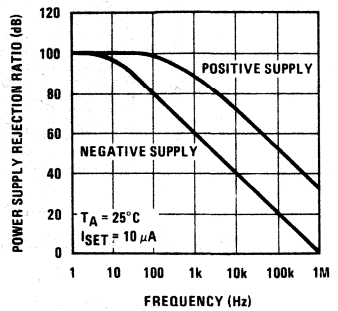
Input Noise Voltage vs Frequency



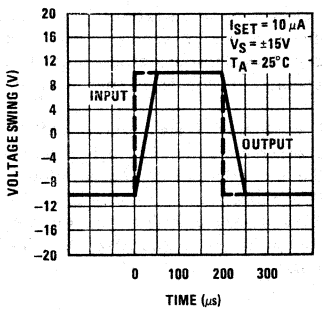
Input Noise Current vs Frequency



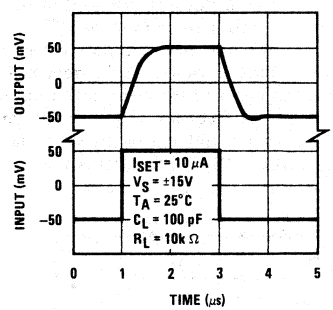
Power Supply Rejection Ratio vs Frequency



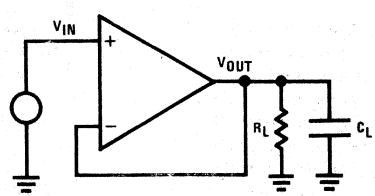
Voltage Follower Pulse Response



Voltage Follower Transient Response



Transient Response Test Circuit



Application Hints

Avoid reversing the power supply polarity, the device will fail.

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

Output Voltage Swing vs I_{SET}: For a desired output voltage swing the value of the minimum load depends on the positive and negative output curent capability of the op amp. The maximum available positive output current, (I_{CL+}), of the device increases with I_{SET} whereas the negative output current (I_{CL-}) is independent of I_{SET}. *Figure 1* illustrates the above.

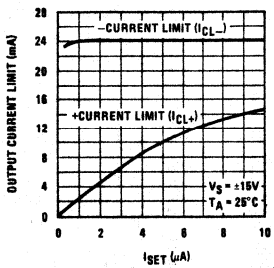


FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN}, of the LM146 is approximately 2 pF; any stray capacitance, C_S, (due to external circuit circuit layout) will add to C_{IN}. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback *(Figure 2)*, this pole occurs at $1/2\pi$ (R1||R2) (C_{IN} + C_S). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_I(C_S + C_{IN})$, where R_I is the input resistance of the circuit.

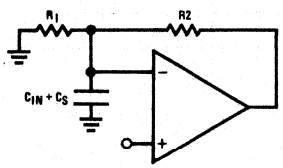


FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product), of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current, I_{SET}, of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an I_{SET} current directly proportional to temperature (see typical applications).

Isolation Between Amplifiers: The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behavior is shown in *Figure 3*. The device is fully predictable. As the set current, I_{SET}, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5–4 MHz.

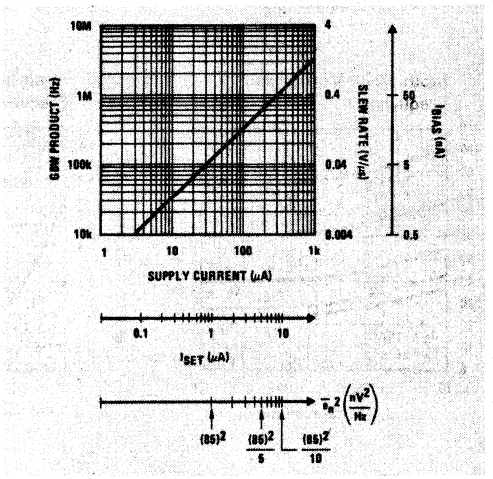


FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz, for GBW products below 200 kHz, the LM4250 will consume less.

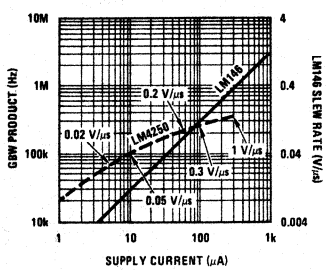
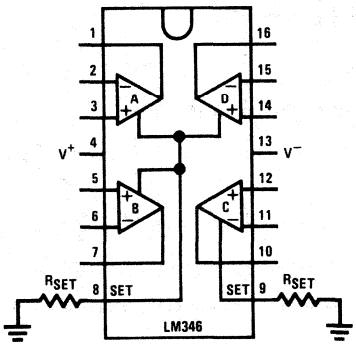


FIGURE 4. LM146 vs LM4250

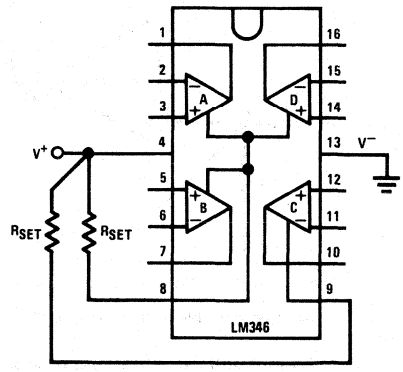
Typical Applications

Dual Supply or Negative Supply Biasing



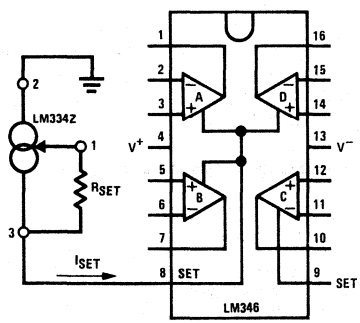
$$I_{SET} \simeq \frac{|V^-| - 0.6V}{R_{SET}}$$

Single (Positive) Supply Biasing



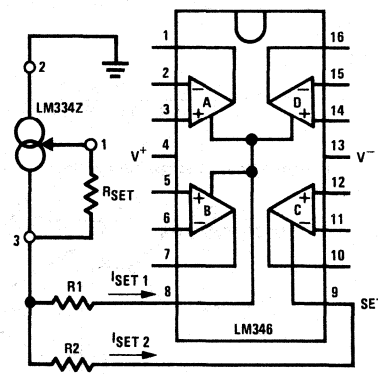
$$I_{SET} \simeq \frac{V^+ - 0.6V}{R_{SET}}$$

Current Source Biasing with Temperature Compensation



$$I_{SET} = \frac{67.7\ mV}{R_{SET}}$$

Biasing all 4 Amplifiers with Single Current Source

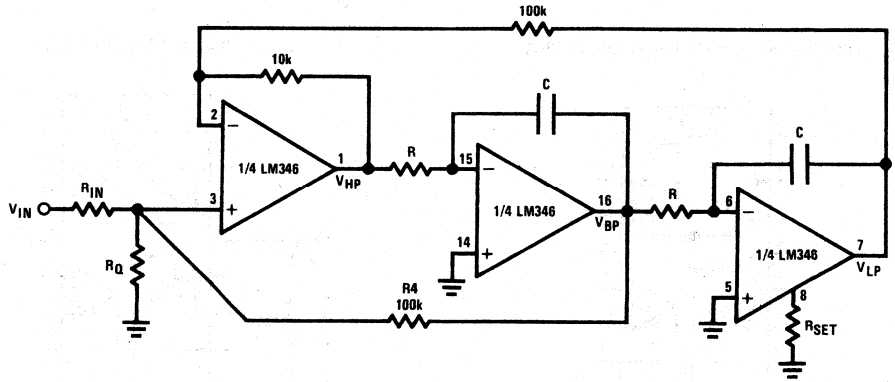


$$\frac{I_{SET1}}{I_{SET2}} = \frac{R2}{R1},\ I_{SET1} + I_{SET2} = \frac{67.7\ mV}{R_{SET}}$$

- The LM334 provides an I_{SET} directly proportional to absolute temperature. This cancels the slight GBW product temperature coefficient of the LM346.
- For $I_{SET1} \simeq I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use R1 = R2 to create a 100 mV drop across these resistors.

Active Filters Applications

Basic (Non-Inverting "State Variable") Active Filter Building Block



- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

  Circuit synthesis equations (for circuit analysis equations, consult with the AF100 and LM148 data sheet).

  Need to know desired: f_o = center frequency measured at the BP output
  Q_o = quality factor measured at the BP output
  H_o = gain at the output of interest (BP or HP or LP or all of them)

  ▲ Relation between different gains: $H_{o(BP)} = 0.316 \times Q_o \times H_{o(LP)}$; $H_{o(LP)} = 10 \times H_{o(HP)}$

  ▲ $R \times C = \dfrac{5.033 \times 10^{-2}}{f_o}$ (sec)

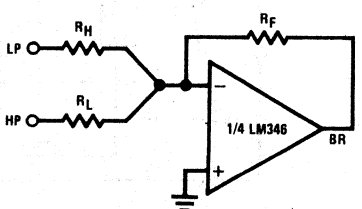
  ▲ For BP output: $R_Q = \left(\dfrac{3.478\ Q_o - H_{o(BP)}}{10^5} - \dfrac{H_{o(BP)}}{10^5 \times 3.478 \times Q_o} \right)^{-1}$; $R_{IN} = \dfrac{\left(\dfrac{3.478\ Q_o}{H_{o(BP)}} - 1 \right)}{\dfrac{1}{R_Q} + 10^{-5}}$

  ▲ For HP output: $R_Q = \dfrac{1.1 \times 10^5}{3.478\ Q_o\ (1.1 - H_{o(HP)}) - H_{o(HP)}}$; $R_{IN} = \dfrac{\dfrac{1.1}{H_{o(HP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

  Note. All resistor values are given in ohms.

  ▲ For LP output: $R_Q = \dfrac{11 \times 10^5}{3.478\ Q_o\ (11 - H_{o(LP)}) - H_{o(LP)}}$; $R_{IN} = \dfrac{\dfrac{11}{H_{o(LP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

  ▲ For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.



$$\sqrt{\frac{R_H}{R_L}} = 0.316\ \frac{f_{notch}}{f_o}$$

Determine R_F according to the desired gains: $H_{o(BR)}\big|_{f << f_{notch}} = \dfrac{R_F}{R_L} H_{o(LP)}$, $H_{o(BR)}\big|_{f >> f_{notch}} = \dfrac{R_F}{R_H} H_{o(HP)}$

- **Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (V_{HP}, V_{BP}, V_{LP}), that is:

$$V_{IN(peak)} < 63.66 \times 10^3 \times \frac{I_{SET}}{10\ \mu A} \times \frac{1}{f_o \times H_o}\ \text{(Volts)}$$

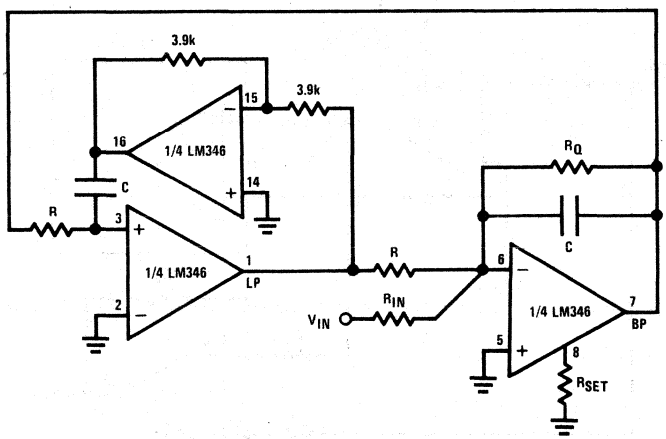
If necessary, use amplifier C, biased at higher I_{SET}, where you get the largest output swing.

Deviation from Theoretical Predictions: Due to the finite GBW products of the op amps the f_o, Q_o will be slightly different from the theoretical predictions.

$$f_{real} \simeq \frac{f_o}{1 + \dfrac{2\ f_o}{GBW}}\ ,\quad Q_{real} \simeq \frac{Q_o}{1 - \dfrac{3.2\ f_o \times Q_o}{GBW}}$$

Active Filters Applications (Continued)

A Simple-to-Design BP, LP Filter Building Block



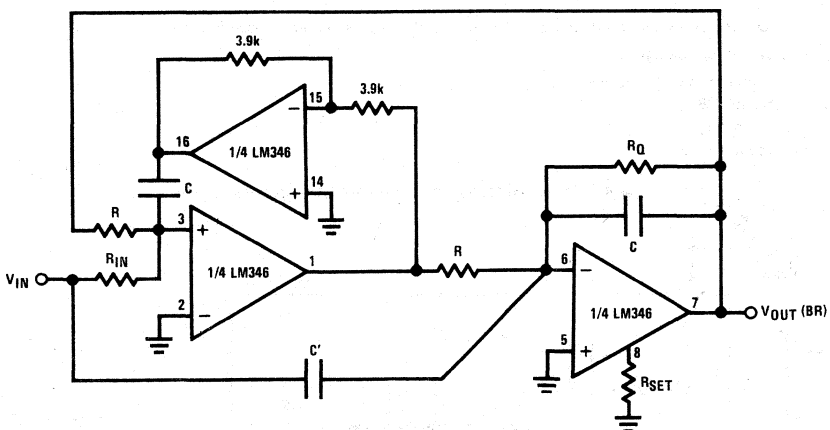
- If resistive biasing is used to set the LM346 performance, the Q_o of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

Circuit Synthesis Equations

$$H_{o(BP)} = Q_o H_{o(LP)};\ R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{R_Q}{H_{o(BP)}} = \frac{R}{H_{o(LP)}}$$

- For the eventual use of amplifier C, see comments on the previous page.

A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)



Circuit Synthesis Equations

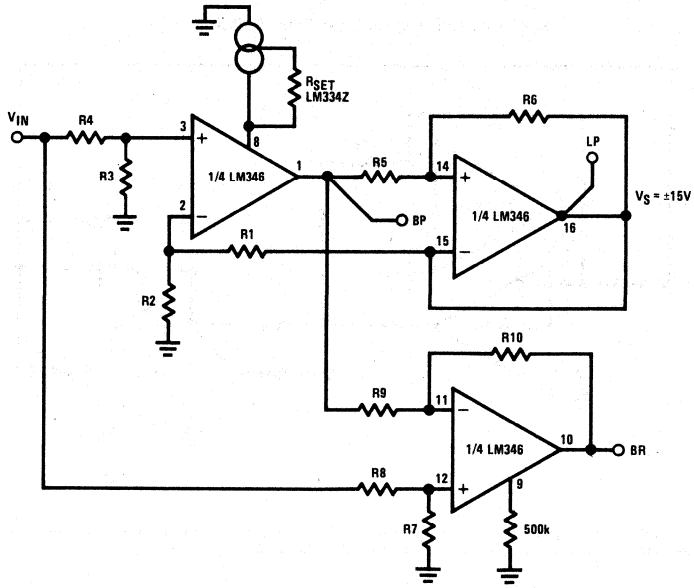
$$R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{0.159 \times f_o}{C' \times f^2_{notch}}$$

$$H_{o(BR)}\Big|_{f << f_{notch}} = \frac{R}{R_{IN}}\ H_{o(BR)}\Big|_{f >> f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R$, $C' = C$.

Active Filters Applications (Continued)

Capacitorless Active Filters (Basic Circuit)

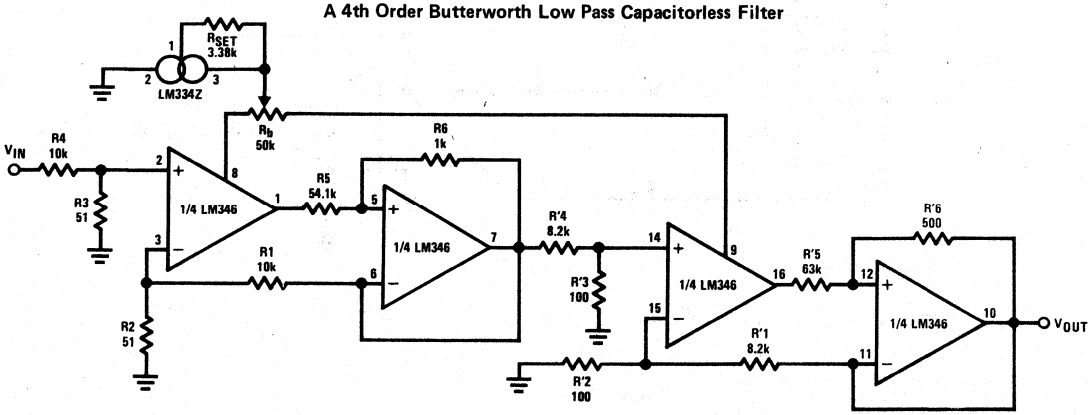


- This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.
- **Limitations:** $Q_o < 10$, $f_o \times Q_o < 1.5$ MHz, output voltage should not exceed $V_{peak(out)} \leq \frac{63.66 \times 10^3}{f_o} \times \frac{I_{SET}\ (\mu A)}{10\ \mu A}$ (V)
- Design equations: $a = \frac{R6 + R5}{R6}$, $b = \frac{R2}{R1 + R2}$, $c = \frac{R3}{R3 + R4}$, $d = \frac{R7}{R8 + R7}$, $e = \frac{R10}{R9 + R10}$, $f_{o(BP)} = f_u \sqrt{\frac{b}{a}}$, $H_{o(BP)} = a \times c$,

  $H_{o(LP)} = \frac{c}{b}$, $Q_o = \sqrt{a \times b}$

  $f_{o(BR)} = f_{o(BP)} \left(1 - \frac{c}{b}\right) \simeq f_{o(BP)}$ $(C << 1)$ provided that $d = H_{o(BP)} \times e$, $H_{o(BR)} = \frac{R10}{R9}$.
- Advantage: f_o, Q_o, H_o can be independently adjusted; that is, the filter is extremely easy to tune.
- Tuning procedure (ex. BP tuning)
  1. Pick up a convenient value for b; $(b < 1)$
  2. Adjust Q_o through R5
  3. Adjust $H_{o(BP)}$ through R4
  4. Adjust f_o through R_{SET}

A 4th Order Butterworth Low Pass Capacitorless Filter

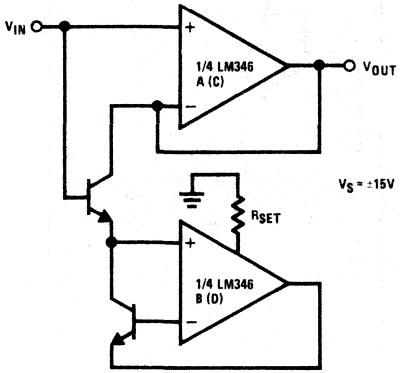


Ex: f_c = 20 kHz, H_o (gain of the filter) = 1, Q_{o1} = 0.541, Q_{o2} = 1.306.

- Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through R_b.

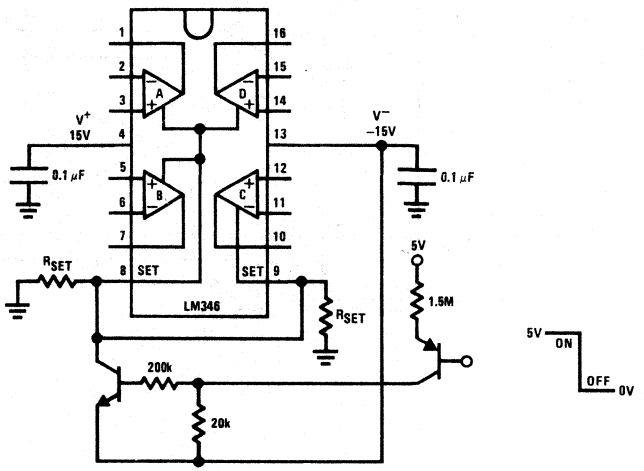
Miscellaneous Applications

A Unity Gain Follower with Bias Current Reduction



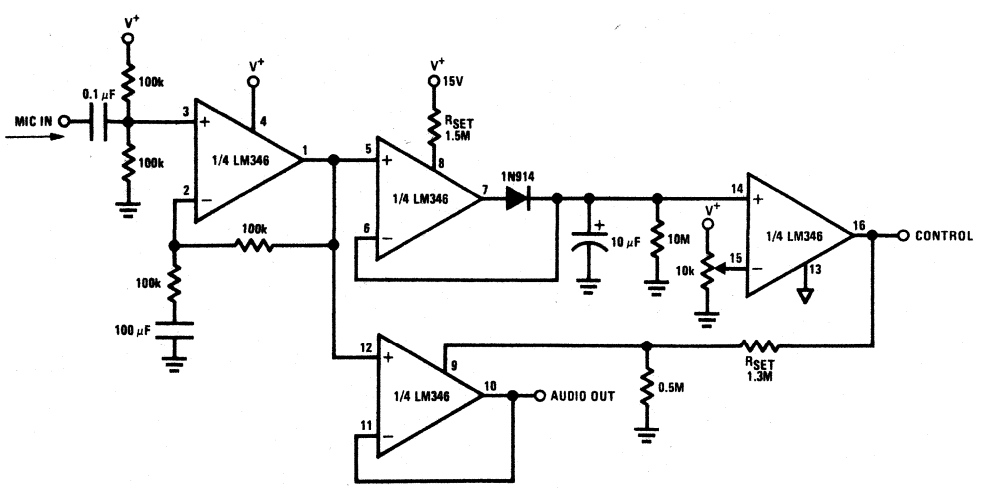
- For better performance, use a matched NPN pair.

Circuit Shutdown



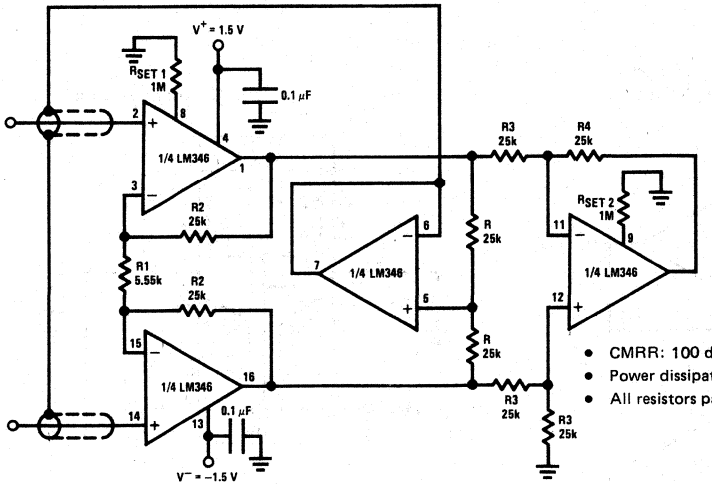
- By pulling the SET pin(s) to V^- the op amp(s) shuts down and its output goes to a high impedance state. According to this property, the LM346 can be used as a very low speed analog switch.

Voice Activated Switch and Amplifier



Miscellaneous Applications (Continued)

X10 Micropower Instrumentation Amplifier with Buffered Input Guarding



- CMRR: 100 dB (typ)
- Power dissipation: 0.4 mW
- All resistors part of RA201 array

National Semiconductor

RA201 Precision Instrumentation Amplifier Resistor Network

General Description

The RA201 is a family of precision instrumentation amplifier networks. This device, when combined with 3 operational amplifiers, provides a precision instrumentation amplifier with common-mode rejection up to 100 dB. All gain setting resistors are provided within the device. This feature assures excellent thermal tracking and thermal matching of all resistors. This network is manufactured using a high stability thin-film technology. Thin-film resistors provide tracking temperature coefficients of better than 5 ppm/°C. The thin-film resistors are laser trimmed to guarantee resistor matching to 0.05% for the RA201-2, and 0.1% for the RA201-1.

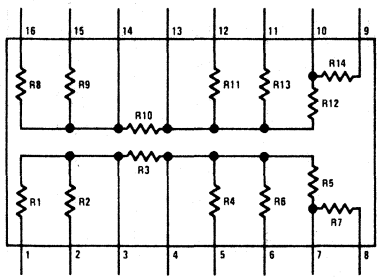
Other applications include process control interfacing and precision decade dividers.

Features

- Gain programmable
- Matching accuracies to 0.05%
- Matching temperature coefficient to 5 ppm/°C
- Absolute temperature coefficient to 80 ppm/°C
- Close thermal proximity of all resistors
- Standard dual-in-line package
- Low-cost

Connection Diagrams

Dual-In-Line Package

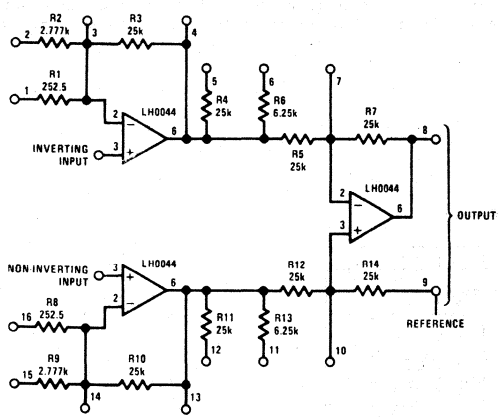


TOP VIEW

R1 = 252.525 . . Ω
R2 = 2.777 . . . kΩ
R3 = 25k
R4 = 25k
R5 = 25k
R6 = 6.25k
R7 = 25k
R8 = 252.525 . . . Ω
R9 = 2.777 . . . kΩ
R10 = 25k
R11 = 25k
R12 = 25k
R13 = 6.25k
R14 = 25k

R3:R2 = 9:1
R3:R1 = 99:1
R3||R2 = 2.50k
R3||R1 = 250.0Ω
R5||R6 = 5.0k

Typical Applications



Overall Gain	Input Stage Gain	Output Stage Gain	Jumper Pins on RA201
X1	X1	X1	–
X2	X1	X2	5 to 7, 12 to 10
X5	X1	X5	6 to 7, 11 to 10
X10	X10	X1	2 to 15
X20	X10	X2	2 to 15, 5 to 7, 12 to 10
X50	X10	X5	2 to 15, 6 to 7, 11 to 10
X100	X100	X1	1 to 16
X200	X100	X2	1 to 16, 5 to 7, 12 to 10
X500	X100	X5	1 to 16, 6 to 7, 11 to 10
X995	X199	X5	1 to 14, 6 to 7, 11 to 10

Precision Instrumentation Amplifier

Absolute Maximum Ratings

Rated Voltage Between Sections	200V
Rated Voltage Across Resistors	(Note 1)
Package Power Dissipation at 25°C (See Curve)	2.0W
Individual Resistor Power at 25°C	0.25W
Operating Temperature Range	
RA201-1N, RA201-2N	−25°C to +85°C
RA201-1D, RA201-2D	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A = 25°C (Note 2)

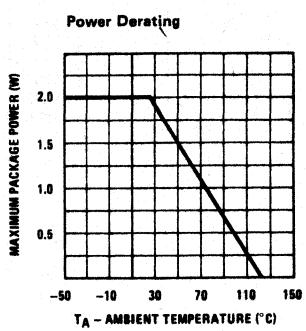
PARAMETER	CONDITIONS; RESISTORS TESTED	TYP	RA201-2 MAX	RA201-1 MAX	UNITS
Input Stage x10	R2:R3	1:9	±0.05	±0.1	%
	(R2||R9):(R3||R10)	1:9	±0.05	±0.1	%
Input Stage x100	R1:R3	1:99	±1	±1	%
	(R8||R1):(R3||R10)	1:99	±1	±1	%
Output Stage x1	R7:R5	1:1	±0.05	±0.1	%
	R14:R12	1:1	±0.05	±0.1	%
Output Stage x2	(R4||R5):R7	1:2	±0.05	±0.1	%
	(R12||R11):R14	1:2	±0.05	±0.1	%
Output Stage x5	(R6||R5):R7	1:5	±0.05	±0.1	%
	(R12||R13):R14	1:5	±0.05	±0.1	%
Output Stage CMRR	(R7:R5):(R14:R12), (Note 3)	1:1	±0.05	±0.1	%
Absolute Tolerance	R3	25 kΩ	±5	±5	%
Absolute Tempco		80			ppm/°C

Note 1: Rated voltage is limited by the individual resistor power rating of 0.25W. For example, a 25k resistor could withstand a maximum of $V = \sqrt{(0.25)(25{,}000)} = 79V$. This rating may need to be reduced to be consistent with maximum package power if several resistors are dissipating power simultaneously.

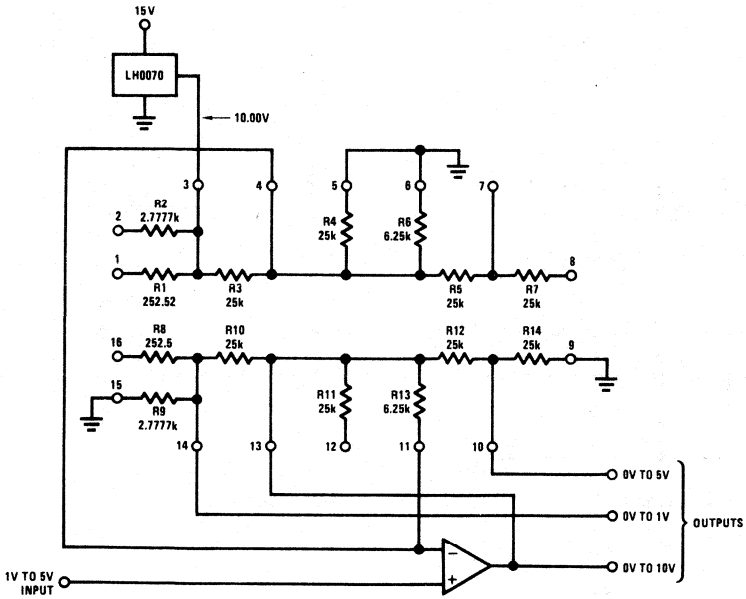
Note 2: Resistor ratios shown apply at T_A = 25°C; for $T_{MIN} \leq T_A \leq T_{MAX}$ the ratio tolerances are double the specifications shown.

Note 3: This test guarantees the CMRR contributed by resistance mismatch. In low gain applications, all 3 amplifiers contribute strongly to the overall CMRR. In high gain applications, the degradation due to resistor mismatch and output stage CMRR are divided by the gain of the input stage.

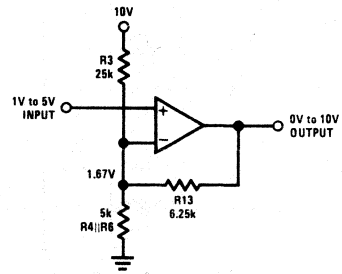
Typical Performance Characteristics



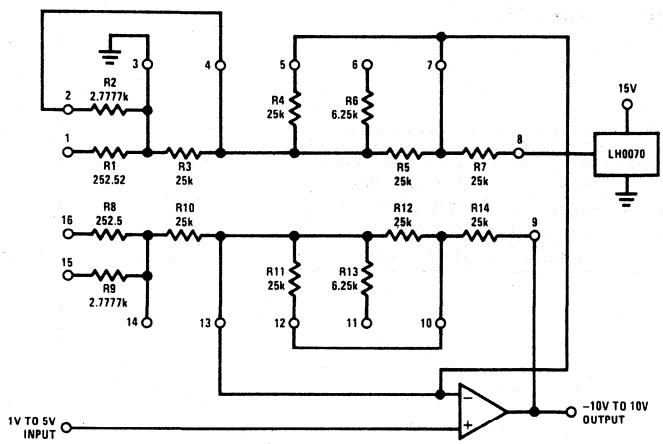
Applications Information



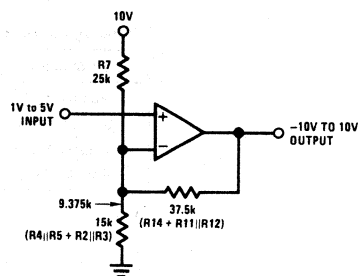
RA201 Process Control Interface No. 1



Equivalent Circuit

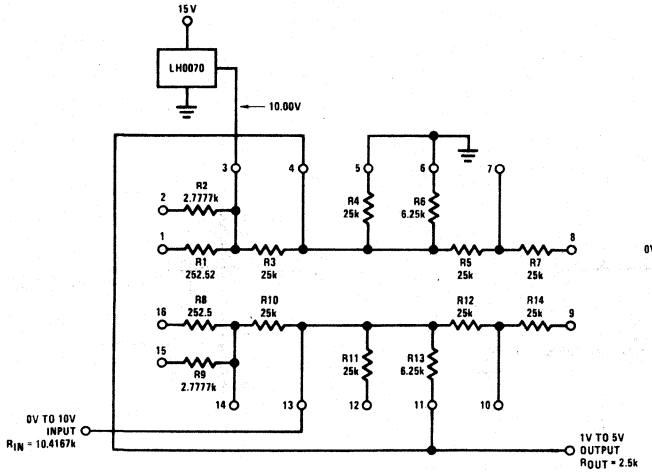


RA201 Process Control Interface No. 2

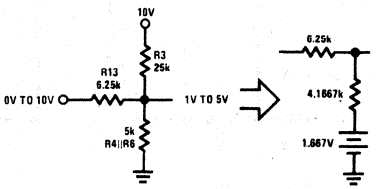


Equivalent Circuit

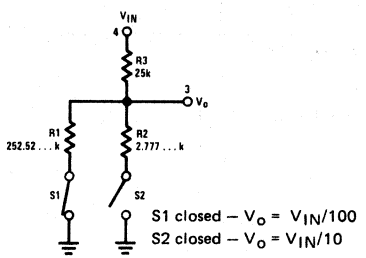
Applications Information (Continued)



RA201 Process Control Interface No. 3



Equivalent Circuit



Precision Decade Divider

Ordering Information

Part Number	Accuracy	Package	Temperature Range
RA201-1D	0.1%	D16C	–55°C to +125°C
RA201-2D	0.2%	D16C	–55°C to +125°C
RA201-1N	0.1%	N16A	–25°C to +85°C
RA201-2N	0.2%	N16A	–25°C to +85°C

Section 4

Analog Switches

4

Section Contents

National Semiconductor

Analog Switches

AH0120/AH0130/AH0140/AH0150/AH0160 Series Analog Switches

General Description

The AH0100 series represents a complete family of junction FET analog switches. The inherent flexibility of the family allows the designer to tailor the device selection to the particular application. Switch configurations available include dual DPST, dual SPST, DPDT, and SPDT. $r_{ds(ON)}$ ranges from 10 ohms through 100 ohms. The series is available in both 14 lead flat pack and 14 lead cavity DIP. Important design features include:

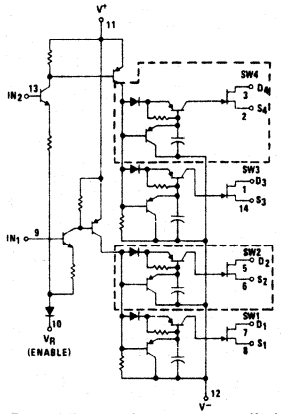
- TTL/DTL and RTL compatible logic inputs
- Up to 20V p-p analog input signal
- $r_{ds(ON)}$ less than 10Ω (AH0140, AH0141, AH0145, AH0146)
- Analog signals in excess of 1 MHz
- "OFF" power less than 1 mW
- Gate to drain bleed resistors eliminated
- Fast switching, t_{ON} is typically 0.4 μs, t_{OFF} is 1.0 μs
- Operation from standard op amp supply voltages, ±15V, available (AH0150/AH0160 series)
- Pin compatible with the popular DG 100 series

The AH0100 series is designed to fulfill a wide variety of analog switching applications including commutators, multiplexers, D/A converters, sample and hold circuits, and modulators/demodulators. The AH0100 series is guaranteed over the temperature range -55°C to +125°C; whereas, the AH0100C series is guaranteed over the temperature range -25°C to +85°C

4

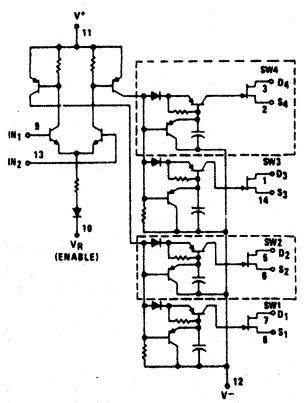
Schematic Diagrams

DUAL DPST and DUAL SPST



Note: Dotted line portions are not applicable to the dual SPST.

DPDT (diff.) and SPDT (diff.)

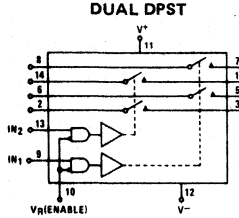


Note: Dotted line portions are not applicable to the SPDT (differential).

Order any of the devices below using the part number with a D or F suffix. See NS Packages D14A or F14A. AH0133C, AH0134C, AH0151C, AH0152C available in N Package also.

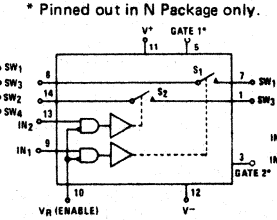
Logic and Connection Diagrams

DUAL DPST



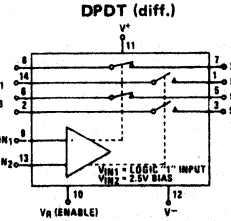
HIGH LEVEL (±10V)
AH0140 (10Ω)
AH0129 (30Ω)
AH0126 (80Ω)
MEDIUM LEVEL (±7.5V)
AH0153 (15Ω)
AH0154 (50Ω)

DUAL SPST
* Pinned out in N Package only.



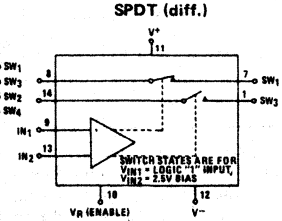
HIGH LEVEL (±10V)
AH0141 (10Ω)
AH0133 (30Ω)
AH0134 (80Ω)
MEDIUM LEVEL (±7.5V)
AH0151 (15Ω)
AH0152 (50Ω)

DPDT (diff.)



HIGH LEVEL (±10V)
AH0145 (10Ω)
AH0139 (30Ω)
AH0142 (80Ω)
MEDIUM LEVEL (±7.5V)
AH0163 (15Ω)
AH0164 (50Ω)

SPDT (diff.)



HIGH LEVEL (±10V)
AH0146 (10Ω)
AH0144 (30Ω)
AH0143 (80Ω)
MEDIUM LEVEL (±7.5V)
AH0161 (15Ω)
AH0162 (50Ω)

Absolute Maximum Ratings

		High Level	Medium Level
Total Supply Voltage ($V^+ - V^-$)		36V	34V
Analog Signal Voltage ($V^+ - V_A$ or $V_A - V^-$)		30V	25V
Positive Supply Voltage to Reference ($V^+ - V_R$)		25V	25V
Negative Supply Voltage to Reference ($V_R - V^-$)		22V	22V
Positive Supply Voltage to Input ($V^+ - V_{IN}$)		25V	25V
Input Voltage to Reference ($V_{IN} - V_R$)		±6V	±6V
Differential Input Voltage ($V_{IN} - V_{IN2}$)		±6V	±6V
Input Current, Any Terminal		30 mA	30 mA
Power Dissipation		See Curve	
Operating Temperature Range	AH0100 Series	−55°C to +125°C	
	AH0100C Series	−25°C to +85°C	
Storage Temperature Range		−65°C to +150°C	
Lead Temperature (Soldering, 10 sec)		300°C	

Electrical Characteristics for "HIGH LEVEL" Switches (Note 1)

PARAMETER	SYMBOL	DEVICE TYPE: DUAL DPST	DUAL SPST	DPDT (DIFF)	SPDT (DIFF)	CONDITIONS: $V^+ = 12.0V$, $V^- = -18.0V$, $V_R = 0.0V$		LIMITS: TYP	MAX	UNITS
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	T_A = 25°C	2.0	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	T_A = 25°C	.01	.1	µA
							Over Temp. Range		2.0	µA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	−1.0	−1.8	mA
							Over Temp. Range		−2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	−1.0	−1.4	mA
							Over Temp. Range		−1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				V_{IN1} V_{IN2} 0.8V	T_A = 25°C	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				V_{IN1} = V_{IN2} 0.8V	T_A = 25°C	−1.0	−10	µA
							Over Temp. Range		−25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				V_{IN1} = V_{IN2} 0.8V	T_A = 25°C	−1.0	−10	µA
							Over Temp. Range		−25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0126	AH0134	AH0142	AH0143	V_D = 10V	T_A = 25°C	45	80	Ω
						I_D = 1 mA	Over Temp. Range		150	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0129	AH0133	AH0139	AH0144	V_D 10V	T_A = 25°C	25	30	Ω
						I_D = 1 mA	Over Temp. Range		60	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0140	AH0141	AH0145	AH0146	V_D = 10V	T_A = 25°C	8	10	Ω
						I_F = 1 mA	Over Temp. Range		20	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -10V$	T_A = 25°C	.01	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	V_{DS} = ±20V	T_A = 25°C	0.8	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0140	AH0141	AH0145	AH0146	V_{DS} = ±20V	T_A = 25°C	4	10	nA
							Over Temp. Range		1.0	µA
Switch Turn-ON Time	t_{ON}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit V_A = ±10V	T_A = 25°C	0.5	0.8	µs
Switch Turn-ON Time	t_{ON}	AH0140	AH0141	AH0145	AH0146	See Test Circuit V_A = ±10V	T_A = 25°C	0.8	1.0	µs
Switch Turn-OFF Time	t_{OFF}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit V_A = ±10V	T_A = 25°C	0.9	1.6	µs
Switch Turn-OFF Time	t_{OFF}	AH0140	AH0141	AH0145	AH0146	See Test Circuit V_A = ±10V	T_A = 25°C	1.1	2.5	µs

Note 1: Unless otherwise specified these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for T_A = 25°C.

Note 2: For the DPST and Dual DPST, the ON condition is for V_{IN} = 2.5V; the OFF condition is for V_{IN} = 0.8V. For the differential switches and SW1 and 2 ON, V_{IN2} = 2.5V, V_{IN1} = 3.0V. For SW3 and 4 ON, V_{IN2} = 2.5V, V_{IN1} = 2.0V.

Electrical Characteristics for "MEDIUM LEVEL" Switches (Note 1)

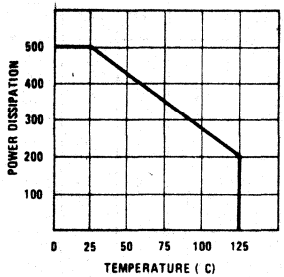
PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DUAL DPDT	SPDT (DIFF)	$V^+ = +15.0V$, $V^- = -15V$, $V_R = 0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	20	60	μA
							Over Temp. Range		120	μA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	0.1	μA
							Over Temp. Range		2	μA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.8	mA
							Over Temp. Range		-2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.4	mA
							Over Temp. Range		-1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				V_{IN1} V_{IN2} 0.8V	$T_A = 25°C$	1.0	10	μA
							Over Temp. Range		25	μA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				V_{IN1} V_{IN2} 0.8V	$T_A = 25°C$	-1.0	-10	μA
							Over Temp. Range		-25	μA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				V_{IN1} V_{IN2} 0.8V	$T_A = 25°C$	-1.0	-10	μA
							Over Temp. Range		-25	μA
Switch ON Resistance	$r_{ds(ON)}$	AH0153	AH0151	AH0163	AH0161	V_D 7.5V, I_D 1 mA	$T_A = 25°C$	10	15	Ω
							Over Temp. Range		30	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0154	AH0152	AH0164	AH0162	V_D 7.5V, I_D 1 mA	$T_A = 25°C$	45	50	Ω
							Over Temp. Range		100	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				V_D V_S -7.5V	$T_A = 25°C$	.01	2	nA
							Over Temp. Range		500	nA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0153	AH0151	AH0163	AH0161	V_{DS} ±15V	$T_A = 25°C$	5	10	nA
							Over Temp. Range		1.0	μA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0154	AH0152	AH0164	AH0162	V_{DS} ±15.0V	$T_A = 25°C$	1.0	2.0	nA
							Over Temp. Range		200	nA
Switch Turn-ON Time	t_{ON}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.8	1.0	μs
Switch Turn-ON Time	t_{ON}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.5	0.8	μs
Switch Turn-OFF Time	t_{OFF}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		1.1	2.5	μs
Switch Turn-OFF Time	t_{OFF}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.9	1.5	μs

Note 1: Unless otherwise specified, these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

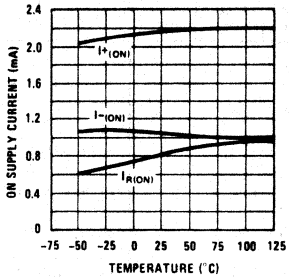
Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

Typical Performance Characteristics

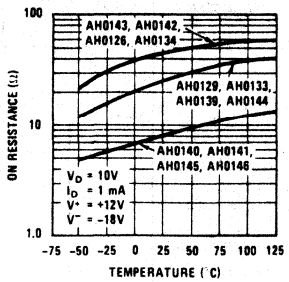
Power Dissipation vs Temperature



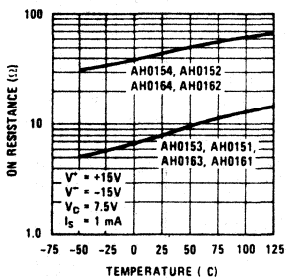
ON Supply Current vs Temperature



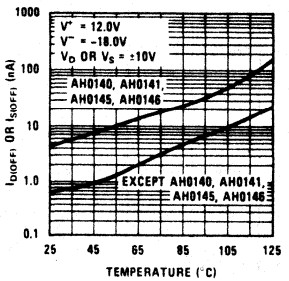
rds(ON) vs Temperature AH0120 thru AH0140 Series



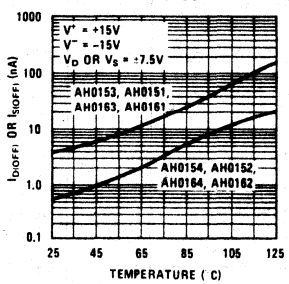
rds(ON) vs Temperature AH0150/AH0160 Series



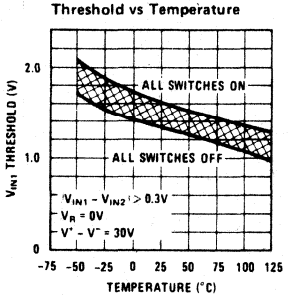
Leakage Current vs Temperature AH0120, AH0130, & AH0140



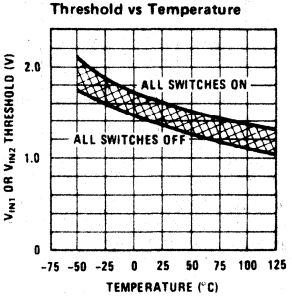
Leakage Current vs Temperature AH0150 & AH0160



Single Ended Switch Input Threshold vs Temperature

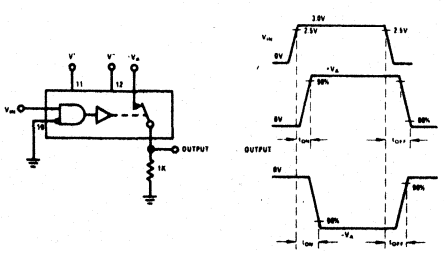


Differential Switch Input Threshold vs Temperature

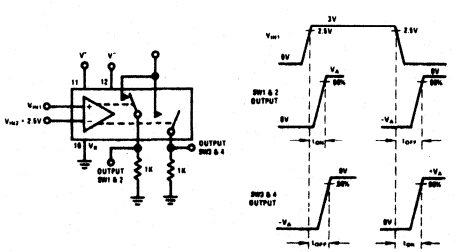


Switching Time Test Circuits

Single Ended Input



Differential Input



Applications Information

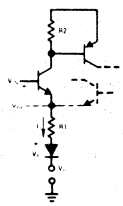
1. INPUT LOGIC COMPATIBILITY

A. Voltage Considerations

In general, the AH0100 series is compatible with most DTL, TTL, and RTL logic families. The ON-input threshold is determined by the V_{BE} of the input transistor plus the V_f of the diode in the emitter leg, plus I x R_1, plus V_R. At room temperature and V_R = 0V, the nominal ON threshold is: 0.7V + 0.7V + 0.2V, = 1.6V. Over temperature and manufacturing tolerances, the threshold may be as high as 2.5V and as low as 0.8V. The rules for proper operation are:

$V_{IN} - V_R \geq 2.5V$ All switches ON

$V_{IN} - V_R \leq 0.8V$ All switches OFF



B. Input Current Considerations

$I_{IN(ON)}$, the current drawn by the driver with V_{IN} = 2.5V is typically 20 μA at 25°C and is guaranteed less than 120 μA over temperature. DTL, such as the DM930 series can supply 180 μA at logic "1" voltages in excess of 2.5V. TTL output levels are comparable at 400 μA. The DTL and TTL can drive the AH0100 series directly. However, at low temperature, DC noise margin in the logic "1" state is eroded with DTL. A pull-up resistor of 10 kΩ is recommended when using DTL over military temperature range.

If more than one driver is to be driven by a DM930 series (6K) gate, an external pull-up resistor should be added. The value is given by:

$$R_P = \frac{11}{N-1} \text{ for } N > 2$$

where:

R_P = value of the pull-up resistor in kΩ

N = number of drivers.

C. Input Slew Rate

The slew rate of the logic input must be in excess of 0.3V/μs in order to assure proper operation of the analog switch. DTL, TTL, and RTL output rise times are far in excess of the minimum slew rate requirements. Discrete logic designs, however, should include consideration of input rise time.

2. ENABLE CONTROL

The application of a positive signal at the V_R terminal will open all switches. The V_R (ENABLE) signal must be capable of rising to within 0.8V of $V_{IN(ON)}$ in the OFF state and of sinking $I_{R(ON)}$ milliamps in the ON state (at $V_{IN(ON)} - V_R >$ 2.5V). The V_R terminal can be driven from most TTL and DTL gates.

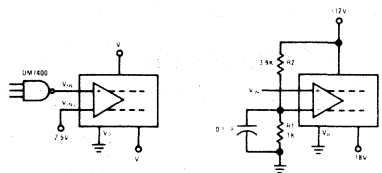
3. DIFFERENTIAL INPUT CONSIDERATIONS

The differential switch driver is essentially a differential amplifier. The input requirements for proper operation are:

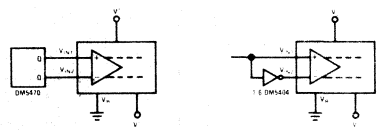
$$|V_{IN1} - V_{IN2}| \geq 0.3V$$

$$2.5 \leq (V_{IN1} \text{ or } V_{IN2}) - V_R \leq 5V$$

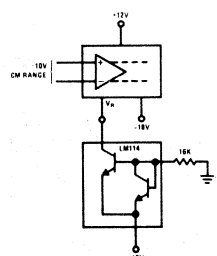
The differential driver may be furnished by a DC level as shown below. The level may be derived from a voltage divider to V^+ or the 5V V_{CC} of the DTL logic. In order to assure proper operation, the divider should be "stiff" with respect to I_{IN2}. Bypassing R1 with a 0.1 μF disc capacitor will prevent degradation of t_{ON} and t_{OFF}.



Alternatively, the differential driver may be driven from a TTL flip-flop or inverter.



Connection of a 1 mA current source between V_R and V^- will allow operation over a ±10V common mode range. Differential input voltage must be less than the 6V breakdown, and input threshold of 2.5V and 300mV differential overdrive still prevail.



4. ANALOG VOLTAGE CONSIDERATIONS

The rules for operating the AH0100 series at supply voltages other than those specified essentially breakdown into OFF and ON considerations. The OFF considerations are dictated by the maximum negative swing of the analog signal and the pinch off of the JFET switch. In the OFF state, the gate of the FET is at $V^- + V_{BE} + V_{SAT}$ or about 1.0V above the V^- potential. The maximum V_P of the FET switches is 7V. The most negative analog voltage, V_A, swing which can be accommodated for any given supply voltage is:

$$|V_A| \leq |V^-| - V_P - V_{BE} - V_{SAT} \text{ or}$$

$$|V_A| \leq |V^-| - 8.0 \text{ or } |V^-| \geq |V_A| + 8.0V$$

For the standard high level switches, $V_A \leq |-18| + 8 = -10V$. The value for V^+ is dictated by the maximum positive swing of the analog input voltage. Essentially the collector to base junction of the turn-on PNP must remain reversed biased for all positive value of analog input voltage. The base of the PNP is at $V^+ - V_{SAT} - V_{BE}$ or $V^+ - 1.0V$. The PNP's collector base junction should have at least 1.0V reverse bias. Hence, the most positive analog voltage swing which may be accommodated for a given value of V^+ is:

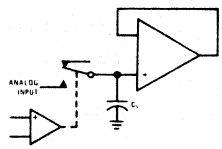
$$V_A \leq V^+ - V_{SAT} - V_{BE} - 1.0V \text{ or}$$

$$V_A \leq V^+ - 2.0V \text{ or } V^+ \geq V_A + 2.0V$$

For the standard high level switches, $V_A = 12 - 2.0V = +10V$.

5. SWITCHING TRANSIENTS

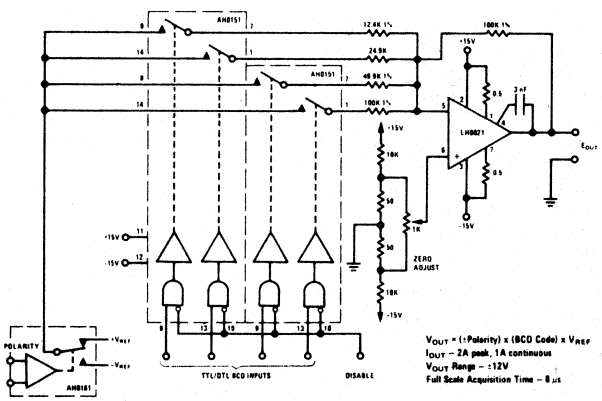
Due to charge stored in the gate-to-source and gate-to-drain capacitances of the FET switch, transients may appear in the output during switching. This is particularly true during the OFF to ON transition. The magnitude and duration of the transient may be minimized by making source and load impedance levels as small as practical.



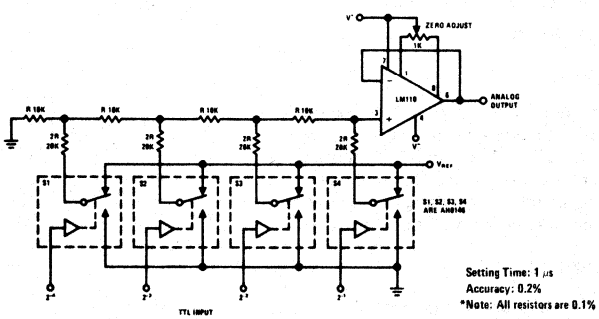
Furthermore, transients may be minimized by operating the switches in the differential mode; i.e., the charge delivered to the load during the ON to OFF transition is, to a large extent, cancelled by the OFF to ON transition.

Typical Applications

Programmable One Amp Power Supply

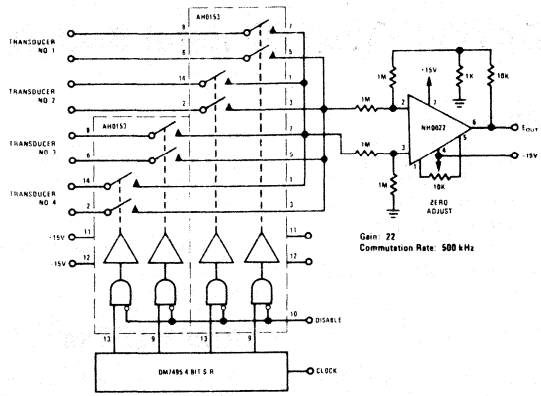


Four to Ten Bit D to A Converter (4 Bits Shown)

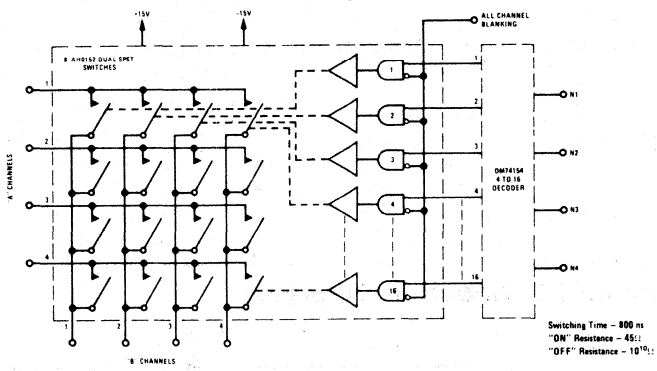


Typical Applications (Continued)

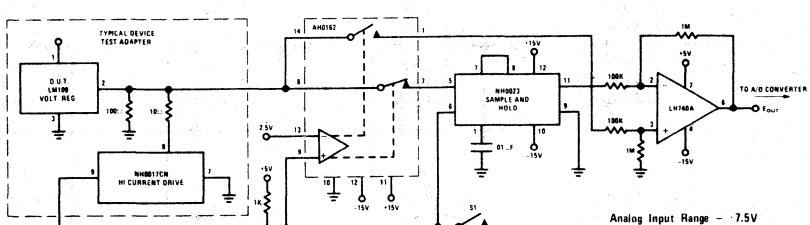
Four Channel Differential Transducer Commutator



4 x 4 Cross Point Analog Switch



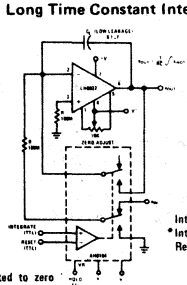
Delta Measurement System for Automatic Linear Circuit Tester



Note: S1 must be open for 50μs min to take first reading with I_L = 50 mA. Second reading is taken with S2 closed. With S1 and other set-up forcing functions under computer control, system will measure line and load regulation on voltage regulators, voltage gain, offset current, CMRR and PSRR on op amps as well as other circuits requiring measurement of the change of a parameter with the change of a forcing function.

Analog Input Range – ±7.5V
E_{OUT} = 10x (Analog Input 2 – Analog Input 1)
Error Rate – 0.01% F.S./sec

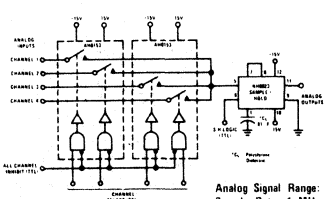
Precision Long Time Constant Integrator with Reset



Integration Internal = 10 sec
*Integration Error = 100μV
Reset Time: 30μs

*Note: V_{OS} adjusted to zero

Four Channel Commutator



Analog Signal Range: $15V_{P-P}$
Sample Rate: 1 MHz
Acquisition Time: 20μs
Drift Rate: 0.5 mV/sec

National Semiconductor

CD4016M/CD4016C Quad Bilateral Switch

General Description

The CD4016M/CD4016C is a quad bilateral switch which utilizes P-channel and N-channel complementary MOS (CMOS) circuits to provide an extremely high "OFF" resistance and low "ON" resistance switch. The switch will pass signals in either direction and is extremely useful in digital switching.

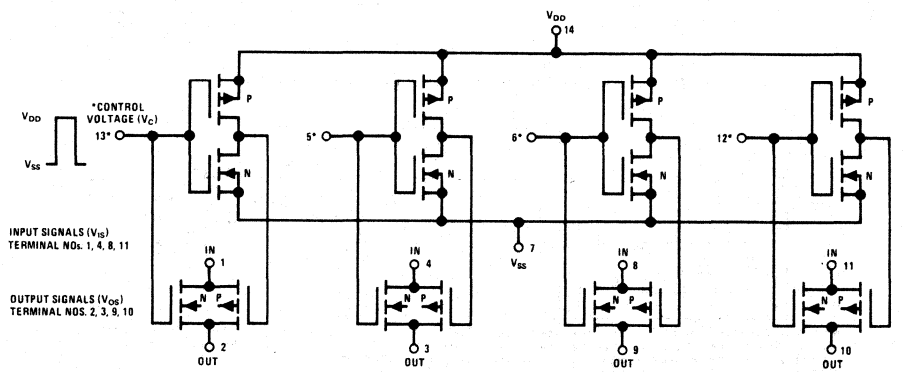
Features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{CC} typ.
■ Wide range of digital and analog levels	±7.5 V_{PEAK}
■ Low "ON" resistance	300Ω typ. $V_{DD} - V_{SS}$ = 15V
■ Matched switch characteristics	ΔR_{ON} = 40Ω typ.
■ High "ON/OFF" output voltage ratio	65 dB typ. @ f_{is} = 10 kHz R_L = 10k
■ High degree of linearity	.5% distortion typ. @ f_{is} = 1 kHz
■ Extremely low leakage	V_{is} = 5 V_{p-p} $V_{DD} - V_{SS}$ = 10V R_L = 10 kΩ
■ Transmits frequencies up to 10 MHz	

Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog to digital/digital to analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

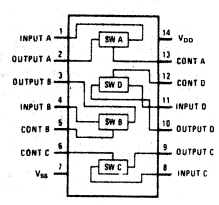
Schematic and Connection Diagrams



Note 1: All switch P-channel substrates are internally connected to terminal No. 14.
Note 2: All switch N-channel substrates are internally connected to terminal No. 7.

Signal-level range: $V_{SS} < V_{is} > V_{DD}$

Normal operation: Control-line biasing, switch ON V_C "1" = V_{DD}, switch OFF V_C "0" = V_{SS}



Order Number CD4016MJ or CD4016CJ
See NS Package J14A

Order Number CD4016CN
See NS Package N14A

Order Number CD4016MW
See NS Package W14A

Absolute Maximum Ratings

Voltage at Any Pin (Note 1) V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range CD4016M −55°C to +125°C
CD4016C −40°C to +85°C
Storage Temperature Range −65°C to +150°C
Package Dissipation 500mW
Lead Temperature (Soldering, 10 seconds) 300°C
Operating V_{DD} Range V_{SS} + 3V to V_{SS} + 15V

Electrical Characteristics CD4016M

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS −55°C MIN	−55°C TYP	−55°C MAX	25°C MIN	25°C TYP	25°C MAX	125°C MIN	125°C TYP	125°C MAX	UNITS
Quiescent Dissipation per Package	P_T	V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 GND; V_{is} 1, 4, 8, 11 < +10; V_{os} 2, 3, 9, 10 < +10			5		0.1	5			300	μW
All Switches "ON"	P_T	V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 +10; $V_{is} = V_{OS}$ 1-4, 8-11 < +10			5		0.1	5			300	μW
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		−1.7			−1.5			−1.3		V
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
"ON" Resistance	R_{ON}	R_L = 10kΩ; $V_C = V_{DD}$, V_{SS}, V_{is}: +7.5V		120	360		200	400		300	600	Ω
		+7.5V, −7.5V, −7.5V		120	360		200	400		300	600	Ω
		±0.25V		130	775		280	850		470	1230	Ω
		+5V		130	600		250	660		400	960	Ω
		+5V, −5V, −5V		130	600		250	660		400	960	Ω
		±0.25V		325	1870		580	2000		900	2600	Ω
		+15V		120	360		200	400		300	600	Ω
		+15V, 0V, +0.25V		120	360		200	400		300	600	Ω
		9.3V		150	775		300	850		490	1230	Ω
		+10V		130	600		250	660		400	960	Ω
		+10V, 0V, +0.25V		130	600		250	660		400	960	Ω
		5.6V		300	1870		560	2000		880	2600	Ω
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V, −7.5V, +7.5V					10					Ω
		+5V, −5V, +5V					15					Ω
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz; +5V, −5V, 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage—Switch "OFF" (Effective "OFF" Resistance)		V_{DD} +7.5V, V_C −7.5V, V_{SS} −7.5V, V_{is} +7.5V					±100					pA
		V_{DD} +7.5V, V_C −7.5V, V_{SS} −7.5V, V_{is} +7.5V					±100					pA
		V_{DD} +5V, V_C −5V, V_{SS} −5V, V_{is} +5V					(Note 2)	125				nA
		V_{DD} +5V, V_C −5V, V_{SS} −5V, V_{is} −5V					(Note 2)	125				nA
Frequency Response—Switch "ON" (Sine Wave Input)		$V_C = V_{DD}$ = +5V, V_{SS} = −5V; R_L = 1 kΩ, V_{is} = 5V(p-p); $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −3 dB					40					MHz
Feedthrough Switch "OFF"		V_{DD} = +5V, $V_C = V_{SS}$ = −5V; $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −50 dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at −50 dB)		R_L = 1 kΩ, $V_{is}(A)$ = 5V(p-p); $V_C(A) = V_{DD}$ = +5V, $V_C(B) = V_{SS}$ = −5V; $20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)}$ = −50 dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = −5V					4					pF
Output	C_{OS}						4					pF
Feedthrough	C_{IOS}						0.2					pF
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD}$ = +10V, V_{SS} = GND, C_L = 15 pF, V_{is} = 10V (square wave), $t_r = t_f$ = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} < V_{DD}$; $V_{DD} - V_{SS}$ = 15V, 10V, 5V; I_{IS} = 10 μA	0.7		2.9	0.5	1.5	2.7	0.2		2.4	V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V; $V_C < V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk — Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V, V_C = 10V (square wave), R_L = 10 kΩ					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc}$ = 20 ns, $V_{is} < 10V$, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1 kΩ, C_L = 15 pF, V_C = 10V (square wave), $t_r = t_f$ = 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on. **Note 2:** ±10 x 10^{-3}. **Note 3:** Symmetrical about 0V.

Electrical Characteristics CD4016C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS –40°C MIN	–40°C TYP	–40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C TYP	85°C MAX	UNITS
Quiescent Dissipation per Package	P_T	TERMINALS: V_{DD} 14 (+10 V); V_{SS} 7 (GND); V_C 5, 6, 12, 13 (GND); V_{is} 1, 4, 8, 11 (≤ +10); V_{os} 2, 3, 9, 10 (≤ +10)										
All Switches "OFF"					5		0.1	5			80	μW
All Switches "ON"		TERMINALS: V_{DD} 14 (+10 V); V_{SS} 7 (GND); V_C 5, 6, 12, 13 (+10 V); $V_{is} = V_{os}$ 1–4, 8–11 (≤ +10)			5		0.1	5			80	μW
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		−1.7			−1.5			−1.3		V
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
"ON" Resistance	R_{ON}	R_L = 10kΩ; $V_C = V_{DD}$, V_{SS}, V_{is}: +7.5V: 130 370 / 200 400 / 260 520; +7.5V, −7.5V, −7.5V: 130 370 / 200 400 / 260 520; ±0.25V: 160 790 / 280 850 / 400 1080; +5V: 150 610 / 250 660 / 340 840; +5V, −5V, −5V: 150 610 / 250 660 / 340 840; ±0.25V: 370 1900 / 580 2000 / 770 2380; +15V: 130 370 / 200 400 / 260 520; +15V, 0V, +0.25V: 130 370 / 200 400 / 260 520; 9.3V: 180 790 / 300 850 / 400 1080; +10V: 150 610 / 250 660 / 340 840; +10V, 0V, +0.25V: 150 610 / 250 660 / 340 2380; 5.6V: 350 1900 / 560 2000 / 750 2380										Ω
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V, −7.5V, ±7.5V: 10; +5V, −5V, ±5V: 15					10 / 15					Ω
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz; +5V, −5V, 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage–Switch "OFF" (Effective "OFF" Resistance)		V_{DD} +7.5V, $V_C = V_{SS}$ −7.5V, V_{is} +7.5V / −7.5V: ±100 / ±100; V_{DD} +5V, $V_C = V_{SS}$ −5V, V_{is} +5V / −5V: (Note 2) 125 / (Note 2) 125					±100 / ±100 / (Note 2) 125 / (Note 2) 125					pA / nA
Frequency Response–Switch "ON" (Sine Wave Input)		$V_C = V_{DD}$ = +5V, V_{SS} = −5V; R_L = 1 kΩ; V_{is} = 5V(p-p); $20 \log_{10} \frac{V_{os}}{V_{is}} = -3$ dB					40					MHz
Feedthrough Switch "OFF"		V_{DD} = +5V, $V_C = V_{SS}$ = −5V; $20 \log_{10} \frac{V_{os}}{V_{is}} = -50$ dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at −50 dB)		R_L = 1 kΩ; $V_{is}(A)$ = 5V(p-p); $V_C(A) = V_{DD}$ = +5V, $V_C(B) = V_{SS}$ = −5V; $20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50$ dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = −5V					4					pF
Output	C_{OS}						4					pF
Feedthrough	C_{IOS}						0.2					pF
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD}$ = +10V, V_{SS} = GND, C_L = 15 pF; V_{is} = 10V (square wave); $t_r = t_f$ = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} < V_{DD}$; $V_{DD} - V_{SS}$ = 15V, 10V, 5V; I_{IS} = 10 μA				0.5	1.5	2.7				V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V; $V_C < V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk – Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V; V_C = 10V (square wave); R_L = 10 kΩ					50					mV
Turn "ON" Propagation Delay	$t_{pHL}C$	t_{rC}, t_{fC} = 20 ns; $V_{is} < 10$V, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} 10V, V_{SS} = GND, R_L = 1 kΩ; C_L 15 pF; V_C 10V (square wave); t_r, t_f 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on. **Note 2:** $\pm 10 \times 10^{-3}$. **Note 3:** Symmetrical about 0V.

Typical ON Resistance Characteristics

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1 kΩ		R_L = 10 kΩ		R_L = 100 kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+5	0	860	+5	470	+5	450	+5
			600	0	580	0	800	0
R_{ON} (max.)	+5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON} (max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+5	−5	260	+5	250	+5	240	+5
			310	−5	250	−5	240	−5
R_{ON} (max.)	+5	−5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
R_{ON} (max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

*Variation from a perfect switch: R_{ON} = 0Ω.

National Semiconductor

CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

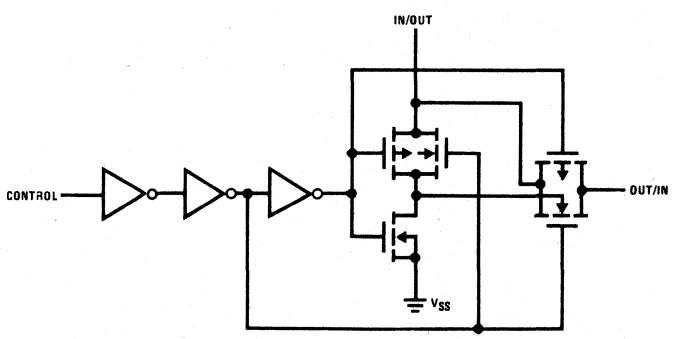
Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Wide range of digital and analog switching — ±7.5 V_{PEAK}
- "ON" resistance for 15V operation — 80Ω typ
- Matched "ON" resistance over 15V signal input — ΔR_{ON} = 5Ω typ
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB typ @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity — < 0.4% distortion typ @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage — 0.1 nA typ @ $V_{DD} - V_{SS}$ = 10V, T_A = 25°C
- Extremely high control input impedance — 10^{12}Ω typ
- Low crosstalk between switches — −50 dB typ @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON" — 40 MHz typ

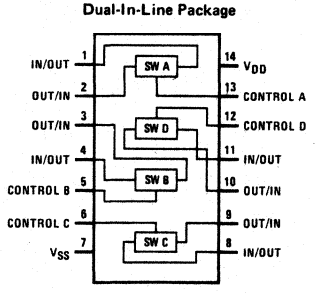
Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number CD4066MJ or CD4066CJ
See NS Package J14A

Order Number CD4066CN
See NS Package N14A

Order Number CD4066MW
See NS Package W14A

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

DC Electrical Characteristics CD4066BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		0.25		0.01	0.25		7.5	μA
	V_{DD} = 10V		0.5		0.01	0.5		15	μA
	V_{DD} = 15V		1.0		0.01	1.0		30	μA
Signal Inputs and Outputs									
R_{ON} "ON" Resistance	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
	V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
	V_{DD} = 5V		2000		270	2500		3500	Ω
	V_{DD} = 10V		400		120	500		550	Ω
	V_{DD} = 15V		220		80	280		320	Ω
ΔR_{ON} Δ "ON" Resistance Between any 2 of 4 Switches	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
	V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
	V_{DD} = 10V				10				Ω
	V_{DD} = 15V				5				Ω
I_{IS} Input or Output Leakage Switch "OFF"	V_C = 0 V_{IS} = 15V and 0V, V_{OS} = 0V and 15V		±50		±0.1	±50		±500	nA
Control Inputs									
V_{ILC} Low Level Input Voltage	V_{IS} = V_{SS} and V_{DD} V_{OS} = V_{DD} and V_{SS} I_{IS} = ±10 μA								
	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IHC} High Level Input Voltage	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V (see note 6)	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN} Input Current	V_{DD} − V_{SS} = 15V $V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA

DC Electrical Characteristics CD4066BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		7.5	μA
	V_{DD} = 10V		2.0		0.01	2.0		15	μA
	V_{DD} = 15V		4.0		0.01	4.0		30	μA

DC Electrical Characteristics (Continued) CD4066BC (Note 2)

Parameter	Conditions	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Signal Inputs and Outputs									
R_{ON} "ON" Resistance	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$ V_C = V_{DD}, V_{SS} to V_{DD}								
	V_{DD} = 5V		2000		270	2500		3200	Ω
	V_{DD} = 10V		450		120	500		520	Ω
	V_{DD} = 15V		250		80	280		300	Ω
ΔR_{ON} Δ"ON" Resistance Between Any 2 of 4 Switches	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$ V_{CC} = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
	V_{DD} = 10V				10				Ω
	V_{DD} = 15V				5				Ω
I_{IS} Input or Output Leakage Switch "OFF"	V_C = 0		±50		±0.1	±50		±200	nA
Control Inputs									
V_{ILC} Low Level Input Voltage	V_{IS} = V_{SS} and V_{DD} V_{OS} = V_{DD} and V_{SS} I_{IS} = ±10μA								
	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IHC} High Level Input Voltage	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V (See note 6)	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN} Input Current	V_{DD} − V_{SS} = 15V $V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

AC Electrical Characteristics T_A = 25°C, t_r = t_f = 20 ns and V_{SS} = 0V unless otherwise specified

Parameter		Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	V_C = V_{DD}, C_L = 50 pF, *(Figure 1)* R_L = 200k				
		V_{DD} = 5V		25	55	ns
		V_{DD} = 10V		15	35	ns
		V_{DD} = 15V		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	R_L = 1.0 kΩ, C_L = 50 pF, *(Figures 2 and 3)*				
		V_{DD} = 5V			125	ns
		V_{DD} = 10V			60	ns
		V_{DD} = 15V			50	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	R_L = 1.0 kΩ, C_L = 50 pF, *(Figures 2 and 3)*				
		V_{DD} = 5V			125	ns
		V_{DD} = 10V			60	ns
		V_{DD} = 15V			50	ns
	Sine Wave Distortion	V_C = V_{DD} = 5V, V_{SS} = −5V R_L = 10 kΩ, V_{IS} = 5 V_{p-p}, f = 1 kHz, *(Figure 4)*		0.4		%
	Frequency Response–Switch "ON" (Frequency at −3 dB)	V_C = V_{DD} = 5V, V_{SS} = −5V, R_L = 1 kΩ, V_{IS} = 5V_{p-p}, 20 Log_{10} V_{OS}/V_{OS}(1kHz)−dB, *(Figure 4)*		40		MHz

AC Electrical Characteristics (Continued)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

	Parameter	Conditions	Min	Typ	Max	Units
	Feedthrough – Switch "OFF" (Frequency at –50 dB)	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5V_{p-p}$, 20 Log_{10}, $V_{OS}/V_{IS} = -50$ dB, *(Figure 4)*		1.25		
	Crosstalk Between Any Two Switch (Frequency at –50 dB)	$V_{DD} = V_{C(1)} = 5V$; $V_{SS} = V_{C(2)} = -5V$, $R_L = 1\ k\Omega$, $V_{IS(A)} = 5V_{p-p}$, 20 Log_{10} $V_{OS(2)}/V_{IS(1)} = -50$ dB, *(Figure 5)*		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$ $R_{IN} = 1\ k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$pF *(Figure 6)*		150		mV_{p-p}
	Maximum Control Input	$R_L = 1\ k\Omega$, $C_L = 50$ pF, *(Figure 7)* $V_{OS(f)} = \frac{1}{2}V_{OS(1kHz)}$				
		$V_{DD} = 5V$		6.0		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		8.5		MHz
C_{is}	Signal Input Capacitance			8		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		8		pF
C_{ios}	Feedthrough Capacitance	$V_C = 0V$		0.5		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: Conditions for V_{IHC}:
a) $V_{IS} = V_{DD}$, I_{OS} = standard B series I_{OH} b) $V_{IS} = 0V$, I_{OS} = standard B series I_{OL}

AC Test Circuit and Switching Time Waveforms

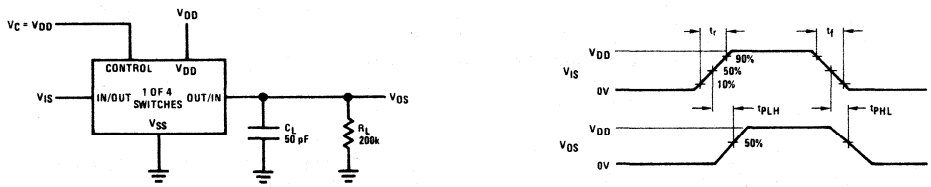


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

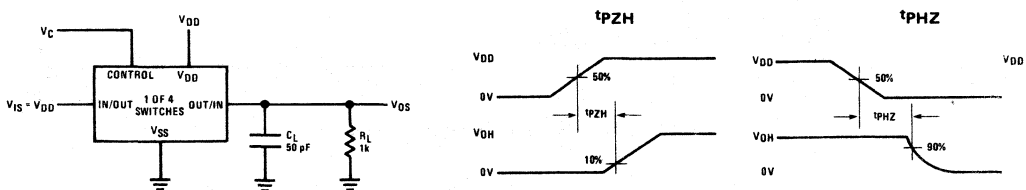


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

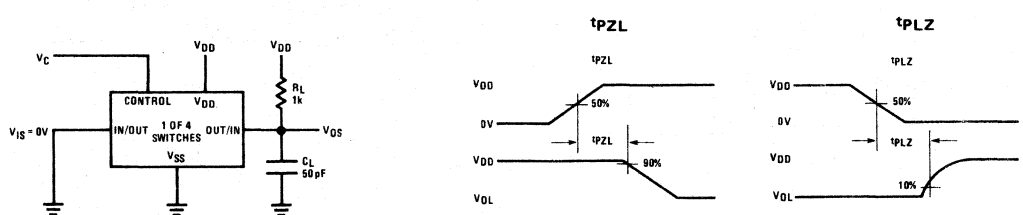
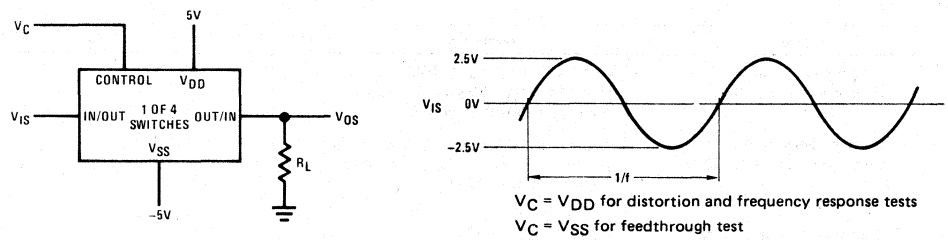


FIGURE 3. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuit and Switching Time Waveforms (Continued)



$V_C = V_{DD}$ for distortion and frequency response tests

$V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

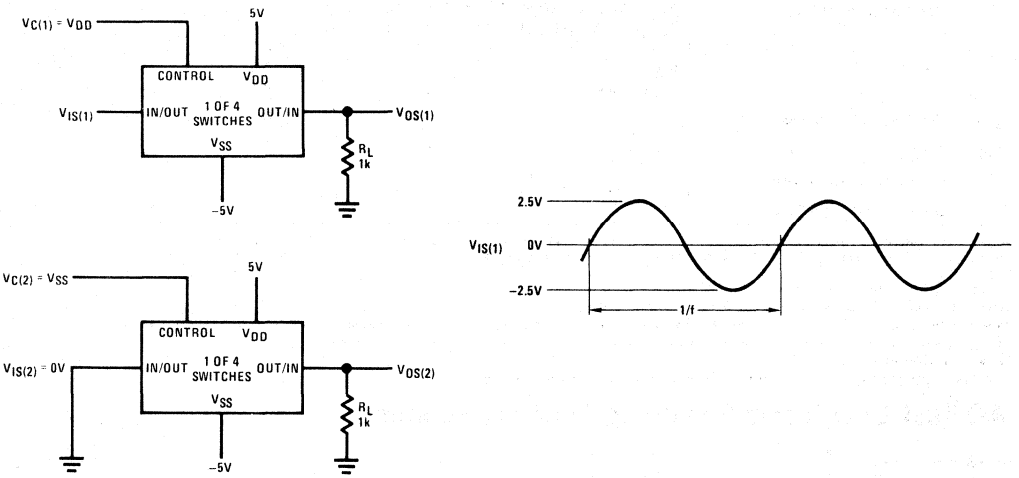


FIGURE 5. Crosstalk Between Any Two Switches

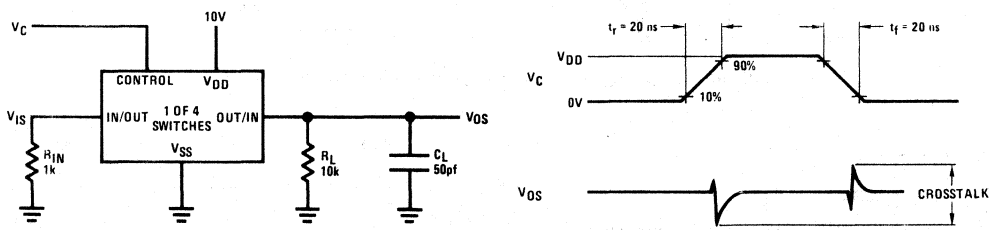


FIGURE 6. Crosstalk: Control Input to Signal Output

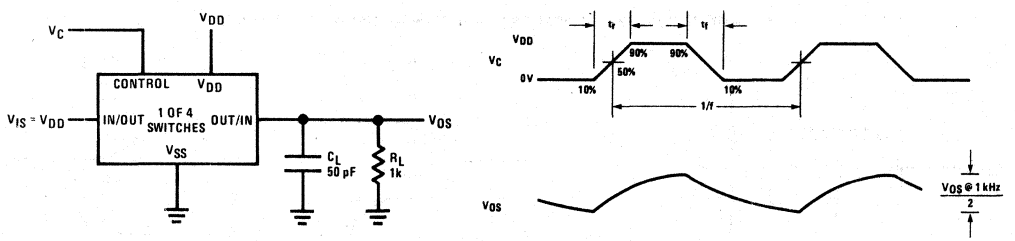
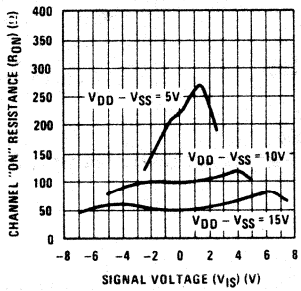


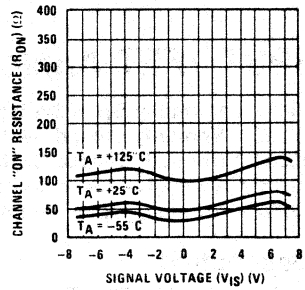
FIGURE 7. Maximum Control Input Frequency

Typical Performance Characteristics

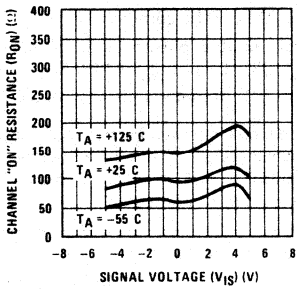
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



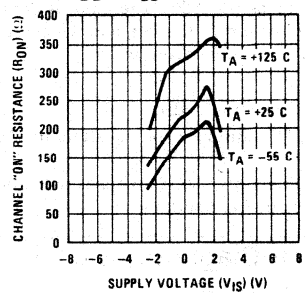
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$



Special Considerations

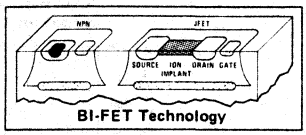
In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

National Semiconductor

Analog Switches



BI-FET Technology

Quad SPST JFET Analog Switches

LF11331/LF13331 4 Normally Open Switches with Disable
LF11332/LF13332 4 Normally Closed Switches with Disable
LF11333/LF13333 2 Normally Closed Switches and 2 Normally Open Switches with Disable
LF11201/LF13201 4 Normally Closed Switches
LF11202/LF13202 4 Normally Open Switches

General Description

These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

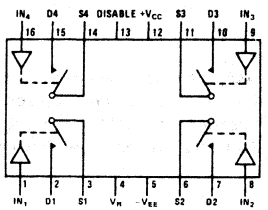
Features

- Analog signals are not loaded
- Constant "ON" resistance for signals up to ±10V and 100 kHz
- Pin compatible with CMOS switches with the advantage of blow out free handling
- Small signal analog signals to 50 MHz
- Break-before-make action $t_{OFF} < t_{ON}$
- High open switch isolation at 1.0 MHz −50 dB
- Low leakage in "OFF" state <1.0 nA
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package on LF11331, LF11332, LF11333
- LF11201 is pin compatible with DG201

These devices operate from ±15V supplies and swing a ±10V analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

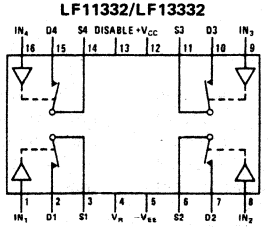
Connection Diagrams (Dual-In-Line Packages) (All Switches Shown are For Logical "0")

LF11331/LF13331



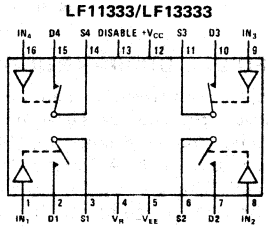
TOP VIEW

LF11332/LF13332



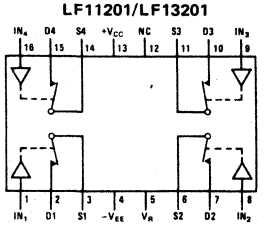
TOP VIEW

LF11333/LF13333



TOP VIEW

LF11201/LF13201

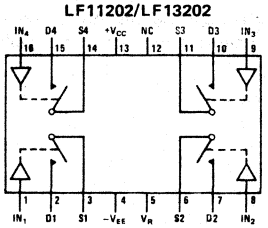


TOP VIEW

Order Number LF11201D, LF13201D, LF11202D, LF13202D, LF11331D, LF13331D, LF11332D, LF13332D, LF11333D, or LF13333D
See NS Package D16C

Order Number LF13201N, LF13202N, LF13331N, LF13332N, or LF13333N
See NS Package N16A

LF11202/LF13202



TOP VIEW

Test Circuit and Schematic Diagram

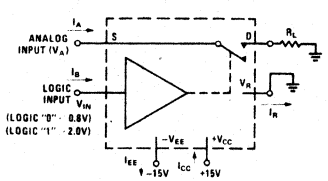


FIGURE 1. Typical Circuit for One Switch

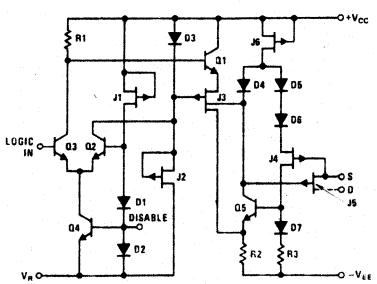


FIGURE 2. Schematic Diagram (Normally Open)

Absolute Maximum Ratings

Positive Supply – Negative Supply (V_{CC}–V_{EE})	36V
Reference Voltage	$V_{EE} \leq V_R \leq V_{CC}$
Logic Input Voltage	V_R –4.0V $\leq V_{IN} \leq V_R$ +6.0V
Analog Voltage	$V_{EE} \leq V_A \leq V_{CC}$ +6V; $V_A \leq V_{EE}$ +36V
Analog Current	$\|I_A\| <$ 20 mA
Power Dissipation (Note 1)	
Molded DIP (N Suffix)	500 mW
Cavity DIP (D Suffix)	900 mW

Operating Temperature Range	
LF11201, 2 and LF11331, 2, 3	–55°C to +125°C
LF13201, 2 and LF13331, 2, 3	0°C to +70°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Notes 2, 7)

SYMBOL	PARAMETER	CONDITIONS		LF11331/2/3 LF11201/2			LF13331/2/3 LF13201/2			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
R_{ON}	"ON" Resistance	V_A = 0, I_D = 1 mA	T_A = 25°C		150	200		150	250	Ω
					200	300		200	350	Ω
R_{ON} Match	"ON" Resistance Matching		T_A = 25°C		5	20		10	50	Ω
V_A	Analog Range			±10	±11		±10	±11		V
$I_{S(ON)}$ + $I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON," V_S = V_D = ±10V	T_A = 25°C		0.3	5		0.3	10	nA
					3	100		3	30	nA
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF," V_S = +10V, V_D = –10V	T_A = 25°C		0.4	5		0.4	10	nA
					3	100		3	30	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF," V_S = +10V, V_D = –10V	T_A = 25°C		0.1	5		0.1	10	nA
					3	100		3	30	nA
V_{INH}	Logical "1" Input Voltage			2.0			2.0			V
V_{INL}	Logical "0" Input Voltage					0.8			0.8	V
I_{INH}	Logical "1" Input Current	V_{IN} = 5V	T_A = 25°C		3.6	10		3.6	40	μA
						25			100	μA
I_{INL}	Logical "0" Input Current	V_{IN} = 0.8	T_A = 25°C			0.1			0.1	μA
						1			1	μA
t_{ON}	Delay Time "ON"	V_S = ±10V, *(Figure 3)*	T_A = 25°C		500			500		ns
t_{OFF}	Delay Time "OFF"	V_S = ±10V, *(Figure 3)*	T_A = 25°C		90			90		ns
$t_{ON} - t_{OFF}$	Break-Before-Make	V_S = ±10V, *(Figure 3)*	T_A = 25°C		80			80		ns
$C_{S(OFF)}$	Source Capacitance	Switch "OFF," V_S = ±10V	T_A = 25°C		4.0			4.0		pF
$C_{D(OFF)}$	Drain Capacitance	Switch "OFF," V_D = ±10V	T_A = 25°C		3.0			3.0		pF
$C_{S(ON)}$ + $C_{D(ON)}$	Active Source and Drain Capacitance	Switch "ON," V_S = V_D = 0V	T_A = 25°C		5.0			5.0		pF
$I_{SO(OFF)}$	"OFF" Isolation	*(Figure 4)*, (Note 3)	T_A = 25°C		–50			–50		dB
CT	Crosstalk	*(Figure 4)*, (Note 3)	T_A = 25°C		–65			–65		dB
SR	Analog Slew Rate	(Note 4)	T_A = 25°C		50			50		V/μs
I_{DIS}	Disable Current	*(Figure 5)*, (Note 5)	T_A = 25°C		0.4	1.0		0.6	1.5	mA
					0.6	1.5		0.9	2.3	mA
I_{EE}	Negative Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		3.0	5.0		4.3	7.0	mA
					4.2	7.5		6.0	10.5	mA
I_R	Reference Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		2.0	4.0		2.7	5.0	mA
					2.8	6.0		3.8	7.5	mA
I_{CC}	Positive Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		4.5	6.0		7.0	9.0	mA
					6.3	9.0		9.8	13.5	mA

Note 1: For operating at high temperature the molded DIP products must be derated based on a +100°C maximum junction temperature and a thermal resistance of +150°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at +100°C/W.

Note 2: Unless otherwise specified, V_{CC} = +15V, V_{EE} = –15V, V_R = 0V, and limits apply for –55°C $\leq T_A \leq$ +125°C for the LF11331, 2, 3 and the LF11202, 2, –25°C $\leq T_A \leq$ +85°C for the LF13331, 2, 3 and the LF13201, 2.

Note 3: These parameters are limited by the pin to pin capacitance of the package.

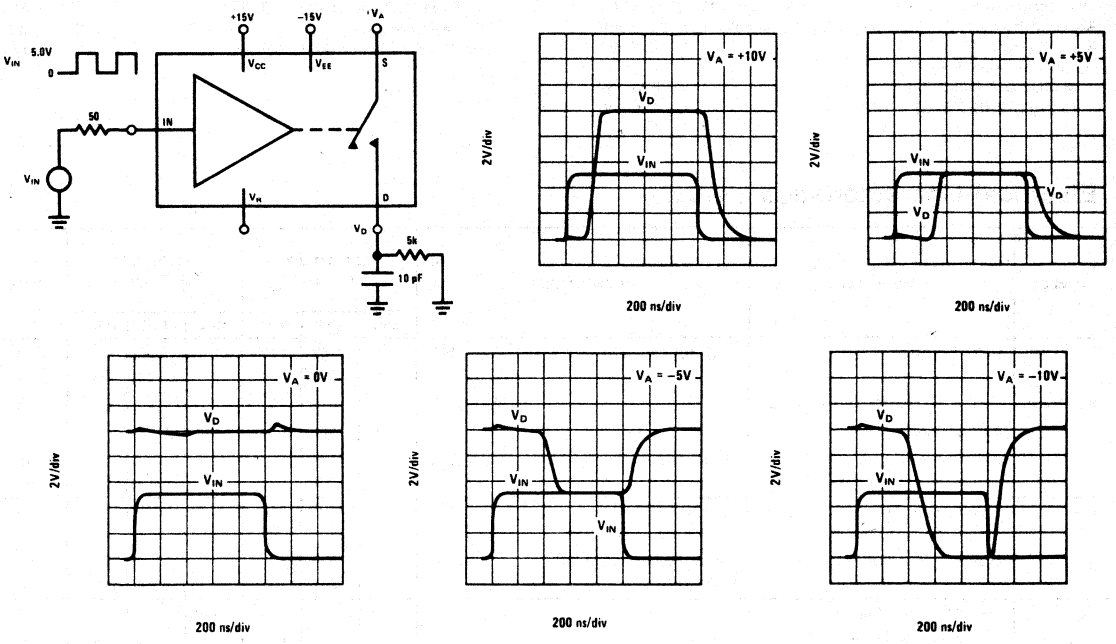
Note 4: This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.

Note 5: All switches in the device are turned "OFF" by saturating a transistor at the disable node as shown in *Figure 5.* The delay times will be approximately equal to the t_{ON} or t_{OFF} plus the delay introduced by the external transistor.

Note 6: This graph indicates the analog current at which 1% of the analog current is lost when the drain is positive with respect to the source.

Test Circuit and Typical Performance Curves

Delay Time, Rise Time, Settling Time, and Switching Transients



Additional Test Circuits

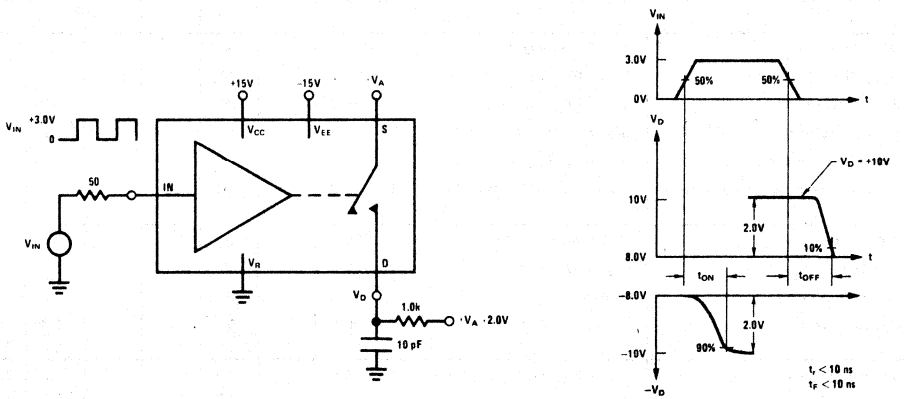


FIGURE 3. t_{ON}, t_{OFF} Test Circuit and Waveforms for a Normally Open Switch

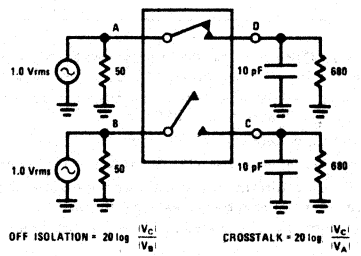
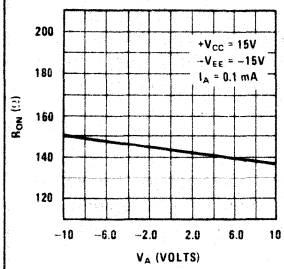


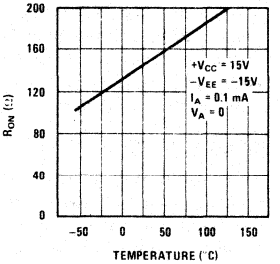
FIGURE 4. "OFF" Isolation, Crosstalk, Small Signal Response

Typical Performance Characteristics

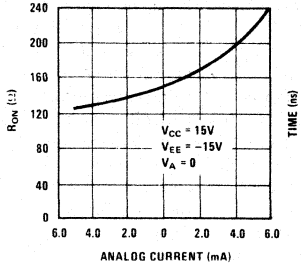
"ON" Resistance



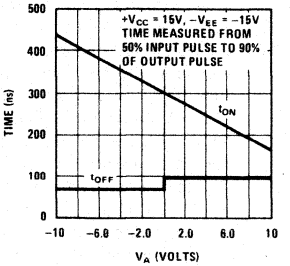
"ON" Resistance



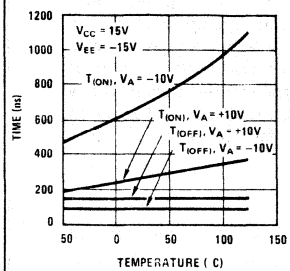
"ON" Resistance



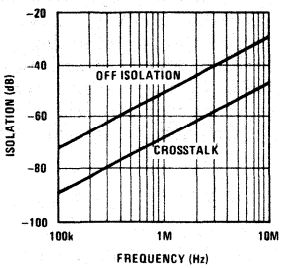
Break-Before-Make Action



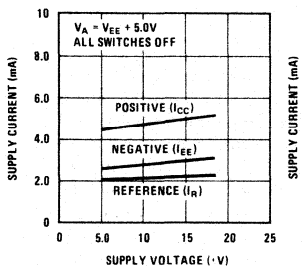
Switching Times



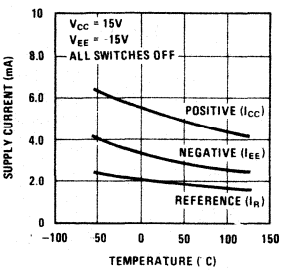
Crosstalk and "OFF" Isolation vs Frequency Using Test Circuit of *Figure 5*



Supply Current



Supply Current



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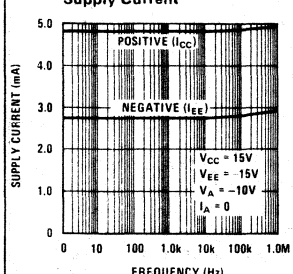
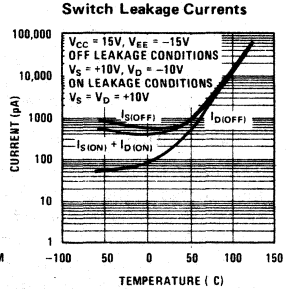
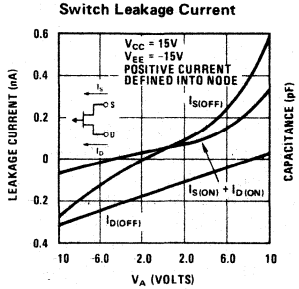


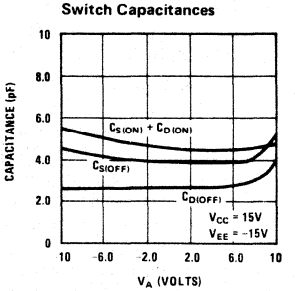
Switch Leakage Currents



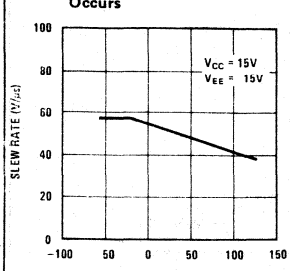
Switch Leakage Current



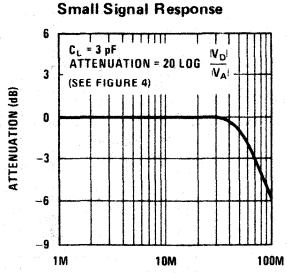
Switch Capacitances



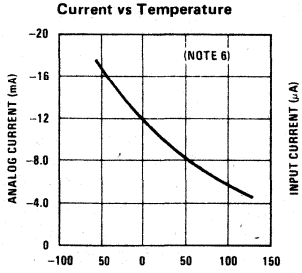
Slew Rate of Analog Voltage Above Which Signal Loading Occurs



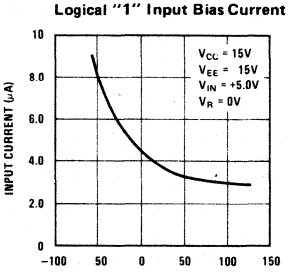
Small Signal Response



Maximum Accurate Analog Current vs Temperature



Logical "1" Input Bias Current



Application Hints

GENERAL INFORMATION

These devices are monolithic quad JFET analog switches with "ON" resistances which are essentially independent of analog voltage or analog current. The leakage currents are typically less than 1 nA at 25°C in both the "OFF" and "ON" switch states and introduce negligible errors in most applications. Each switch is controlled by minimum TTL logic levels at its input and is designed to turn "OFF" faster than it will turn "ON." This prevents two analog sources from being transiently connected together during switching. The switches were designed for applications which require break-before-make action, no analog current loss, medium speed switching times and moderate analog currents.

Because these analog switches are JFET rather than CMOS , they do not require special handling.

LOGIC INPUTS

The logic input (IN), of each switch, is referenced to two forward diode drops (1.4V at 25°C) from the reference supply (V_R) which makes it compatible with DTL, RTL, and TTL logic families. For normal operation, the logic "0" voltage can range from 0.8V to −4.0V with respect to V_R and the logic "1" voltage can range from 2.0V to 6.0V with respect to V_R, provided V_{IN} is not greater than (V_{CC} − 2.5V). If the input voltage is greater than (V_{CC} − 2.5V), the input current will increase. If the input voltage exceeds 6.0V or −4.0V with respect to V_R, a resistor in series with the input should be used to limit the input current to less than 100μA.

ANALOG VOLTAGE AND CURRENT

Analog Voltage

Each switch has a constant "ON" resistance (R_{ON}) for analog voltages from (V_{EE} + 5V) to (V_{CC} − 5V). For analog voltages greater than (V_{CC} − 5V), the switch will remain ON independent of the logic input voltage. For analog voltages less than (V_{EE} + 5V), the ON resistance of the switch will increase. Although the switch will not operate normally when the analog voltage is out of the previously mentioned range, the source voltage can go to either (V_{EE} + 36V) or (V_{CC} + 6V), whichever is more positive, and can go as negative as V_{EE} without destruction. The drain (D) voltage can also go to either (V_{EE} + 36V) or (V_{CC} + 6V), whichever is more positive, and can go as negative as (V_{CC} − 36V) without destruction.

Analog Current

With the source (S) positive with respect to the drain (D), the R_{ON} is constant for low analog currents, but will increase at higher currents (>5 mA) when the FET enters the saturation region. However, if the drain is positive with respect to the source and a small analog current loss at high analog currents (Note 6) is tolerable, a low R_{ON} can be maintained for analog currents greater than 5 mA at 25°C.

LEAKAGE CURRENTS

The drain and source leakage currents, in both the ON and the OFF states of each switch, are typically less than 1 nA at 25°C and less than 100 nA at 125°C. As shown in the typical curves, these leakage currents are dependent on power supply voltages, analog voltage, analog current and the source to drain voltage.

DELAY TIMES

The delay time OFF (t_{OFF}) is essentially independent of both the analog voltage and temperature. The delay time ON (t_{ON}) will decrease as either ($V_{CC} - V_A$) decreases or the temperature decreases.

POWER SUPPLIES

The voltage between the positive supply (V_{CC}) and either the negative supply (V_{EE}) or the reference supply (V_R) can be as much as 36V. To accommodate variations in input logic reference voltages, V_R can range from V_{EE} to (V_{CC} − 4.5V). Care should be taken to ensure that the power supply leads for the device never become reversed in polarity or that the device is never inadvertantly installed backwards in a test socket. If one of these conditions occurs, the supplies would zener an interal diode to an unlimited current; and result in a destroyed device.

SWITCHING TRANSIENTS

When a switch is turned OFF or ON, transients will appear at the load due to the internal transient voltage at the gate of the switch JFET being coupled to the drain and source by the junction capacitances of the JFET. The magnitude of these transients is dependent on the load. A lower value R_L produces a lower transient voltage. A negative transient occurs during the delay time ON, while a positive transient occurs during the delay time OFF. These transients are relatively small when compared to faster switch families.

DISABLE NODE

This node can be used, as shown in *Figure 5,* to turn all the switches in the unit off independent of logic inputs. Normally, the node floats freely at an internal diode drop (≈ 0.7V) above V_R. When the external transistor in *Figure 5* is saturated, the node is pulled very close to V_R and the unit is disabled. Typically, the current from the node will be less than 1 mA. This feature is not available on the LF11201 or LF11202 series.

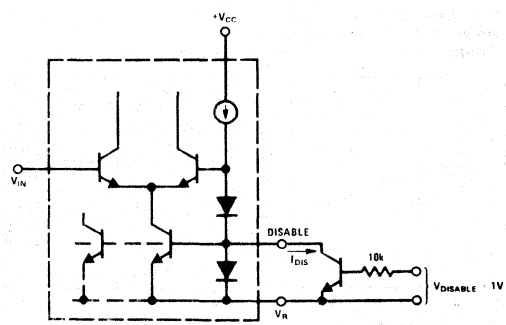
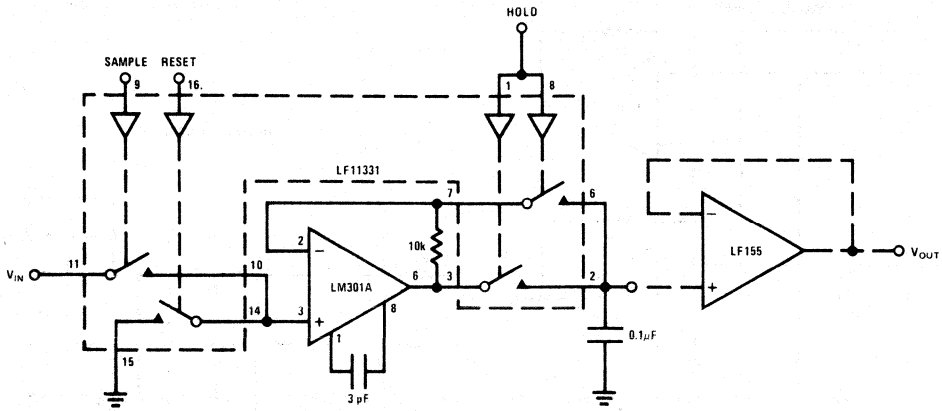


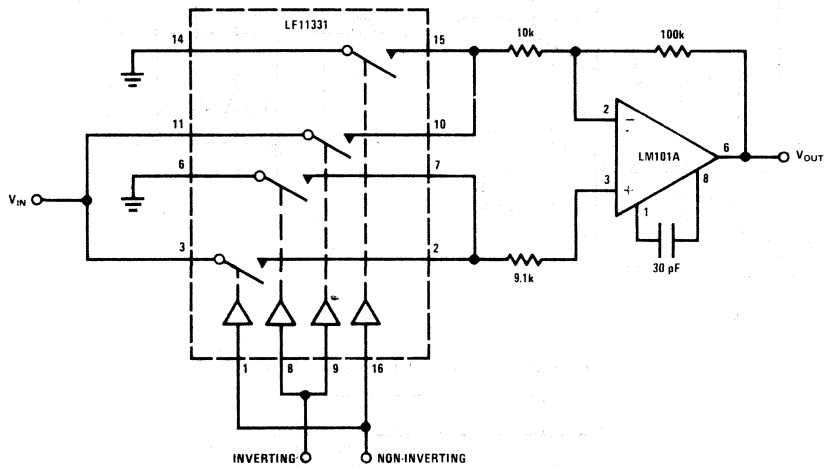
FIGURE 5. Disable Function

Typical Applications

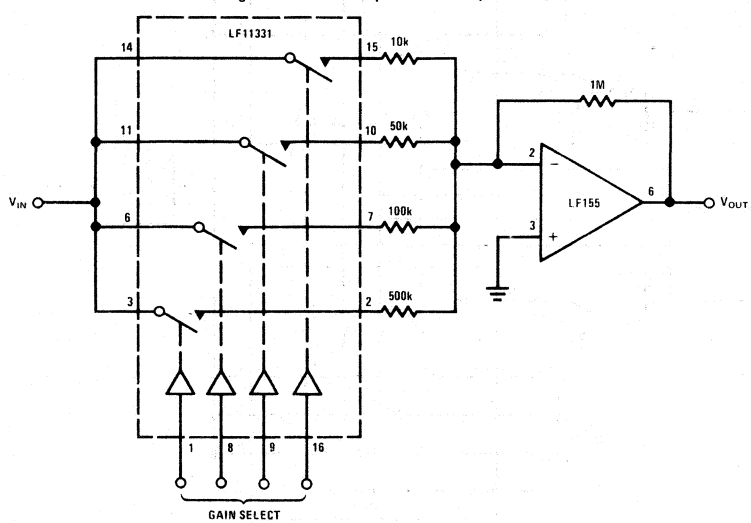
Sample and Hold with Reset



Programmable Inverting Non-Inverting Operational Amplifier

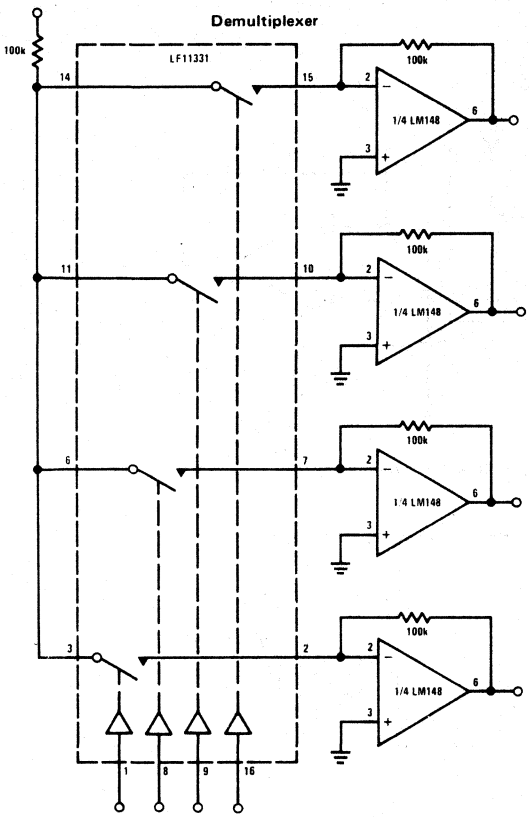


Programmable Gain Operational Amplifier

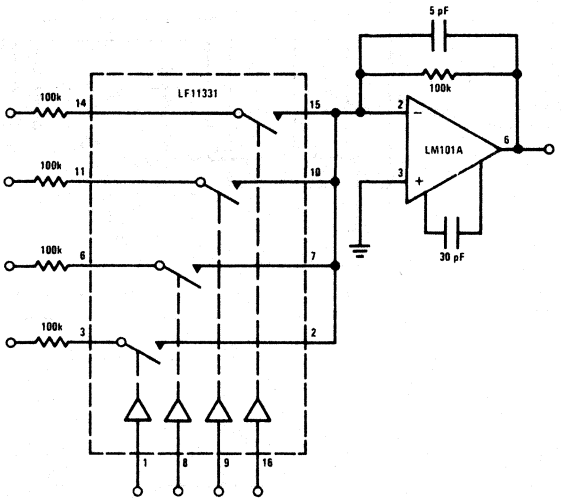


Typical Applications (Continued)

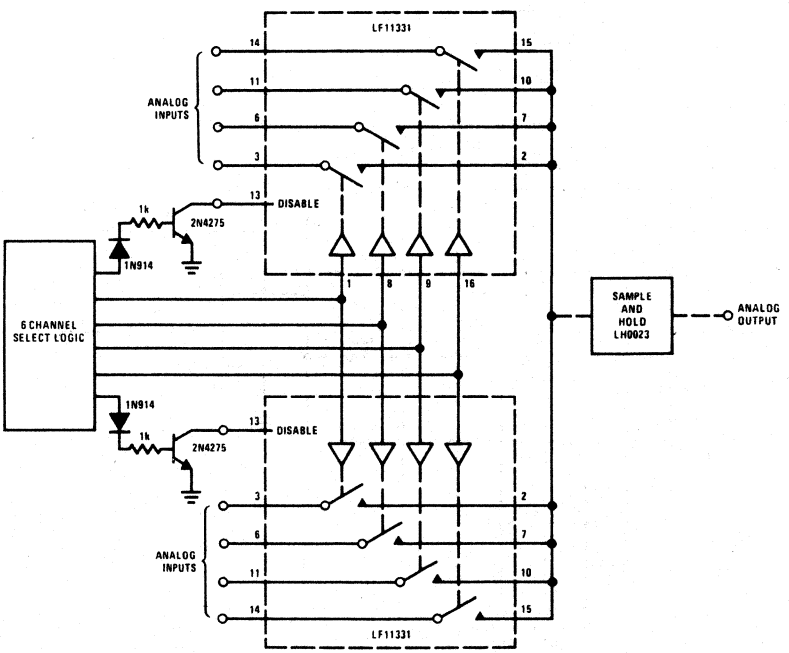
Demultiplexer



Multiplexer/Mixer

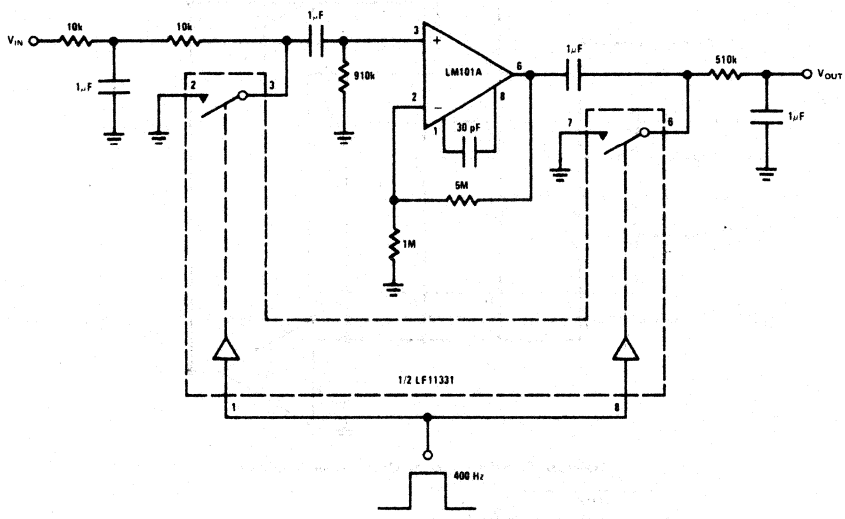


8-Channel Analog Commutator with 6-Channel Select Logic

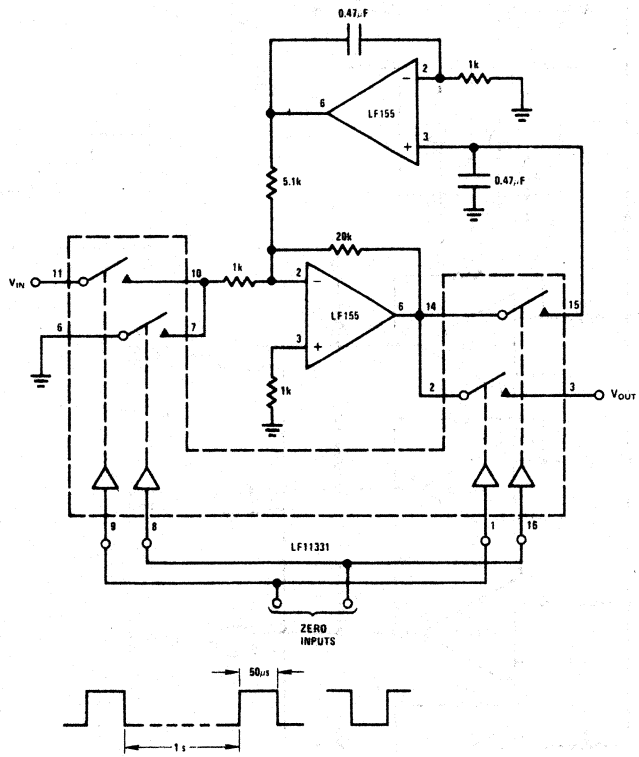


Typical Applications (Continued)

Chopper Channel Amplifier

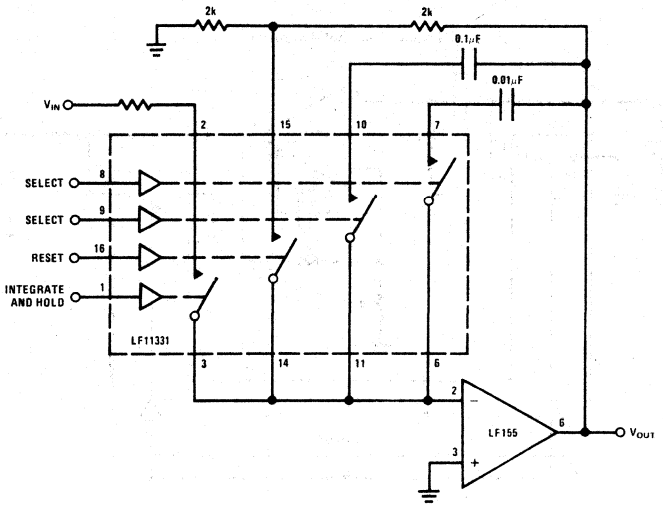


Self-Zeroing Operational Amplifier

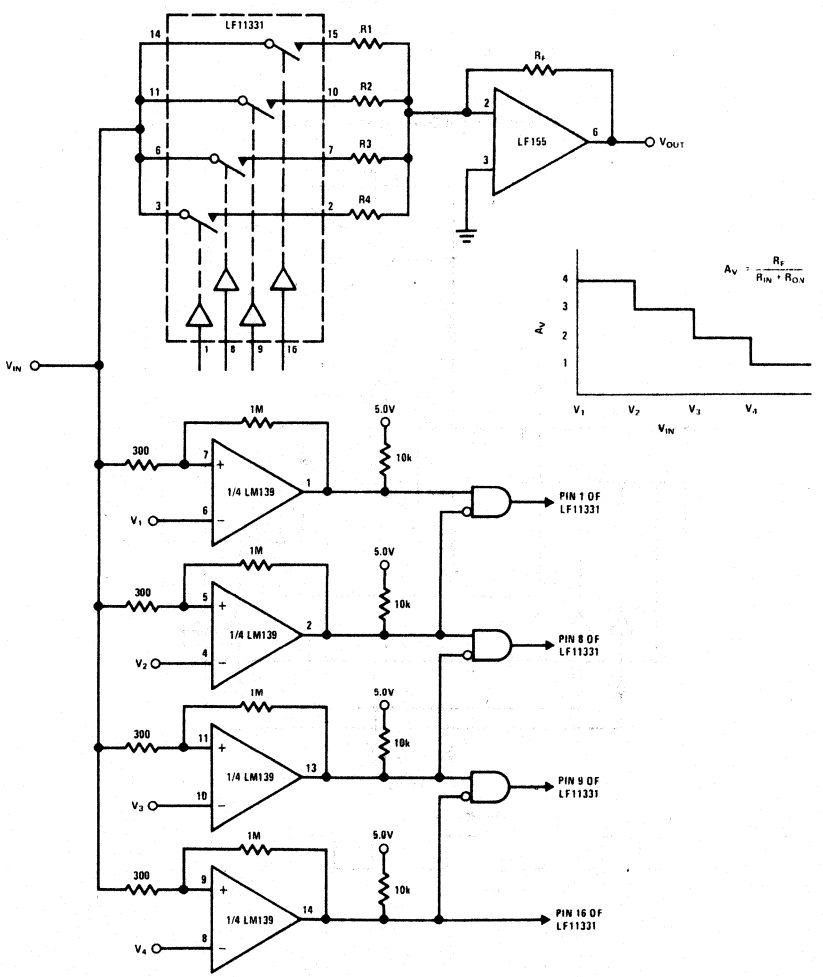


Typical Applications (Continued)

Programmable Integrator with Reset and Hold

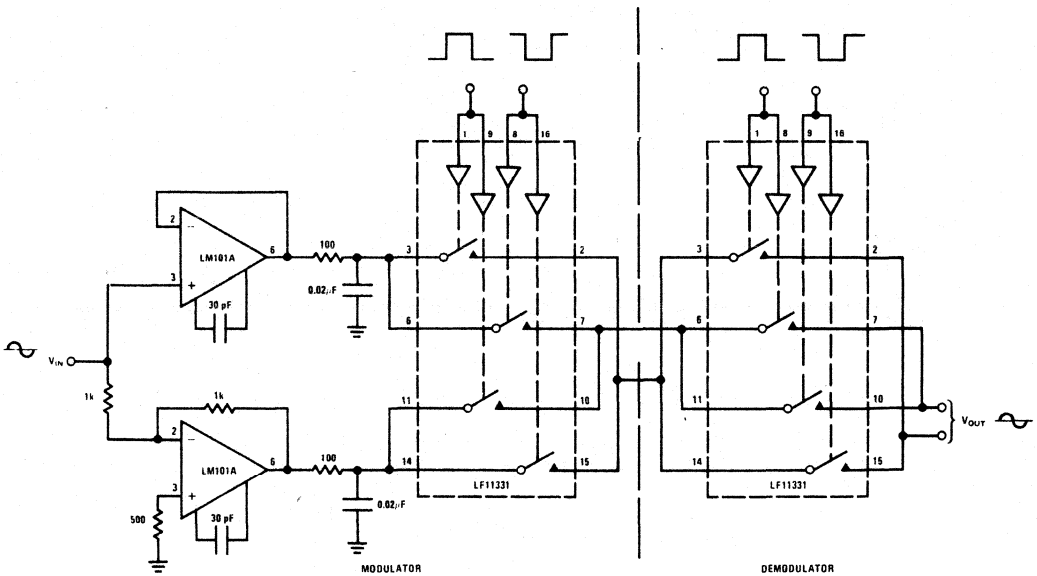


Staircase Transfer Function Operational Amplifier



Typical Applications (Continued)

DSB Modulator-Demodulator



Section 5

Analog-to-Digital Converters

5

Analog-to-Digital Converters

Section Contents

ADB1200 (MM5863) 12-Bit Binary A/D Building Block

General Description

The ADB1200 is the digital controller for the LF13300D* analog building block. Together they form an integrating 12-bit A/D converter. The ADB1200 provides all the necessary control functions, plus features like auto zeroing, polarity and overrange indication, as well as continuous conversion. The 12-bit plus sign parallel and serial outputs are TRI-STATE® TTL level compatible. The device also includes output latches to simplify data bus interfacing.

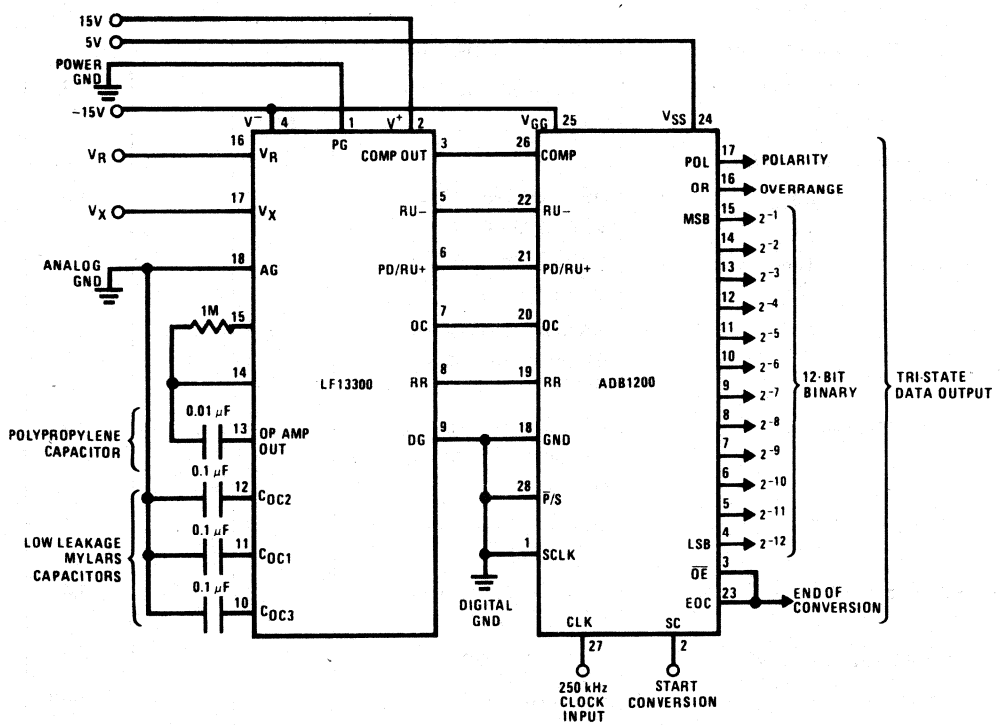
*See LF13300D data sheet for more information

Features

- 12-bit binary output
- Parallel or serial output
- TRI-STATE output
- Polarity indication
- Overrange indication
- Continuous conversion capability
- 100% overrange capability
- 5V, −15V power requirements
- TTL compatible
- Clock frequency to 1 MHz

Circuit Diagram/Typical Applications

12-Bit A/D Converter



Absolute Maximum Ratings

Supply Voltage (V_{SS})	5.25V
Supply Voltage (V_{GG})	−16.5V
Voltage at Any Input	5.25V
Operating Temperature	0°C to +70°C
Storage Temperature	−40°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

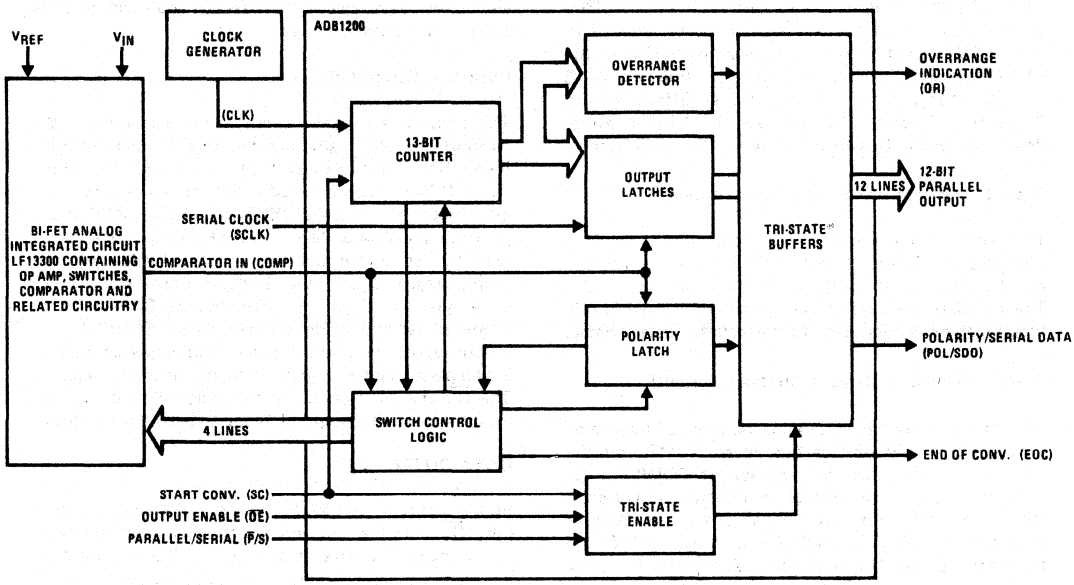
Electrical Characteristics

V_{SS} = 5V, V_{GG} = −15V, 0°C to +70°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})		4.75	5.00	5.25	V
Power Supply Voltage (V_{GG})		−13.5	−15.00	−16.5	V
Power Supply Current (I_{SS})				28	mA
Power Supply Current (I_{GG})				34	mA
Logic "1" Input Voltage		3.4			V
Logic "0" Input Voltage				0.8	V
Logic "1" Output Voltage	V_{SS} = 4.75V, I_{OH} = 100 μA	3.8			V
Logic "0" Output Voltage	V_{SS} = 5.25V, I_{OL} = −1.6 mA			0.4	V
Width of EOC	Auto Cycle	5/f			sec
Prop. Delay COMP to EOC		4/f		5/f+1 μs	sec
Output Enable Time	$\overline{OE}$ to Any Data Output, SC = 1, $\overline{P}$/S = 0			1.0	μs
Output Disable Time	$\overline{OE}$ to Any Data Output, SC = 1, $\overline{P}$/S = 0			2.4	μs
Output Enable Time	$\overline{P}$/S to Any Data Output Except Polarity, SC = 1, $\overline{OE}$ = 0			0.9	μs
Output Disable Time	$\overline{P}$/S to Any Data Output Except Polarity, SC = 1, $\overline{OE}$ = 0			2.2	μs
Output Enable Time	SC to Any Data Output, $\overline{OE}$ = 0, $\overline{P}$/S = 0			1.0	μs
Output Disable Time	SC to Any Data Output, $\overline{OE}$ = 0, $\overline{P}$/S = 0			2.4	μs
Prop. Delay Serial Clock	SCLK to POL/SDO			0.6	μs
Conversion Time	Full Scale			8966/f	sec
Conversion Time	100% Overrange			13062/f	sec
Maximum Clock Frequency	CLK, Pin 27	500	1000		kHz
Maximum Serial Clock Frequency	SCLK, Pin 1	500	1000		kHz

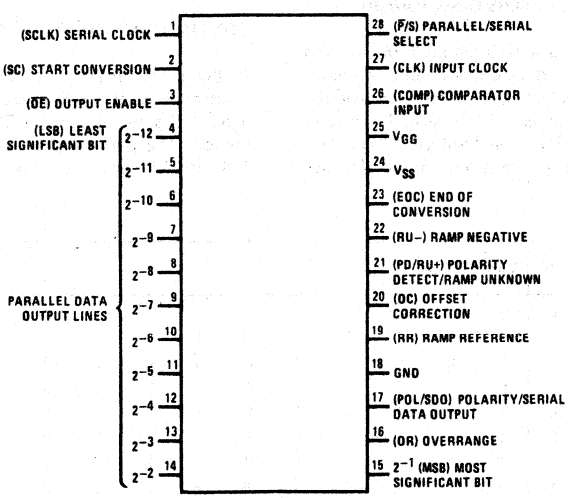
Block Diagram

Digital Control Integrated Circuit



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number ADB1200PCN
See NS Package N28A

Functional Description

OPERATION

The ADB1200 is designed for use with the LF13300 analog front end. Four control signals are supplied to the LF13300 and 1 control signal is required from the LF13300. The conversion cycle is composed of 5 distinct phases. They are: Phase I – Offset Correct; Phase II – Polarity Detect; Phase III – Initialization; Phase IV – Ramp Unknown; Phase V – Ramp Reference.

Phase I – Offset Correct (256 Clock Periods)

This phase is initiated by taking the Start Conversion (SC) and the Output Enable ($\overline{OE}$) lines to a logic "1". At this time, Offset Correct (OC) will be a logic "1". The LF13300 requires this phase to correct any intrinsic offset voltage errors prior to the polarity detect phase.

Phase II – Polarity Detect (256 Clock Periods)

This phase is used to determine polarity of the analog input. At the midpoint of this phase, COMP from the LF13300 is examined for polarity. If COMP = logic "1", then the input voltage is positive. If COMP = logic "0", then the input is negative. The Polarity Detect signal (PD/RU+) will be at a logic "1" during this entire phase. The above operation is also necessary to determine which integrator input (positive or negative) of the LF13300 should be used for proper A/D conversion (see LF13300 data sheet).

Phase III – Initialization (256 Clock Periods)

This phase is identical to Phase I and is used by the LF13300 to eliminate any offsets induced as a result of the Polarity Detect Phase. Offset Correct (OC) will be at a logic "1".

Phase IV – Ramp Unknown (4096 Clock Periods)

The unknown input voltage is integrated for a fixed time, 4096 clock periods, during this phase. The result of the Phase II Polarity Detect Cycle determines whether PD/RU+ or RU– will be at logic "1". If Phase II indicates a positive input, the PD/RU+ signal will be a logic "1". If phase II indicates a negative input, Ramp Negative (RU–) will be a logic "1". These 2 signals will never be at logic "1" simultaneously.

Phase V – Ramp Reference

This phase is a variable length phase depending on the magnitude of the analog input voltage. During this time, Ramp Reference (RR) will be in the logic "1" state. When COMP goes to a logic "0" state, or when the internal counter reaches 100% of full scale (8192 clock periods), the Ramp Reference (RR) signal goes to the logic "0" state, the counter output is loaded into the output register, and the End of Conversion (EOC) signal goes to a logic "1". The Polarity Bit will reflect whatever value was determined during Phase II. The output register will hold the data until a new conversion is completed and new data is loaded into the register. The $\overline{OE}$ line must be low in the logic "0" state and SC must be high in the logic "1" state to enable the outputs.

DATA OUTPUTS

Both serial and parallel outputs are available. In either case, $\overline{OE}$ must be low and SC must be high to enable the outputs. For parallel output, the $\overline{P}$/S line must be low in the logic "0" state. For serial outputs, the $\overline{P}$/S line must be high. In the serial mode, the data is shifted out of the Polarity/Serial Output (POL/SDO) line and all other data outputs are in the high impedance state. Each Serial Clock (SCLK) will right shift the output register one bit. Thus, 13 clock pulses are required to fully shift out the data. The data will be shifted out in the following order: Polarity, Overrange, MSB, 2SB, 3SB, . . . , LSB. If $\overline{OE}$ and $\overline{P}$/S are in the logic "0" state and SC in the logic "1" state, all outputs will momentarily go to the logic "1" state for 1 clock period immediately preceding EOC.

CONTINUOUS CONVERT MODE

In this mode, the End of Conversion (EOC) output is connected to the $\overline{OE}$ input. As long as SC is in the logic "1" state, then each EOC will initiate a new conversion. The data outputs will be disabled for the first 5 clock cycles after EOC goes high.

Truth Table

INPUT	SC	OE	P/S	LSB											MSB	OVER-RANGE	POLARITY
100% Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1
Zero	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Zero	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
–Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
–100% Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Any	1	1	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Any	1	0	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Serial Output
Any	0	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

1 = High
0 = Low
Z = High Impedance
X = Don't Care

Timing Diagrams

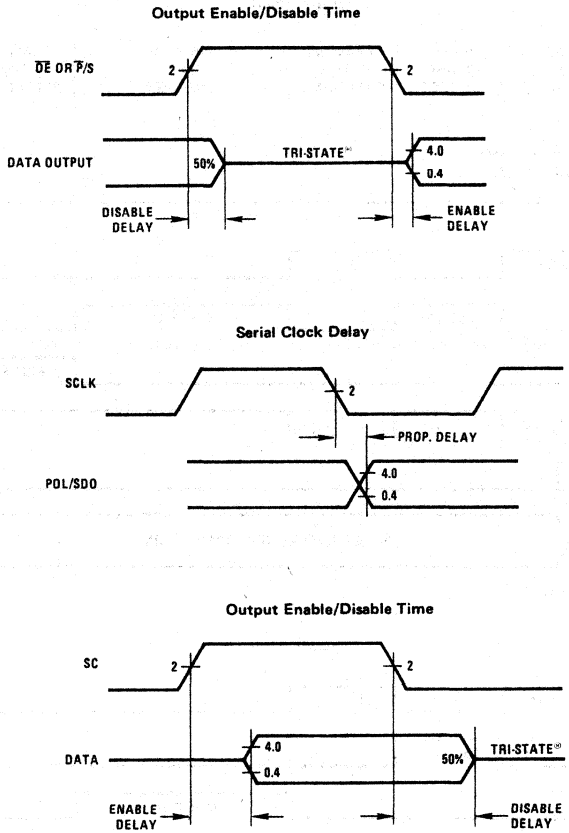


FIGURE 1. Parallel Data

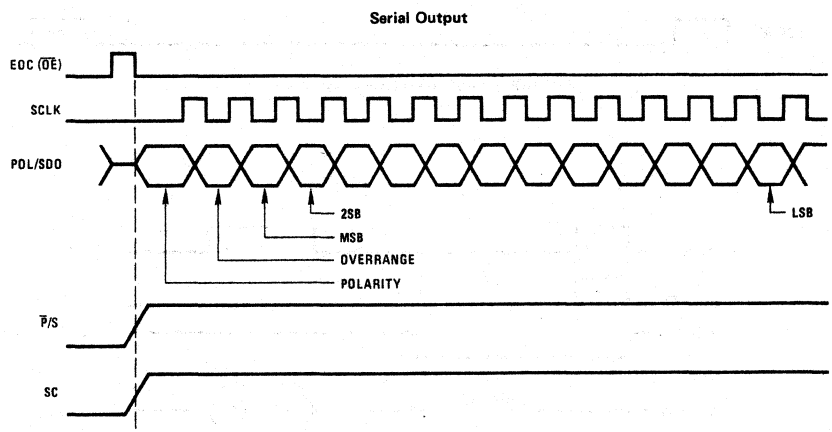


FIGURE 2. Serial Data

Timing Diagrams (Continued)

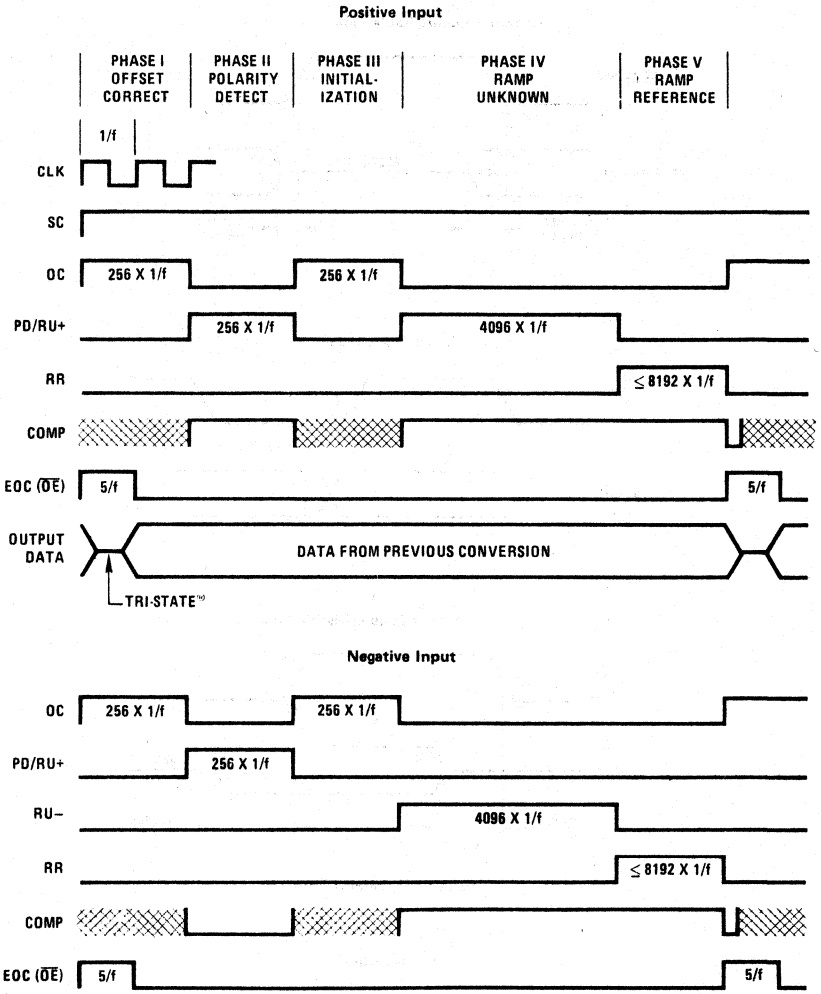


FIGURE 3. Continuous Conversion Mode

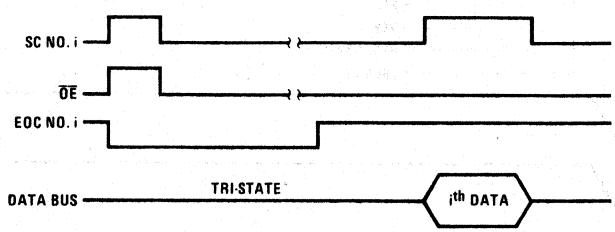
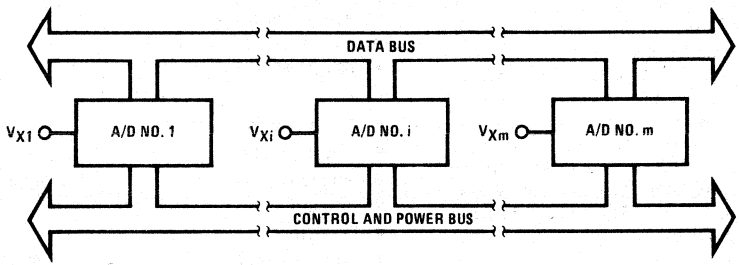


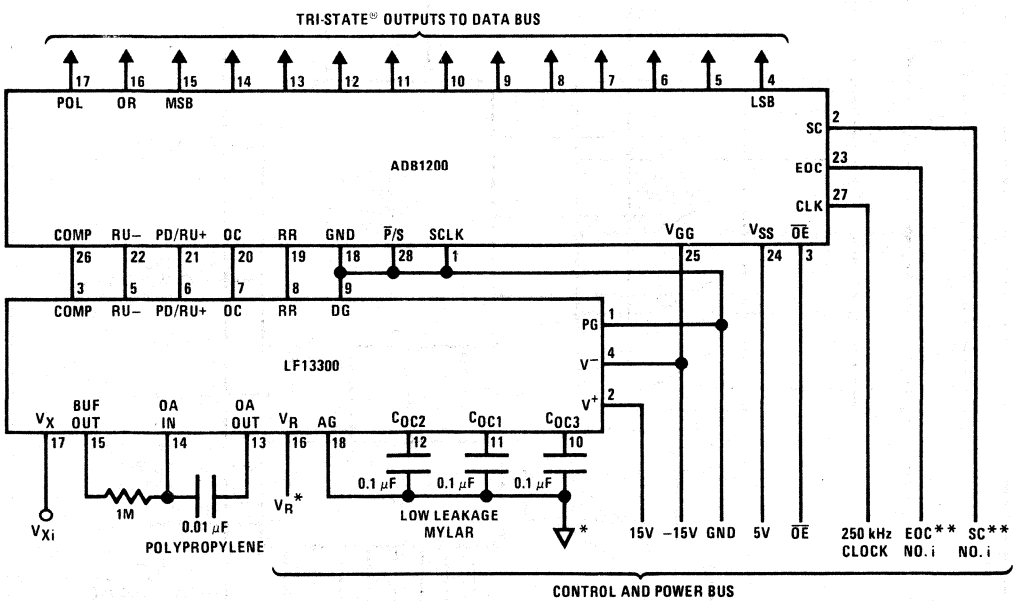
FIGURE 4. i^{th} A/D Converter Data Retrieval Sequence

Typical Applications (Continued)

Multi A/D Converter System on Common Bus



i^{th} A/D Converter



*May be common or separate. Care should be taken to avoid ground currents
**Direct or multiplexed access to the processor
Note. This application is related to *Figure 4* of timing diagrams

National Semiconductor

Analog-to-Digital Converters

ADC0800 8-Bit A/D Converter

General Description

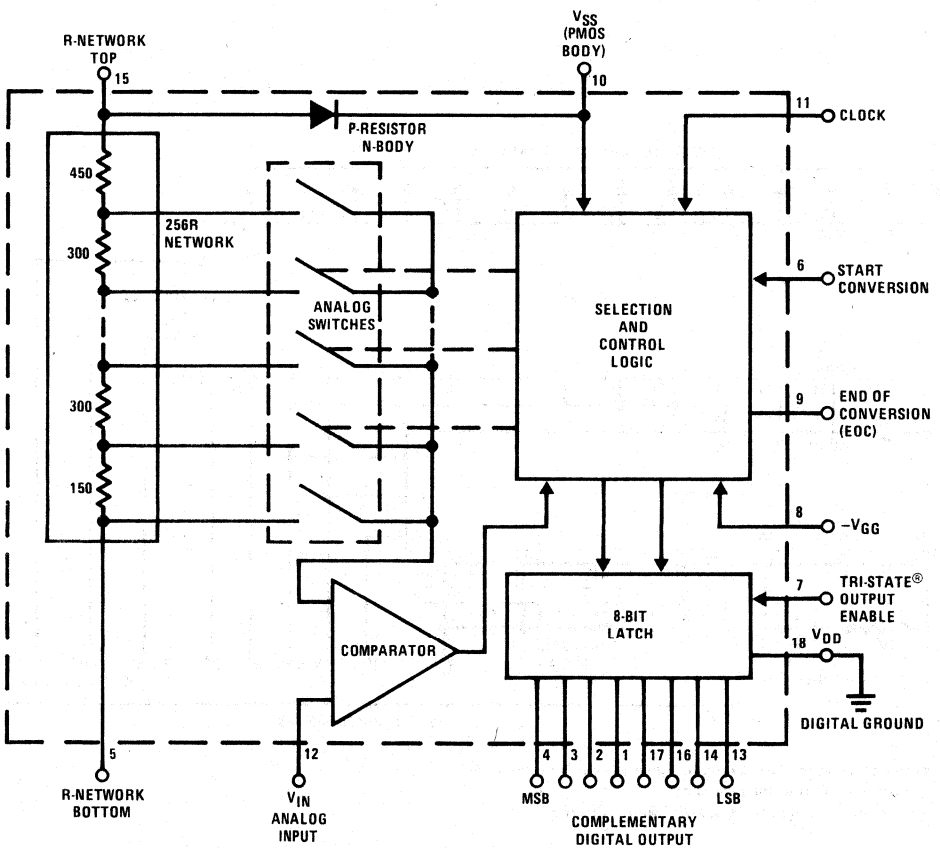
The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCD is specified over 0°C to 70°C.

Features

- Low cost
- ±5V, 10V input ranges
- No missing codes
- Ratiometric conversion
- TRI-STATE outputs
- Fast — T_C = 50 μs
- Contains output latches
- TTL compatible
- Supply voltages — 5 V_{DC} and −12 V_{DC}
- Resolution — 8 bits
- Linearity — ±1 LSB
- Conversion speed — 40 clock periods
- Clock range — 50 to 800 kHz

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD})	V_{SS}–22V
Supply Voltage (V_{GG})	V_{SS}–22V
Voltage at Any Input	V_{SS} + 0.3V to V_{SS}–22V
Storage Temperature	150°C
Operating Temperature	
ADC0800PD	−55°C to +125°C
ADC0800PCD	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

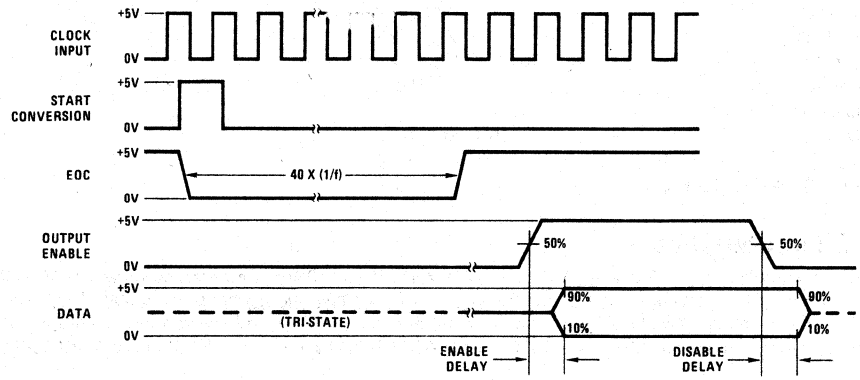
Electrical Characteristics

These specifications apply for V_{SS} = 5.0 V_{DC}, V_{GG} = −12.0 V_{DC}, V_{DD} = 0 V_{DC}, a reference voltage of 10.000 V_{DC} across the on-chip R-network ($V_{R\text{-}NETWORK\ TOP}$ = 5.000 V_{DC} and $V_{R\text{-}NETWORK\ BOTTOM}$ = −5.000 V_{DC}), and a clock frequency of 800 kHz. For all tests, a 475Ω resistor is used from pin 5 to ground. Unless otherwise noted, these specifications apply over an ambient temperature range of −55°C to +125°C for the ADC0800PD and 0°C to +70°C for the ADC0800PCD.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Non-Linearity	T_A = 25°C, (Note 1)			±1	LSB
	Over Temperature, (Note 1)			±2	LSB
Differential Non-Linearity				±1/2	LSB
Zero Error				±2	LSB
Zero Error Temperature Coefficient	(Note 2)			0.01	%/°C
Full-Scale Error				±2	LSB
Full-Scale Error Temperature Coefficient	(Note 2)			0.01	%/°C
Input Leakage				1	μA
Logical "1" Input Voltage	All Inputs	V_{SS}–1.0		V_{SS}	V
Logical "0" Input Voltage	All Inputs	V_{GG}		V_{SS}–4.2	V
Logical Input Leakage	T_A = 25°C, All Inputs, V_{IL} = V_{SS} − 10V			1	μA
Logical "1" Output Voltage	All Outputs, I_{OH} = 100 μA	2.4			V
Logical "0" Output Voltage	All Outputs, I_{OL} = 1.6 mA			0.4	V
Disabled Output Leakage	T_A = 25°C, All Outputs, V_{OL} = V_{SS} @ 10V			2	μA
Clock Frequency	0°C ≤ T_A ≤ +70°C	50		800	kHz
	−55°C ≤ T_A ≤ +125°C	100		500	kHz
Clock Pulse Duty Cycle		40		60	%
TRI-STATE Enable/Disable Time				1	μs
Start Conversion Pulse	(Note 3)	1		3 1/2	Clock Periods
Power Supply Current	T_A = 25°C			15	mA

Note 1: Non-linearity specifications are based on best straight line.
Note 2: Guaranteed by design only.
Note 3: Start conversion pulse duration greater than 3 1/2 clock periods will cause conversion errors.

Timing Diagram



Data is complementary binary (full scale is all "0's" output).

Application Hints

OPERATION

The ADC0800 contains a network with 256-300Ω resistors in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference (10.00V) is applied across this network of 256 resistors. An analog input (V_{IN}) is first compared to the center point of the ladder via the appropriate switch. If V_{IN} is larger than $V_{REF}/2$, the internal logic changes the switch points and now compares V_{IN} and 3/4 V_{REF}. This process, known as successive approximation, continues until the best match of V_{IN} and V_{REF}/N is made. N now defines a specific tap on the resistor network. When the conversion is complete, the logic loads a binary word corresponding to this tap into the output latch and an end of conversion (EOC) logic level appears. The output latches hold this data valid until a new conversion is completed and new data is loaded into the latches. The data transfer occurs in about 200 ns so that valid data is present virtually all the time. Conversion requires 40 clock periods. The device may be operated in the free running mode by connecting the Start Conversion line to the End of Conversion line. However, to ensure start-up under all possible conditions, an external Start Conversion pulse is required during power up conditions.

REFERENCE

The reference applied across the 256 resistor network determines the analog input range. V_{REF} = 10.00V with the top of the R-network connected to 5V and the bottom connected to −5V gives a ±5V range. The reference can be level shifted between V_{SS} and V_{GG}. However, the voltage, which is applied to the top of the R-network (pin 15), must not exceed V_{SS} to prevent forward biasing the on-chip parasitic silicon diode which exists between the P-diffused resistors (pin 15) and the N-type body (pin 10, V_{SS}). Use of a standard logic power supply for V_{SS} can cause problems, both due to initial voltage tolerance and changes over temperature. A solution is to power the V_{SS} line (15 mA max drain) from the output of the op amp which is used to bias the top of the R-network (pin 15). The analog input voltage and the voltage which is applied to the bottom of the R-network (pin 5) must be at least 7V above the $-V_{DD}$ supply voltage to insure adequate voltage drive to the analog switches.

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy, it is desirable to operate with at least a 10V reference. For TTL logic levels, this requires 5V and −5V for the R-network. CMOS can operate at the 10 V_{DC} V_{SS} level and a single 10 V_{DC} reference can be used. All digital voltage levels for both inputs and outputs will be from ground to V_{SS}.

ANALOG INPUT AND SOURCE RESISTANCE CONSIDERATIONS

The lead to the analog input (pin 12) should be kept as short as possible. Both noise and digital clock coupling to this input can cause conversion errors. To minimize any input errors, the following source resistance considerations should be noted:

For $R_S \leq 5k$	No analog input bypass capacitor required, although a 0.1 μF input bypass capacitor will prevent pick-up due to unavoidable series lead inductance.
For $5k < R_S \leq 20k$	A 0.1 μF capacitor from the input (pin 12) to ground should be used.
For $R_S > 20k$	Input buffering is necessary.

If the overall converter system requires lowpass filtering of the analog input signal, use a 20 kΩ or less series resistor for a passive RC section or add an op amp RC active lowpass filter (with its inherent low output resistance) to insure accurate conversions.

CLOCK COUPLING

The clock lead should be kept away from the analog input line to reduce coupling.

LOGIC INPUTS

The logical "1" input voltage swing for the Clock, Start Conversion and Output Enable should be (V_{SS} − 1.0V).

Application Hints (Continued)

CMOS will satisfy this requirement but a pull-up resistor should be used for TTL logic inputs.

RE-START AND DATA VALID AFTER EOC

The EOC line (pin 9) will be in the low state for a maximum of 40 clock periods to indicate "busy". A START pulse which occurs while the A/D is BUSY will reset the SAR and start a new conversion with the EOC signal remaining in the low state until the end of this new conversion. When the conversion is complete, the EOC line will go to the high voltage state. An additional 4 clock periods must be allowed to elapse after EOC goes high, before a new conversion cycle is requested. Start Conversion pulses which occur during this last 4 clock period interval may be ignored (see *Figures 1 and 2* for high speed operation). This is only a problem for high conversion rates and keeping the number of conversions per second less than (1/44) x f_{CLOCK} automatically guarantees proper operation. For example, for an 800 kHz clock, 18,000 conversions per second are allowed. The transfer of the new digital data to the output is initiated when EOC goes to the high voltage state.

POWER SUPPLIES

Standard supplies are V_{SS} = 5V, V_{GG} = −12V and V_{DD} = 0V. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to $V_{SS} - V_{GG}$. V_{DD} has no effect on accuracy. Noise spikes on the V_{SS} and V_{GG} supplies can cause improper conversion; therefore, filtering each supply with a 4.7 μF tantalum capacitor is recommended.

CONTINUOUS CONVERSIONS AND LOGIC CONTROL

Simply tying the EOC output to the Start Conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 clock periods after EOC goes high. Adding a D flip-flop between EOC (D input) to Start Conversion (Q output) will prevent the oscillation and will allow a stop/continuous control via the "clear" input.

To prevent missing a start pulse which may occur after EOC goes high and prior to the required 4 clock period time interval, the circuit of *Figure 1* can be used. The RS latch can be set at any time and the 4-stage shift register delays the application of the start pulse to the A/D by 4 clock periods. The RS latch is reset 1 clock period after the A/D EOC signal goes to the low voltage state. This circuit also provides a Start Conversion pulse to the A/D which is 1 clock period wide.

A second control logic application circuit is shown in *Figure 2*. This allows an asynchronous start pulse of arbitrary length less than T_C, continuously converts for a fixed high level and provides a single clock period start pulse to the A/D. The binary counter is loaded with a count of 11 when the start pulse to the A/D appears. Counting is inhibited until the EOC signal from the A/D goes high. A carry pulse is then generated 4 clock periods after EOC goes high and is used to reset the input RS latch. This carry pulse can be used to indicate that the conversion is complete, the data has transferred to the output buffers and the system is ready for a new conversion cycle.

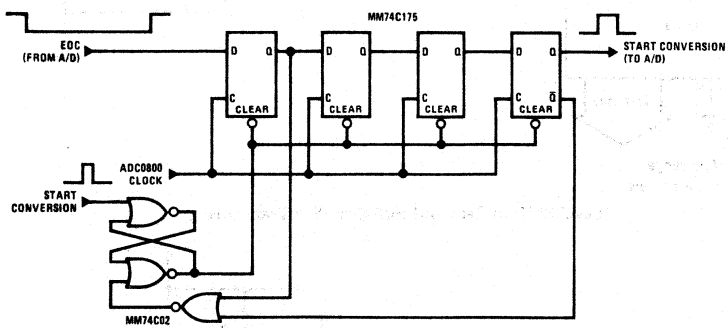


FIGURE 1. Delaying an Asynchronous Start Pulse

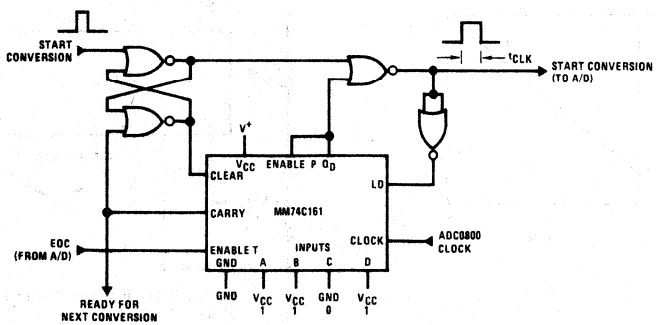


FIGURE 2. A/D Control Logic

Application Hints (Continued)

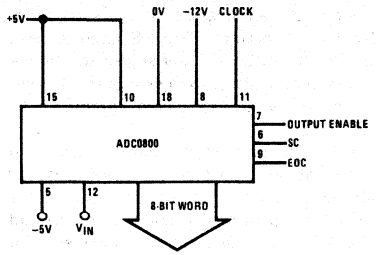
ZERO AND FULL-SCALE ADJUSTMENT

Zero Adjustment: This is the offset voltage required at the bottom of the R-network (pin 5) to make the 11111111 to 11111110 transition when the input voltage is 1/2 LSB (20 mV for a 10.24V scale). In most cases, this can be accomplished by having a 1 kΩ pot on pin 5. A resistor of 475Ω can be used as a non-adjustable best approximation from pin 5 to ground.

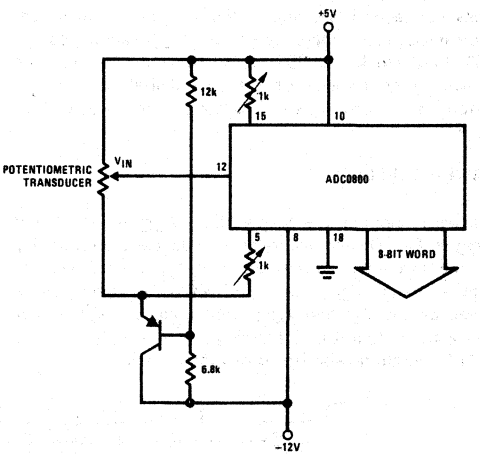
Full-Scale Adjustment: This is the offset voltage required at the top of the R-network (pin 15) to make the 00000001 to 00000000 transition when the input voltage is 1 1/2 LSB from full-scale (60 mV less than full-scale for a 10.24V scale). This voltage is guaranteed to be within 2 LSB for the ADC0800. In most cases, this can be accomplished by having a 1 kΩ pot on pin 15.

Typical Applications

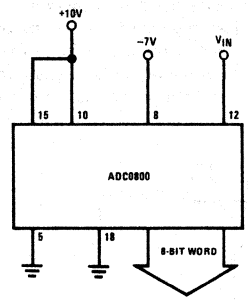
General Connection



Ratiometric Input Signal with Tracking Reference



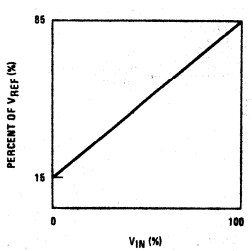
Hi-Voltage CMOS Output Levels

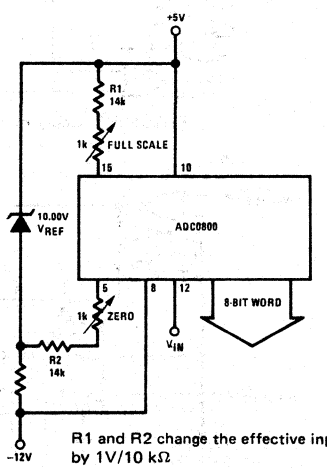


0V to 10V V_{IN} range
0V to 10V output levels

Level Shifted Zero and Full-Scale for Transducers

Level Shifted Input Signal Range

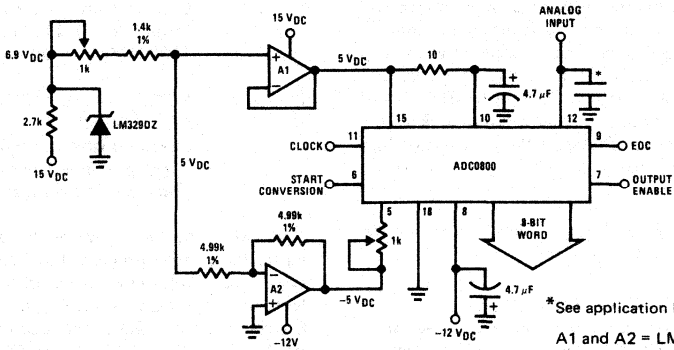




R1 and R2 change the effective input range by 1V/10 kΩ

Typical Applications (Continued)

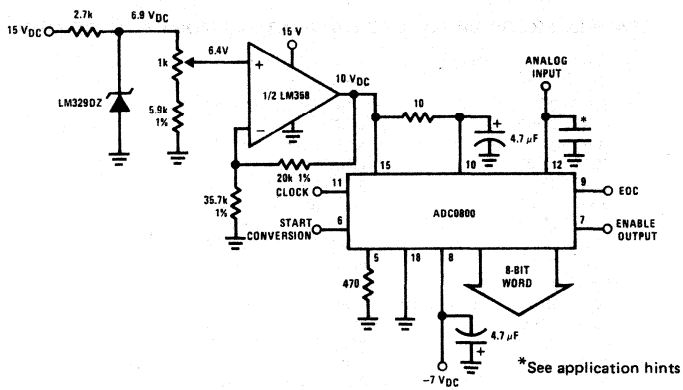
V_{REF} = 10 V_{DC} With TTL Logic Levels



*See application hints

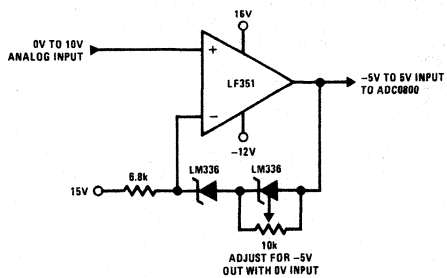
A1 and A2 = LM358N dual op amp

V_{REF} = 10 V_{DC} With 10V CMOS Logic Levels



*See application hints

Input Level Shifting



- Permits TTL compatible outputs with 0V to 10V input range (0V to −10V input range achieved by reversing polarity of zener diodes and returning the 6.8k resistor to V^-).

MICROPROCESSOR INTERFACE

Figure 3 and the following sample program are included to illustrate both hardware and software requirements to allow output data from the ADC0800 to be loaded into the memory of a microprocessor system. For this example, National's INS8060, SC/MP II, microprocessor has been used.

The sample program, as shown, will start the converter, load the converter's output data into the accumulator, keep track of the number of data bytes entered, complement the data and store this data into sequential memory locations. After 256 bytes have been entered, the control jumps to the user's program where proces-

Typical Applications (Continued)

sing of the data entered will be implemented. A more practical program whereby each data byte entered will be processed before another entry is made can easily be done by jumping back to the user's program at the end of the interrupt routine (where the data is loaded into the accumulator and stored in memory). The end of the user's program should provide a jump back to the INITIALIZE statement to start a new conversion and generate a new data entry.

The following arbitrarily chosen addresses and pointer assignments are used in this example:

Pointer 1 — WORD COUNT (ADDR:0100)
Also used to point to the A/D converter at address 0500 for this example when data is to be entered.

Pointer 2 — ENTERED DATA (ADDR's: 0200→ 02FF)
Data is stored in 2's complement binary form, i.e, 01111111 → +full-scale and 10000000→ — full-scale.

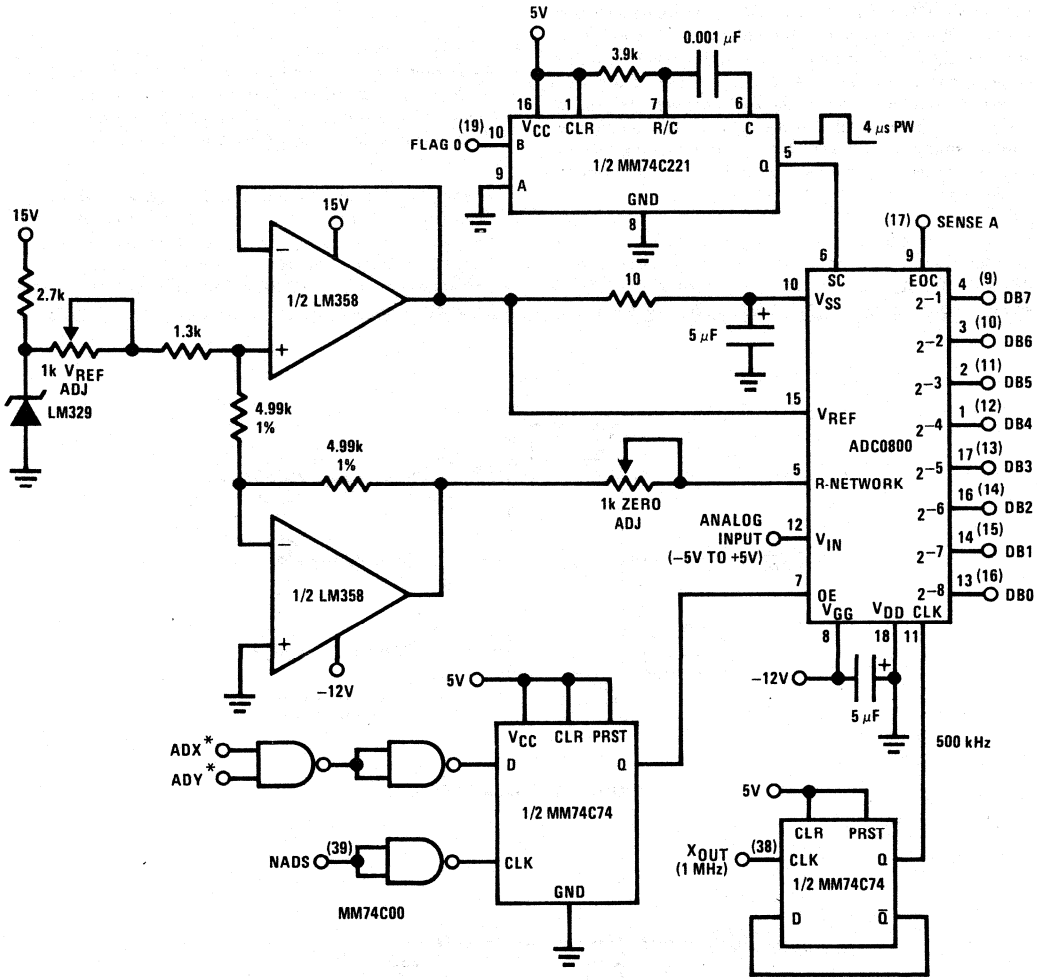
Pointer 3 — LOAD DATA SUBROUTINE (starts at ADDR:0300)
Executed when an EOC signal generates an interrupt request via sense A after an IEN (interrupt enable) instruction.

The address for the converter (0500) is unique for this particular sample program but may not be in a user's system so a different converter address must be used. Note that in *Figure 3* ADX and ADY for the address decode circuitry would be address bits ADB10 and ADB8 (pins 35 and 33 on the SC/MP II package) for converter address 0500.

SAMPLE PROGRAM TO LOAD DATA INTO MEMORY WITH SC/MP II.

```
0001  08     START:      NOP
0002  C4 01               LDIX'01
0004  36                 XPAH 1
0005  C4 00               LDIX'00
0007  31                 XPAL 1      ; P1 = 0100
0008  C4 02               LDIX'02
000A  36                 XPAH 2
000B  C4 00               LDIX'00
000D  C9 00               ST(P1)      ; Zero word count (P1)
000F  32                 XPAL 2      ; P2 = 0200
0010  C4 03               LDIX'03
0012  37                 XPAH 3
0013  08     INITIALIZE: NOP
0014  C4 00               LDIX'00
0016  33                 XPAL 3      ; P3 = 0300
0017  C4 01               LDIX'01
0019  07                 CAS         ; Starts converter via flag 0
001A  C1 00               LD (P1)
001C  F4 FF               XRIX'FF
001E  98 05               JZ DTA IN   ; Test to see if word count is FF,
                                        if so, jump to DTA IN
0020  05                 IEN         ; Enables INTERRUPT
0021  08     LOOP:       NOP
0022  90 FE               JMP LOOP    ; Loop until EOC
0024  08     DTA IN:     NOP
                         .
                         .
                         .           ; User program to process data
                         .
                         .
                         .
   :DATA ENTRY SUBROUTINE
0300  08     DATA IN SR: NOP
0301  A9 00               ILD (P1)    ; Increment word count
0303  C4 05               LDIX'05
0305  35                 XPAH 1      ; P1 will point to converter
0306  C1 00               LD (P1)     ; Converter data loaded into
                                        accumulator
0308  F4 7F               XRIX'7F     ; Put data in 2's complement form
030A  CE 01               ST @ 1(P2)  ; Store data
030C  C4 00               LDIX'00
030E  07                 CAS         ; Resets flag 0
030F  C4 01               LDIX'01
0311  35                 XPAH 1      ; Resets P1 to point at word count
0312  C4 13               LDIX'13
0314  33                 XPAL 3
0315  3F                 XPPC 3      ; Return to INITIALIZE to start a
                                        new conversion
```

Typical Applications (Continued)



- Setting flag 0 (FLG0 = 1) with software, starts conversion (FLG0 must be cleared before another conversion can be initiated)
- With interrupt enabled an EOC will force an interrupt. Interrupt subroutine should load converter data into the accumulator.
- Output data is in complementary offset binary form
- Numbers in parentheses denote pin numbers of SC/MP chip

*ADX and ADY can be any of the address lines but they must be high *only* at the time the converter output data is to be put on the data bus (i.e., the converter must have its own unique address)

FIGURE 3. Interfacing to the SC/MP II Microprocessor

Typical Applications (Continued)

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LED's to display the resulting digital output code as shown in *Figure 4*. Note that the LED drivers invert the digital output of the A/D converter to provide a binary display. A lab DVM can be used if a precision voltage source is not available. After adjusting the zero and full-scale, any number of points can be checked, as desired.

For ease of testing, a 10.24 V_{DC} reference is recommended for the A/D converter. This provides an LSB of 40 mV (10.240/256). To adjust the zero of the A/D, an analog input voltage of 1/2 LSB or 20 mV should be applied and the zero adjust potentiometer should be set to provide a flicker on the LSB LED readout with all the other display LEDs OFF.

To adjust the full-scale adjust potentiometer, an analog input which is 1 1/2 LSB less than the reference (10.240–0.060 or 10.180 V_{DC}) should be applied to the analog input and the full-scale adjusted for a flicker on the LSB LED, but this time with all the other LEDs ON.

A complete circuit for a simple A/D tester is shown in *Figure 5*. Note that the clock input voltage swing and the digital output voltage swings are from 0V to 10.24V. The MM74C901 provides a voltage translation to 5V operation and also the logic inversion so the readout LEDs are in binary.

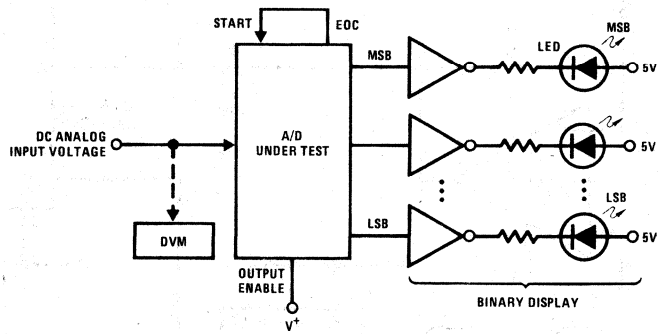


FIGURE 4. Basic A/D Tester

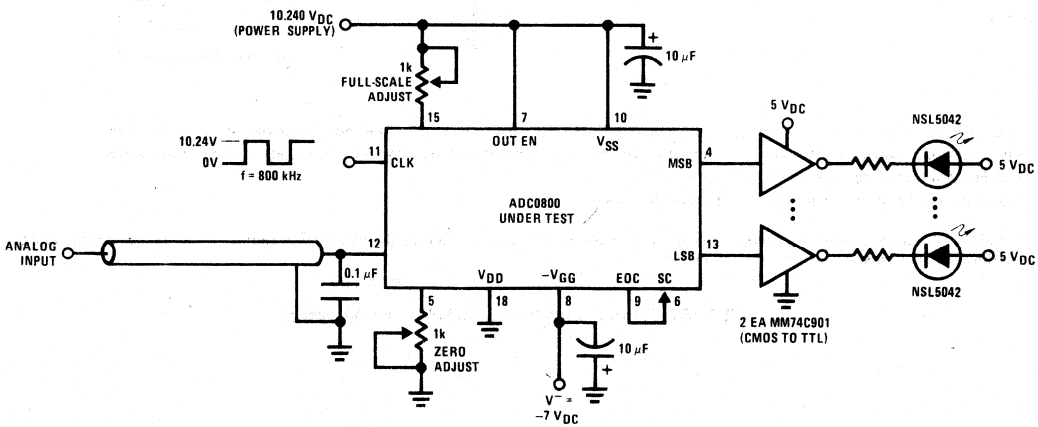


FIGURE 5. Complete Basic Tester Circuit

Typical Applications (Continued)

The digital output LED display can be decoded by dividing the 8 bits into the 4 most significant bits and 4 least significant bits. Table I shows the fractional binary equivalent of these two 8-bit groups. By adding the decoded voltages which are obtained from the column: "Input Voltage Value with a 10.240 V_{REF}" of both the MS and LS groups, the value of the digital display can be determined. For example, for an output LED display of "1011 0110" or "B6" (in hex) the voltage values from the table are 7.04 + 0.24 or 7.280 V_{DC}. These voltage values represent the center values of a perfect A/D converter. The input voltage has to change by ±1/2 LSB (±20 mV), the "quantization uncertainty" of an A/D, to obtain an output digital code change. The effects of this quantization error have to be accounted for in the interpretation of the test results. A plot of this natural error source is shown in *Figure 6* where, for clarity, both the analog input voltage and the error voltage are normalized to LSBs.

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		INPUT VOLTAGE VALUE WITH 10.24 V_{REF}	
		MS GROUP	LS GROUP	MS GROUP	LS GROUP
F	1 1 1 1	15/16	15/256	9.600	0.600
E	1 1 1 0	7/8	7/128	8.960	0.560
D	1 1 0 1	13/16	13/256	8.320	0.520
C	1 1 0 0	3/4	3/64	7.680	0.480
B	1 0 1 1	11/16	11/256	7.040	0.440
A	1 0 1 0	5/8	5/128	6.400	0.400
9	1 0 0 1	9/16	9/256	5.760	0.360
8	1 0 0 0	1/2	1/32	5.120	0.320
7	0 1 1 1	7/16	7/256	4.480	0.280
6	0 1 1 0	3/8	3/128	3.840	0.240
5	0 1 0 1	5/16	5/256	3.200	0.200
4	0 1 0 0	1/4	1/64	2.560	0.160
3	0 0 1 1	3/16	3/256	1.920	0.120
2	0 0 1 0	1/8	1/128	1.280	0.080
1	0 0 0 1	1/16	1/256	0.640	0.040
0	0 0 0 0			0	0

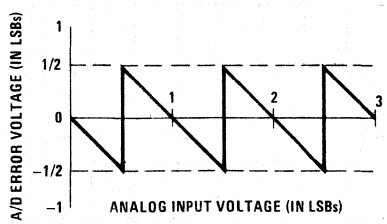


FIGURE 6. Error Plot of a Perfect A/D Showing Effects of Quantization Error

Typical Applications (Continued)

A low speed ramp generator can also be used to sweep the analog input voltage and the LED outputs will provide a binary counting sequence from zero to full-scale.

The techniques described so far are suitable for an engineering evaluation or a quick check on performance. For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in two digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 7*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A–C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 8* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

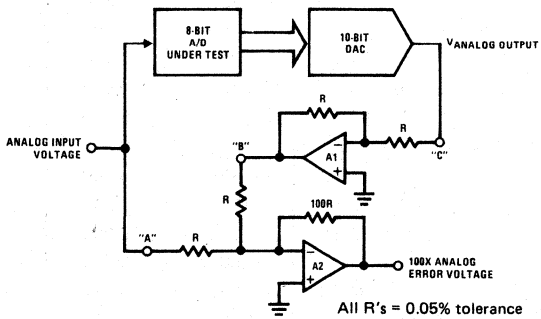


FIGURE 7. A/D Tester with Analog Error Output

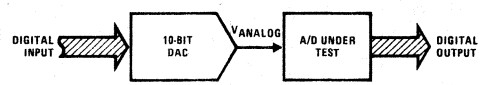
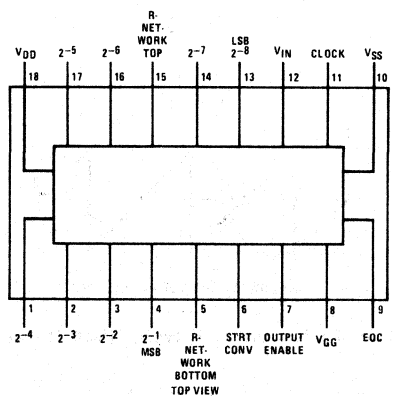


FIGURE 8. Basic "Digital" A/D Tester

Connection Diagram

Dual-In-Line Package



Order Number ADC0800PD (–55°C to +125°C)
or ADC0800PCD (0°C to +70°C)
See NS Package D18A

National Semiconductor

ADC0801, ADC0802, ADC0803, ADC0804 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 are CMOS 8-bit, successive approximation A/D converters which use a modified potentiometric ladder—similar to the 256R products. They are designed to meet the NSC MICROBUS™ standard to allow operation with the 8080A control bus, and TRI-STATE® output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

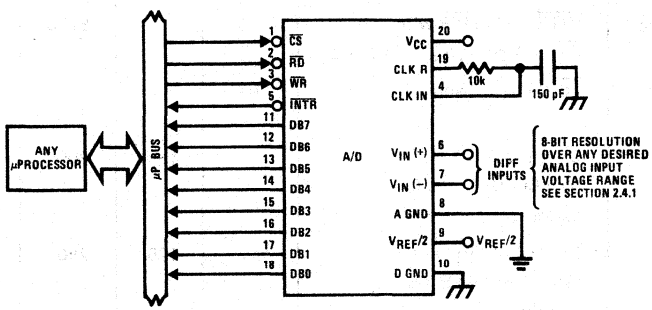
Features

- MICROBUS (8080A) compatible—no interfacing logic needed
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package

Key Specifications

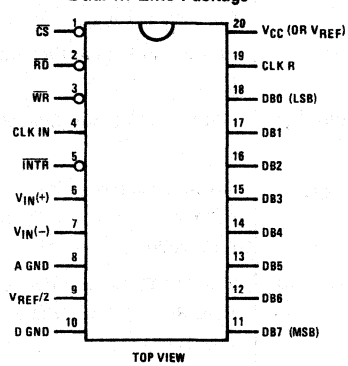
- Resolution 8 bits
- Total error ±1/4 LSB, ±1/2 LSB and ±1 LSB
- Conversion time 100 μs
- Access time 135 ns
- Single supply 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Typical Applications



Connection Diagrams

ADC 080X
Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Input	−0.3V to (V_{CC} +0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0801/02/03 LD	−55°C ≤ T_A ≤ +125°C
ADC0801/02/03/04 LCD	−40°C ≤ T_A ≤ +85°C
ADC0801/02/03/04 LCN	0°C ≤ T_A ≤ 70°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

Converter Specifications:

V_{CC} = 5 V_{DC}, $V_{REF}/2$ = 2.500 V_{DC}, $T_{MIN} \leq T_A \leq T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ADC0801:					
Total Adjusted Error (Note 8)	With Full-Scale Adj.			±1/4	LSB
ADC0802:					
Total Unadjusted Error (Note 8)	Completely Unadjusted			±1/2	LSB
ADC0803:					
Total Adjusted Error (Note 8)	With Full-Scale Adj.			±1/2	LSB
ADC0804:					
Total Unadjusted Error (Note 8)	Completely Unadjusted			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±1/8	LSB

Electrical Characteristics

Timing Specifications: V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency	V_{CC} = 6V, (Note 5) V_{CC} = 5V	100 100	640 640	1280 800	kHz kHz
T_C	Conversion Time	(Note 6)	66		73	1/f_{CLK}
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz			8770	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF (Use Bus Driver IC for Larger C_L)		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	250	ns
t_{WI}	Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

Electrical Characteristics

Digital Levels and DC Specifications:

V_{CC} = 5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS [Note: CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+) - (V_T-)$		0.6	1.3	2.0	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
I_{CC}	Supply Current (Includes Ladder Current)	f_{CLK} = 640 kHz, T_A = 25°C and $\overline{CS}$ = "1"		1.3	2.5	mA
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage	I_O = 1.6 mA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC}	−3			μA_{DC}
		V_{OUT} = 5 V_{DC}			3	μA_{DC}
	Output Short Circuit Current	T_A = 25°C				
I_{SOURCE}		V_{OUT} Short to Gnd	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}	9.0	16		mA_{DC}

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: With V_{CC} = 6V, the digital logic interfaces are no longer TTL compatible.

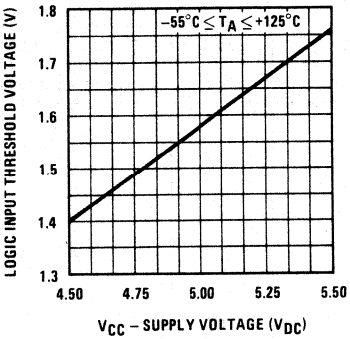
Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

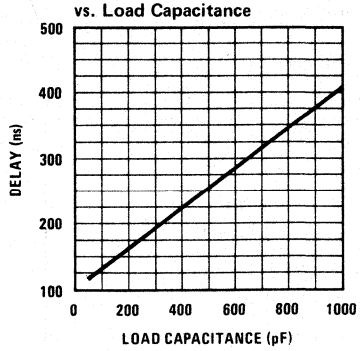
Note 8: None of these A/Ds requires a zero adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the $V_{IN}(-)$ input can be adjusted to achieve this. See section 2.5 and *Figure 19.*

Typical Performance Characteristics

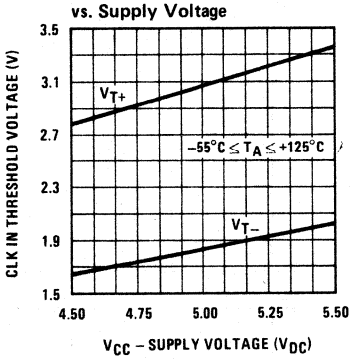
Logic Input Threshold Voltage vs. Supply Voltage



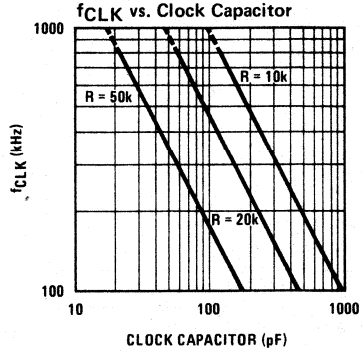
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



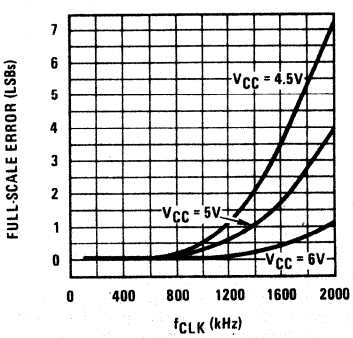
CLK IN Schmitt Trip Levels vs. Supply Voltage



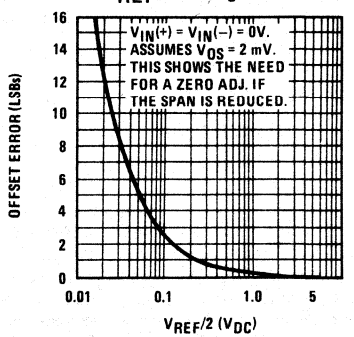
f_{CLK} vs. Clock Capacitor



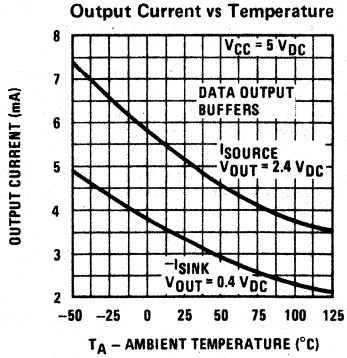
Full-Scale Error vs f_{CLK}



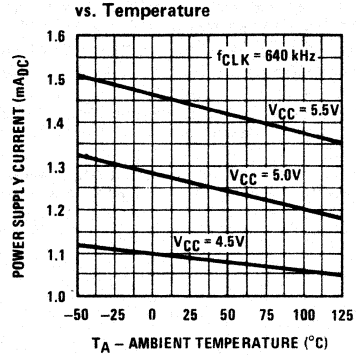
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



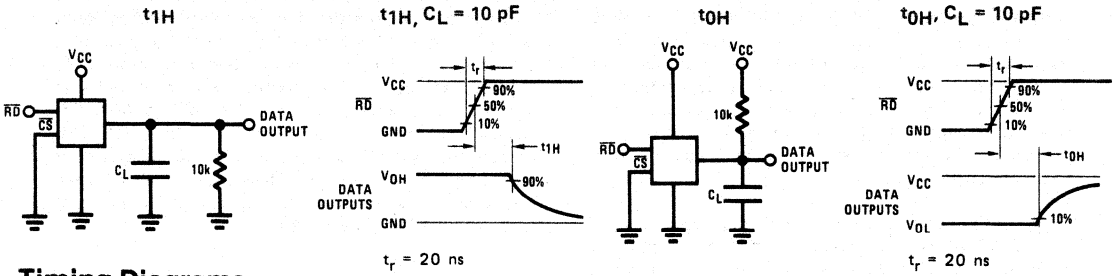
Output Current vs Temperature



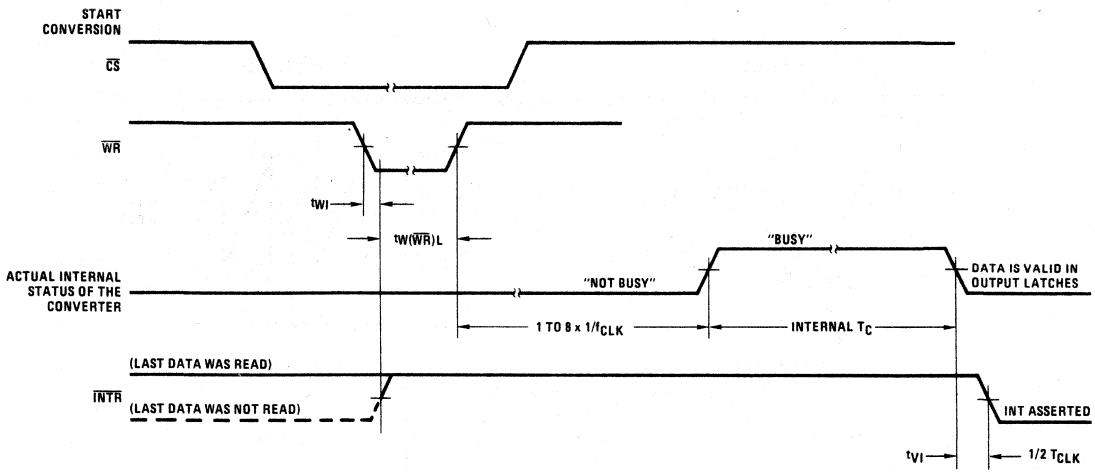
Power Supply Current vs. Temperature



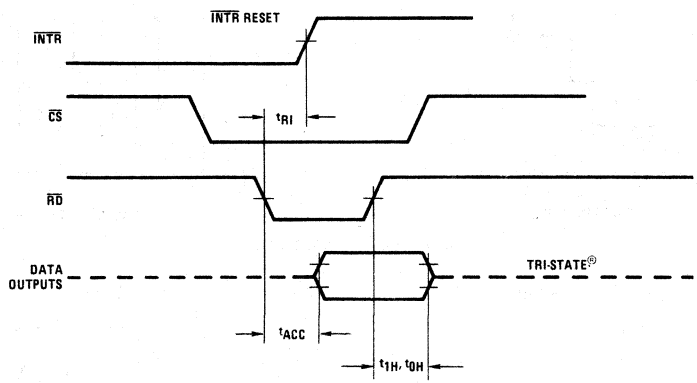
TRI-STATE® Test Circuits and Waveforms



Timing Diagrams



Output Enable and Reset $\overline{INTR}$



Note: All timing is measured from the 50% voltage points.

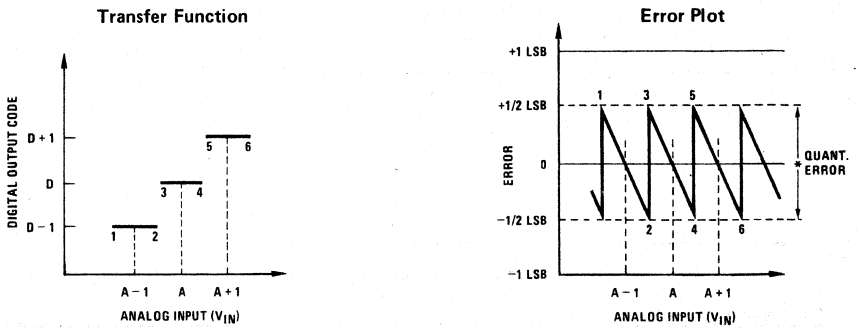
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a.* The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±1/2 LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ±1/2 LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

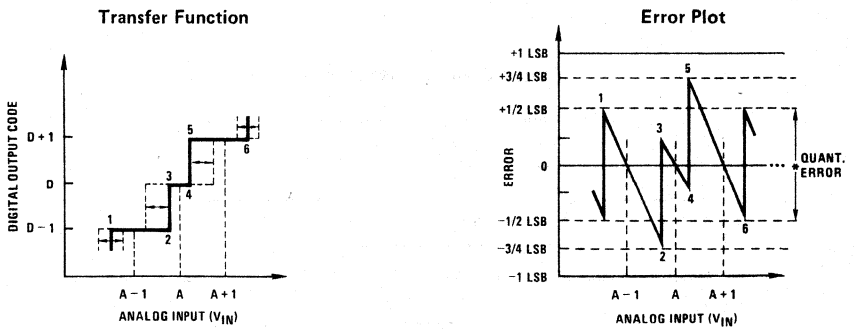
Figure 1b shows worst case error plot for ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±1/4 LSB. In other words, if we apply an analog input equal to the center-value ±1/4 LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than 1/2 LSB.

The error curve of *Figure 1c* shows worst case error plot for ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

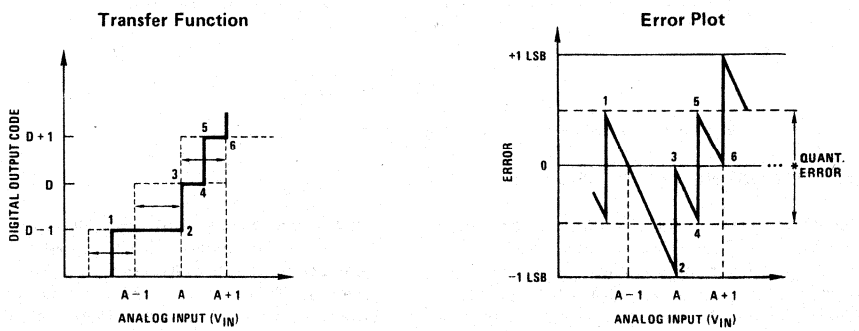
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +1/2 LSB because the digital code appeared 1/2 LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy = ±0 LSB A Perfect A/D



b) Accuracy = ±1/4 LSB



c) Accuracy = ±1/2 LSB

FIGURE 1. Clarifying the Error Specs of an A/D Converter

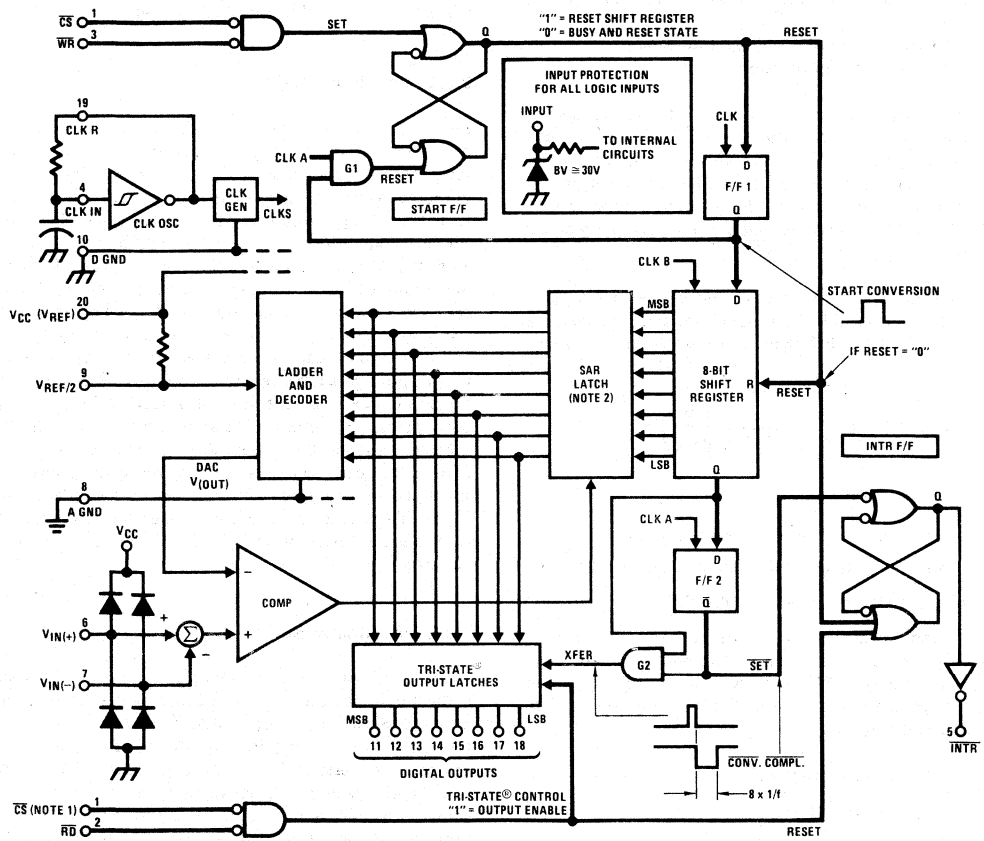
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ = 0. To insure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion in process can be interrupted by issuing a second start command.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2.* All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt ($\overline{INTR}$) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D flop, F/F 2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When F/F 2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-1/2 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)\ (2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to 1/4 LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_e(MAX)\ (f_{CLK})]}{(2\pi f_{cm})\ (4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\ (640 \times 10^3)}{(6.28)\ (60)\ (4.5)}$$

which gives

$V_P \cong 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see section 2.4 Reference Voltage Flexibility).

2.3 Analog Inputs

2.3.1 Input Current

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground. The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($\leq$ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($\leq$ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.3). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 3.*

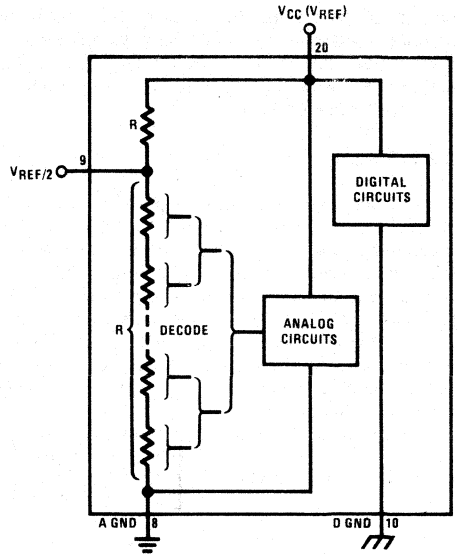


FIGURE 3. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either 1/2 of the voltage which is applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the $V_{REF}/2$ voltage.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V. With 0.5 V_{DC} applied to the V_{IN} (−) pin to absorb the offset, the reference voltage can be made equal to 1/2 of the 3V span or 1.5 V_{DC}. The A/D now will encode the V_{IN} (+) signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) is available which operates with a 5V input voltage and has a temperature stability of 1.8 mV typ (6 mV max) over $0^{\circ}C \leq T_A \leq +70^{\circ}C$. Other temperature range parts are also available.

2.5 Errors

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D V_{IN} (−) input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V (−) input and applying a small magnitude positive voltage to the V (+)

input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal 1/2 LSB value (1/2 LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1-1/2 LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span adjusted $V_{REF}/2$ voltage, the full-scale adjustment is made by inputting V_{MIN} to the V_{IN} (−) input of the A/D and applying a voltage to the V_{IN} (+) input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX}-V_{MIN})}{256}\right]$$

where:

V_{MAX} = The high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 4.*

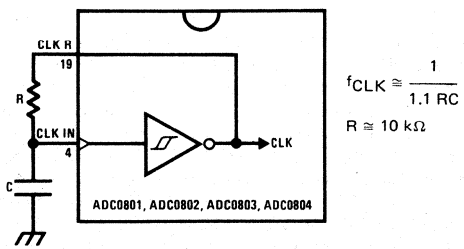


FIGURE 4. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power T^2L buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard T^2L buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to insure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky is recommended such as the DM74LS240 series) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 5*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120 − 1 1/2 LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the decoded voltages which are obtained from the column: Input voltage value for a 2.560 $V_{REF}/2$ of both the MS and the LS groups, the value of the digital display can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in 2 digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 6*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A–C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 7*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

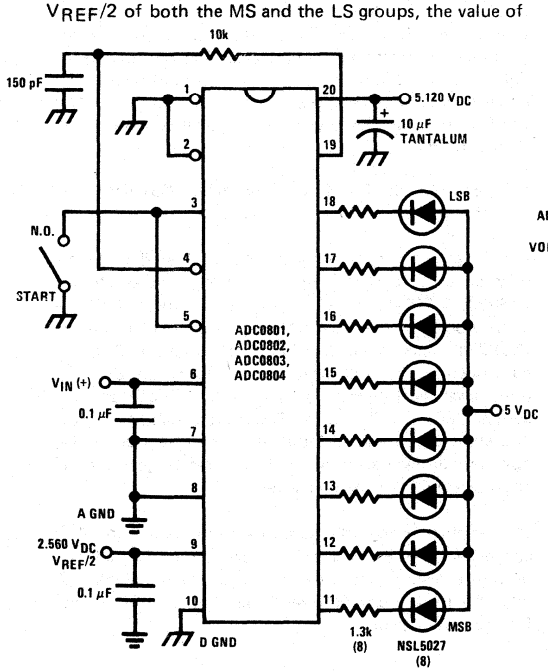


FIGURE 5. Basic A/D Tester

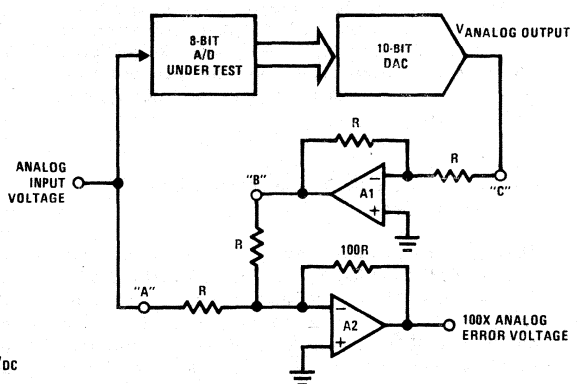


FIGURE 6. A/D Tester with Analog Error Output

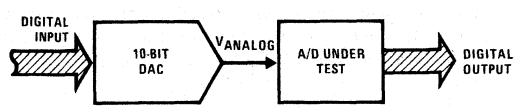


FIGURE 7. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2.880	0.180
8	1 0 0 0	1/2	1/32	2.560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	5/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1.280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

*V Display Output = VMS Group + VLS Group

4.0 MICROPROCESSOR INTERFACING

To discuss the interface with 8080A, 6800 and SC/MP-II microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored at location 0200 to 020F. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

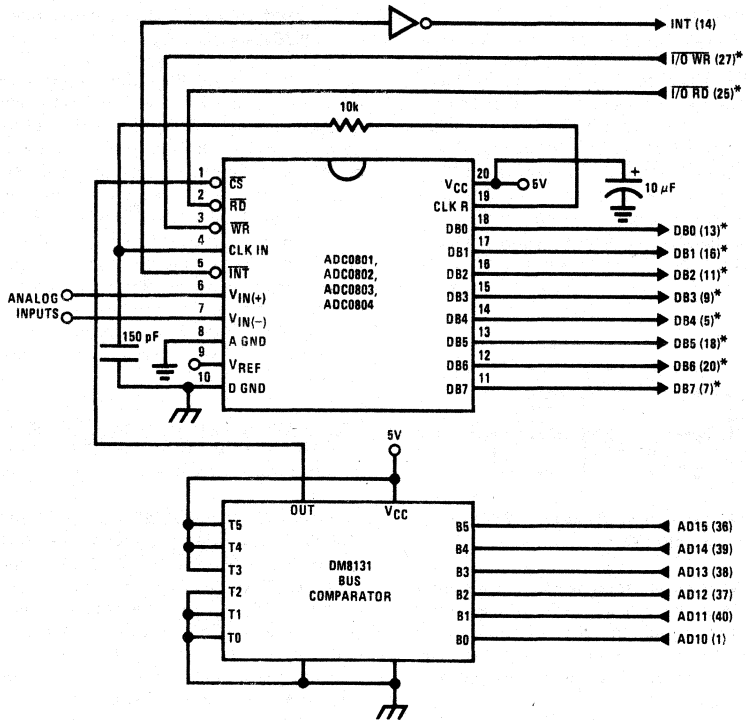
This converter has been designed to directly interface with an 8080A-2 microprocessor (MICROBUS class 2). The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space in shown in *Figure 8.*

The standard control bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bidirectional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.



Note 1: *Pin numbers for the INS8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 8. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 8* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:      JMP      LD DATA
  .        .          .
  .        .          .
0100    21 00 02    START:      LXI H 0200H      ; HL pair will point to
                                                 ; data storage locations
0103    31 00 04    RETURN:     LXI SP 0400H     ; Initialize stack pointer (Note 1)
0106    7D                      MOV A, L         ; Test # of bytes entered
0107    FE OF                   CPI OF H         ; If # = 16. JMP to
0109    CA 13 01                JZ CONT          ; user program
010C    D3 E0                   OUT E0 H         ; Start A/D
010E    FB                      EI               ; Enable interrupt
010F    00          LOOP:       NOP              ; Loop until end of
0110    C3 0F 01                JMP LOOP         ; conversion
0113       .        CONT:          .
  .        .          .              .
  .        .       (User program to  .
  .        .       process data)     .
  .        .          .              .
  .        .          .              .
0300    DB E0       LD DATA:    IN E0 H          ; Load data into accumulator
0302    77                      MOV M, A         ; Store data
0303    23                      INX H            ; Increment storage pointer
0304    C3 03 01                JMP  RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All addresses used were arbitrarily chosen.

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 9*.

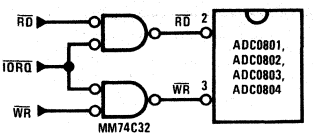


FIGURE 9. Mapping the A/D as an I/O device for use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 10* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using 1/2 DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

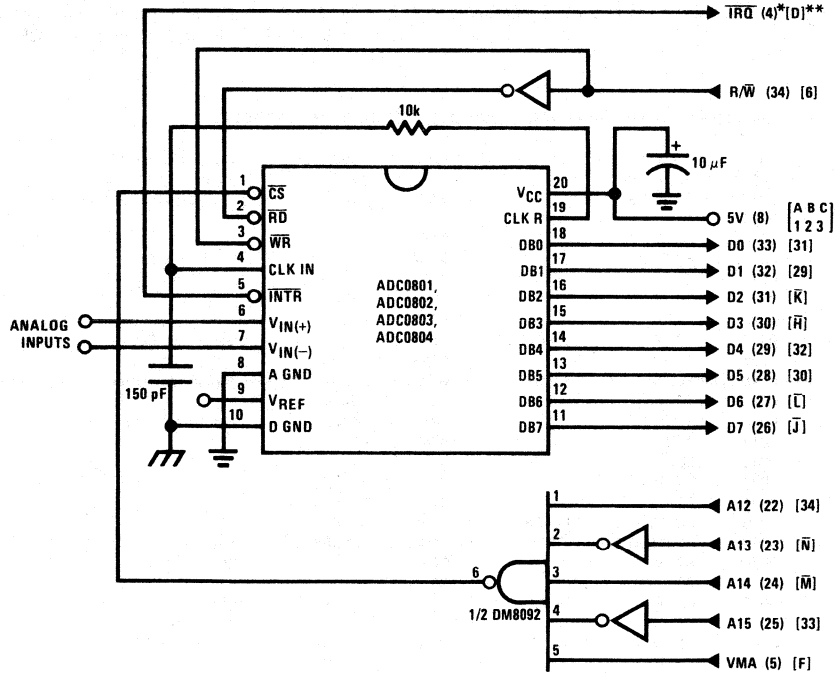
The following subroutine essentially performs the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 11* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–MC6800 CPU INTERFACE

```
0010  DF 36       DATAIN   STX   TEMP2     ; Save contents of X
0012  CE 00 2C             LDX   #$002C    ; Upon IRQ low CPU
0015  FF FF F8             STX   $FFF8     ; jumps to 002C
0018  B7 50 00             STAA  $5000     ; Starts ADC0801
001B  0E                   CLI
001C  3E         CONVRT    WAI             ; Wait for interrupt
001D  DE 34                LDX   TEMP1
001F  8C 02 0F             CPX   #$020F    ; Is final data stored?
0022  27 14                BEQ   ENDP
0024  B7 50 00             STAA  $5000     ; Restarts ADC0801
0027  08                   INX
0028  DF 34                STX   TEMP1
002A  20 F0                BRA   CONVRT
002C  DE 34      INTRPT    LDX   TEMP1
002E  B6 50 00             LDAA  $5000     ; Read data
0031  A7 00                STAA  X         ; Store it at X
0033  3B                   RTI
0034  02 00      TEMP1     FDB   $0200     ; Starting address for
                                           ; data storage
0036  00 00      TEMP2     FDB   $0000
0038  CE 02 00   ENDP      LDX   #$0200    ; Reinitialize TEMP1
003B  DF 34                STX   TEMP1
003D  DE 36                LDX   TEMP2
003F  39                   RTS             ; Return from subroutine
                                           ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers or letters in brackets refer to standard M6800 system common bus code.

FIGURE 10. ADC0801 – MC6800 CPU Interface

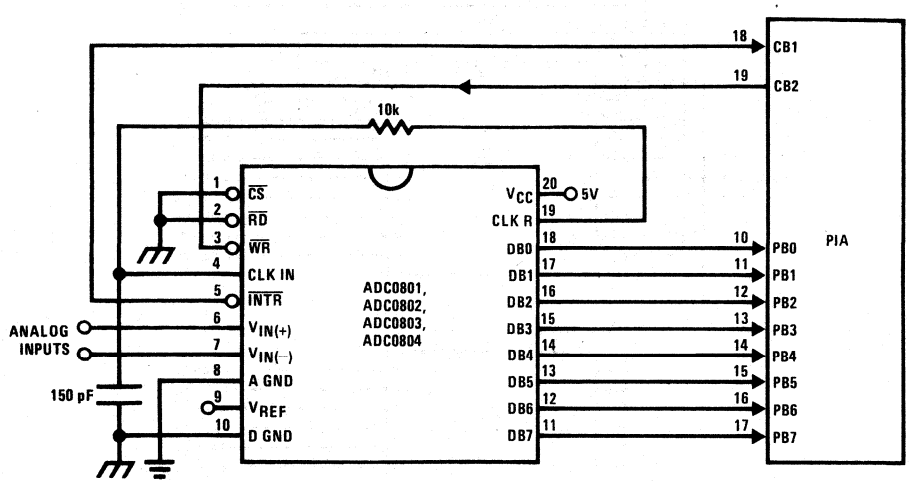


FIGURE 11. ADC0801–MC6820 PIA Interface

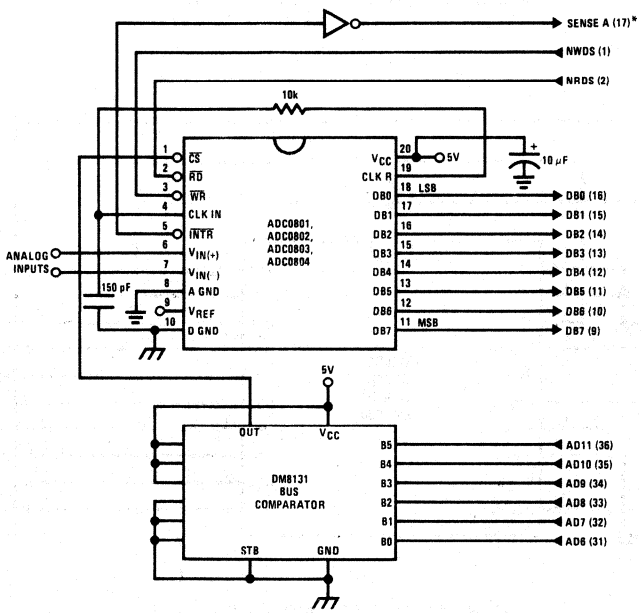
A sample interface program equivalent to the previous one, is shown below. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

4.4 Interfacing the INS8060—SC/MP-II

The SC/MP-II interface technique with the ADC0801 series *Figure 12*, is similar to the 8080A CPU interface.

SAMPLE PROGRAM FOR *FIGURE 11* ADC0801—MC6820 PIA INTERFACE

```
0010  CE 00 38   DATAIN   LDX   #$0038   ; Upon IRQ low CPU
0013  FF FF F8            STX   $FFF8    ; jumps to 0038
0016  B6 80 06            LDAA  PIAORB   ; Clear possible IRQ flags
0019  4F                  CLRA
001A  B7 80 07            STAA  PIACRB
001D  B7 80 06            STAA  PIAORB   ; Set Port B as input
0020  0E                  CLI
0021  C6 34               LDAB  #$34
0023  86 3D               LDAA  #$3D
0025  F7 80 07   CONVRT   STAB  PIACRB   ; Starts ADC0801
0028  B7 80 07            STAA  PIACRB
002B  3E                  WAI            ; Wait for interrupt
002C  DE 40               LDX   TEMP1
002E  8C 02 0F            CPX   #$020F   ; Is final data stored?
0031  27 0F               BEQ   ENDP
0033  08                  INX
0034  DF 40               STX   TEMP1
0036  20 ED               BRA   CONVRT
0038  DE 40   INTRPT      LDX   TEMP1
003A  B6 80 06            LDAA  PIAORB   ; Read data in
003D  A7 00               STAA  X        ; Store it at X
003F  3B                  RTI
0040  02 00   TEMP1       FDB   $0200    ; Starting address for
                                         ; data storage
0042  CE 02 00 ENDP       LDX   #$0200   ; Reinitialize TEMP1
0045  DF 40               STX   TEMP1
0047  39                  RTS            ; Return from subroutine
      PIAORB  EQU   $8006   ; To user's program
      PIACRB  EQU   $8007
```



*Pin numbers in parentheses are for the SC/MP CPU.

FIGURE 12. ADC0801 – SC/MP-II Microprocessor Interface

The A/D is treated as a peripheral and it is mapped into the memory space of the SC/MP-II system. An address, 0D00, is assigned to the A/D and the $\overline{CS}$ signal is shown to be decoded by a bus comparator, DM8131. The $\overline{RD}$ and $\overline{WR}$ pins of the A/D are tied directly to the Write Data Strobe, NWRS, and Read Data Strobe, NRDS, pins of the SC/MP-II CPU. Notice that the $\overline{INTR}$ signal should be inverted before being tied to the SENSE A pin of the SC/MP-II. A sample interface program is shown below.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor which is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 13.*

SAMPLE PROGRAM FOR *FIGURE 12* ADC0801–SC/MP-II MICROPROCESSOR INTERFACE

```
0100        08                  NOP
0101   C4   02                  LDI02
0103        35                  XPAH(P1)
0104   C4   0D                  LDI0D
0106        36                  XPAH(P2)
0107   C4   03                  LDI03
0109        37                  XPAH(P3)
010A   C4   00                  LDI00
010C        31                  XPAL(P1)      ; P1=0200, P1 points to 1st byte address
010D   C4   00                  LDI00
010F   C9   11                  ST(P1+11)     ; Zero the byte count in address 0211
0112        32                  XPAL(P2)      ; P2=0D00, P2 points to A/D
0113   CA   00        START:    ST(P2)        ; START the A/D
0115   C4   00                  LDI00
0117        33                  XPAL(P3)      ; P3=0300, P3 points to DATA in sub.
0118        05                  IEN           ; starting address
0119        08        LOOP:     NOP
011A   90   FE                  JMP(LOOP)
                      User's Program
011C                  USER      NOP
011D                            NOP
                                .
                                .
                                .
0300   C2   00        DATA IN:  LD(P2)        ; Load A/D data into accumulator
0302   CD   01                  ST@1(P1)      ; Store A/D data and increment byte
                                              ; address
0304   A9   11                  1LD(P1+11)    ; Increment byte count
0306   C4   0F                  LDI0F
0308        03                  SCL
0309   F9   11                  CAD(P1+11)    ; 0F–(P1+11): Is byte count = 16?
030B   9B   03                  JZ(USER)      ; If byte count = 16 jump to user's
                                              ; program
030D   C4   13                  LDI13
030F        33                  XPAL(P3)      ; P3=0113
0310        3F                  XPPC(P3)      ; Go to START and do another conversion
```

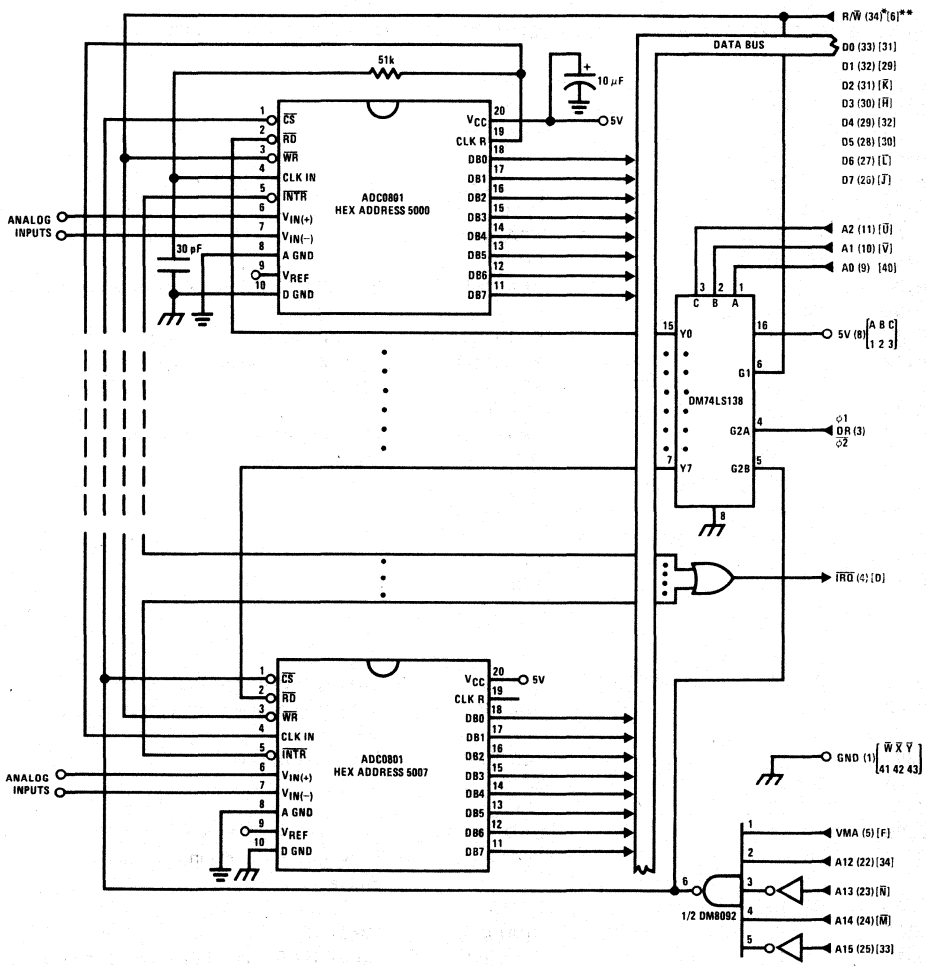
The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers or letters in brackets refer to standard M6800 system common bus code.

FIGURE 13. Interfacing Multiple A/Ds in a MC6800 System

PROGRAM FOR *FIGURE 13* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0010	DF 44	DATAIN	STX	TEMP	;Save Contents of X
0012	CE 00 2A		LDX	#$002A	;Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	;Jumps to 002A
0018	B7 50 00		STAA	$5000	;Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		;Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	;Reset both INDEX
0022	CE 02 00		LDX	#$0200	;1 and 2 to starting
0025	DF 42		STX	INDEX2	;addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		;Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	;INDEX1 → X
002C	A6 00		LDAA	X	;Read data in from A/D at X
002E	08		INX		;Increment X by one
002F	DF 40		STX	INDEX1	;X → INDEX1
0031	DE 42		LDX	INDEX2	;INDEX2 → X
0033	A7 00		STAA	X	;Store data at X
0035	8C 02 07		CPX	#$0207	;Have all A/D's been read?
0038	27 05		BEQ	RETURN	;Yes: branch to RETURN
003A	08		INX		;No: increment X by one
003B	DF 42		STX	INDEX2	;X → INDEX2
003D	20 EB		BRA	INTRPT	;Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	;Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	;Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

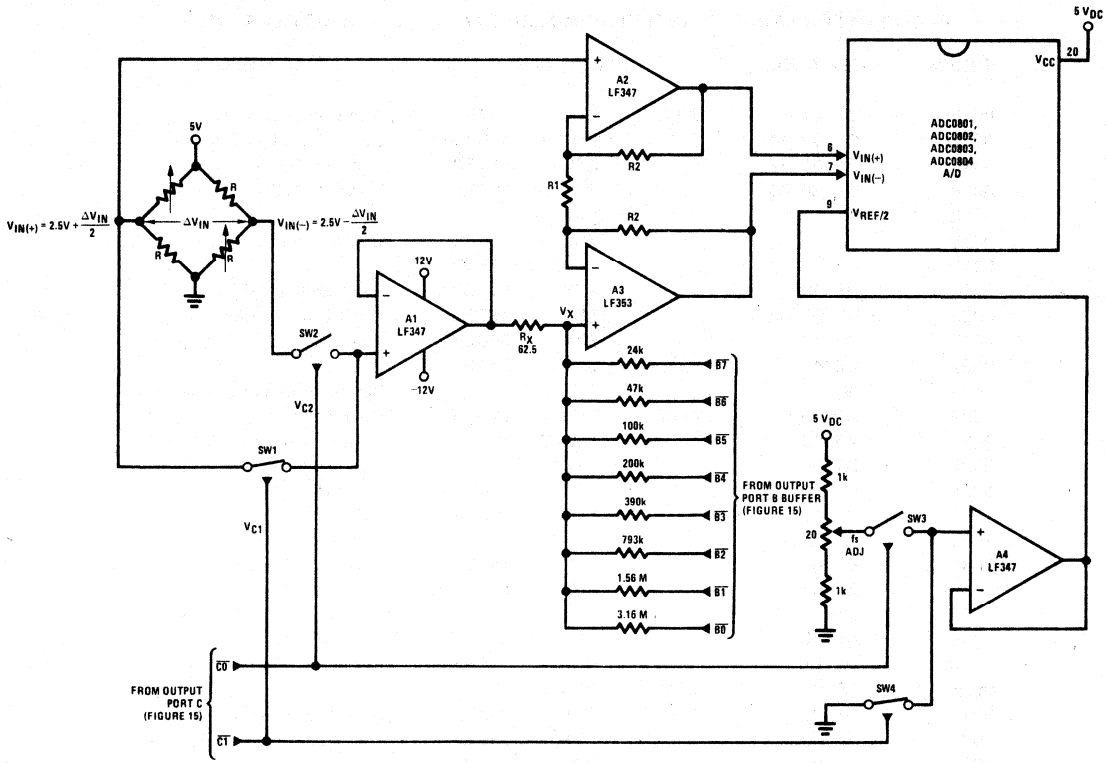
For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 14* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for 1/4 LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} + \underbrace{(V_{os2} - V_{os1} - V_{os3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{os1} + V_{os3} - V_{os2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programmable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 15*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_X increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by insuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 μV which will null the offset error term to 1/4 LSB of full-scale for the ADC0801. It is important that the voltage levels which drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 1: R2 = 49.5 R1

Note 2: Switches are CD4066BC CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 14. Gain of 100 Differential Transducer Preamp

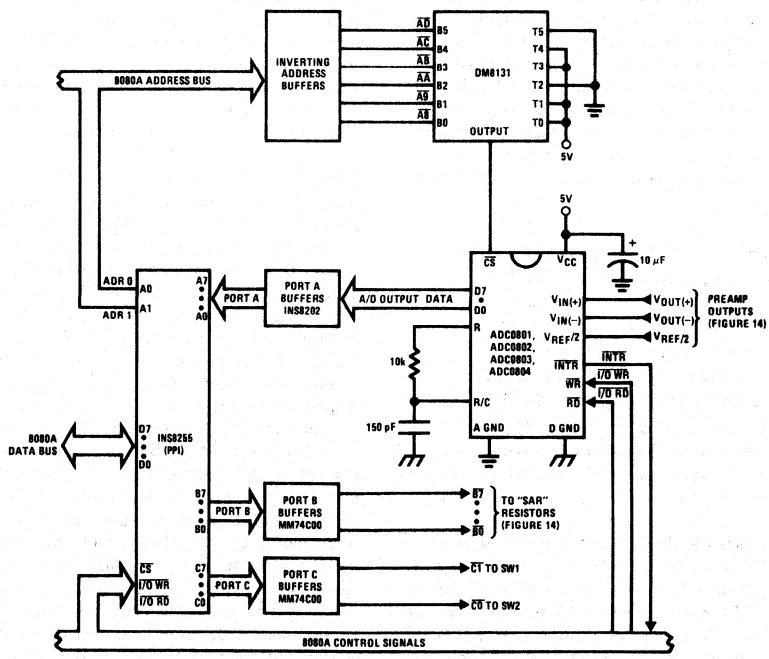


FIGURE 15. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 16*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 17*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4
Port B is at port address E5
Port C is at port address E6
PPI control word port is at port address E7
Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5-3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 18* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

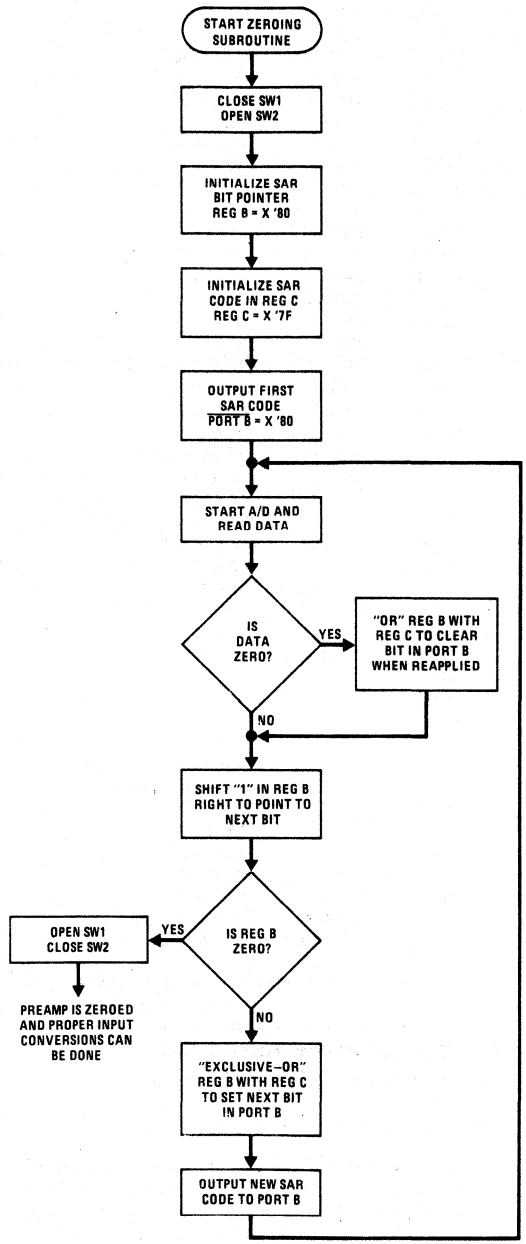


FIGURE 16. Flow Chart for Auto-Zero Routine

```
3D00   3E90     MVI 90
3D02   D3E7     Out Control Port                    ; Program PPI
3D04   2601     MVI H 01          Auto-Zero Subroutine
3D06   7C       MOV A,H
3D07   D3E6     OUT C                              ; Close SW1, open SW2
3D09   0680     MVI B 80                           ; Initialize SAR bit pointer
3D0B   3E7F     MVI A 7F                           ; Initialize SAR code
3D0D   4F       MOV C,A           Return
3D0E   D3E5     OUT B                              ; Port B = SAR code
3D10   31AA3D   LXI SP 3DAA       Start            ; Dimension stack pointer
3D13   D3E4     OUT A                              ; Start A/D
3D15   FB       IE
3D16   00       NOP               Loop             ; Loop until INT asserted
3D17   C3163D   JMP Loop
3D1A   7A       MOV A,D           Auto-Zero
3D1B   C600     ADI 00
3D1D   CA2D3D   JZ Set C                           ; Test A/D output data for zero
3D20   78       MOV A,B           Shift B
3D21   F600     ORI 00                             ; Clear carry
3D23   1F       RAR                                ; Shift "1" in B right one place
3D24   FE00     CPI 00                             ; Is B zero? If yes last
3D26   CA373D   JZ Done                            ; approximation has been made
3D29   47       MOV B,A
3D2A   C3333D   JMP New C
3D2D   79       MOV A,C           Set C
3D2E   B0       ORA B                              ; Set bit in C that is in same
3D2F   4F       MOV C,A                            ; position as "1" in B
3D30   C3203D   JMP Shift B
3D33   A9       XRA C             New C            ; Clear bit in C that is in
3D34   C30D3D   JMP Return                         ; same position as "1" in B
3D37   47       MOV B,A           Done             ; then output new SAR code.
3D38   7C       MOV A,H                            ; Open SW1, close SW2 then
3D39   EE03     XRI 03                             ; proceed with program. Preamp
3D3B   D3E6     OUT C                              ; is now zeroed.
3D3D                .             Normal
                    .
                    .
                Program for processing
                proper data values
3C3D   DBE4     IN A              Read A/D Subroutine  ; Read A/D data
3C3F   EEFF     XRI FF                             ; Invert data
3C41   57       MOV D,A
3C42   78       MOV A,B                            ; Is B Reg = 0? If not stay
3C43   E6FF     ANI FF                             ; in auto zero subroutine
3C45   C21A3D   JNZ Auto-Zero
3C48   C33D3D   JMP Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 17. Software for Auto-Zeroed Differential A/D

5-3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

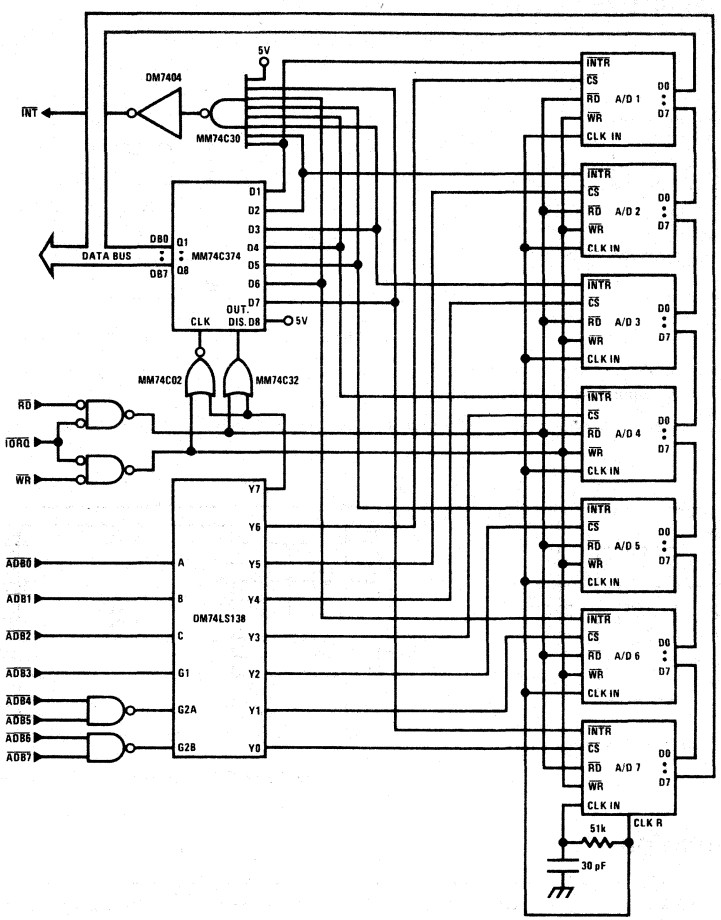


FIGURE 18. Multiple A/D's with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	; Save contents of all registers affected by
0039	C5		PUSH BC	; this subroutine.
003A	F5		PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01		LD C,X01	; C register will be port ADDR of A/D converters.
0040	D300		OUT X00,A	; Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	; Load status word into accumulator.
0044	47		LD B,A	; Save the status word.
0045	79	TEST	LD A,C	; Test to see if the status of all A/D's have
0046	FE 08		CP, X08	; been checked. If so, exit subroutine.
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	; Test a single bit in status word by looking for
004C	1F		RRA	; a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	; is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	; If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF		XOR FF	; the data.
0059	77		LD (HL),A	; Store the data.
005A	2C		INC L	
005B	71		LD (HL),C	; Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	; Test next bit in status word.
0060	F1	DONE	POP AF	; Re-establish all registers as they were
0061	C1		POP BC	; before the interrupt.
0062	E1		POP HL	
0063	C9		RET	; Return to original program.

Typical Applications (Continued)

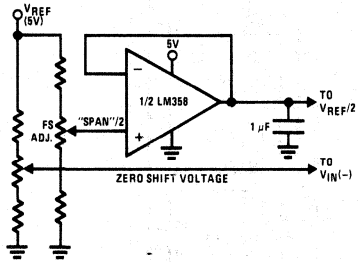


FIGURE 19. Offsetting the Zero of the ADC0801 and Performing an Input Range (Span) Adjustment

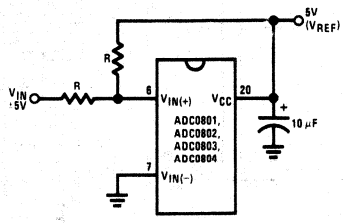


FIGURE 20. Handling ±5V Analog Input Range

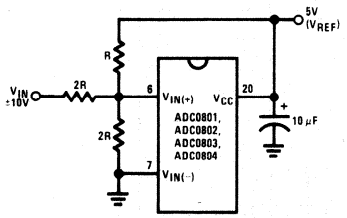


FIGURE 21. Handling ±10V Analog Input Range

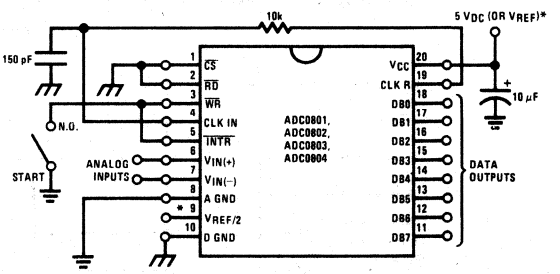


FIGURE 22. Free Running Connection

Ordering Information

TEMPERATURE RANGE		0°C TO +70°C	−40°C TO +85°C	−55°C TO +125°C
ERROR	±1/4 Bit Adjusted	ADC0801LCN	ADC0801LCD	ADC0801LD
	±1/2 Bit Unadjusted	ADC0802LCN	ADC0802LCD	ADC0802LD
	±1/2 Bit Adjusted	ADC0803LCN	ADC0803LCD	ADC0803LD
	±1 Bit Unadjusted	ADC0804LCN	ADC0804LCD	
PACKAGE OUTLINE		N20A–MOLDED DIP	D20A–CAVITY DIP	D20A–CAVITY DIP

National Semiconductor

ADC0808, ADC0809 8-Bit μP Compatible A/D Converters With 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

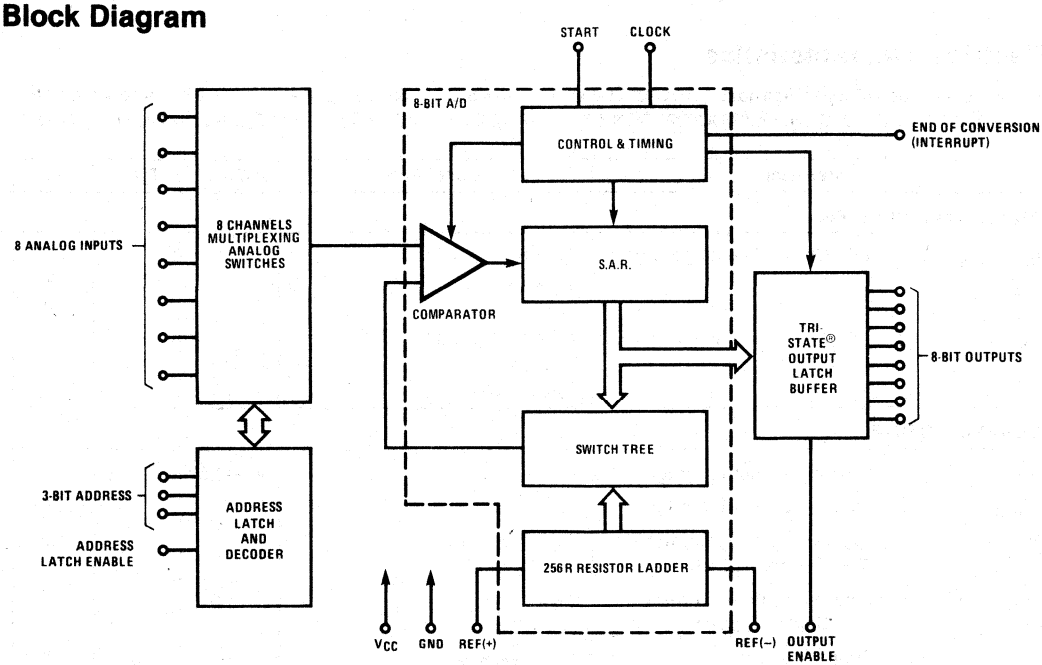
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet.

Features

- Resolution — 8-bits
- Total unadjusted error — ±1/2 LSB and ±1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 8-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 28-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CJ	−55°C ≤ T_A ≤ +125°C
ADC0808CCJ, ADC0808CCN, ADC0809CCN	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC} = 5 V_{DC} = $V_{REF(+)}$, $V_{REF(-)}$ = GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			± 1/2	LSB
	(Note 5)	T_{MIN} to T_{MAX}			± 3/4	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			± 1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			± 1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ 4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted
ADC0808CCJ, ADC0808CCN, and ADC0809CCN 4.75 ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted

	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V,				
		T_A = 25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0,				
		T_A = 25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted
ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

Parameter		Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2$ mA			0.45	V
I_{OUT}	TRI-STATE Output Current	$V_O = 5V$			3	μA
		$V_O = 0$	-3			μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	μs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		$8 + 2\ \mu s$	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE® Output Capacitance	At TRI-STATE® Outputs, (Note 12)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

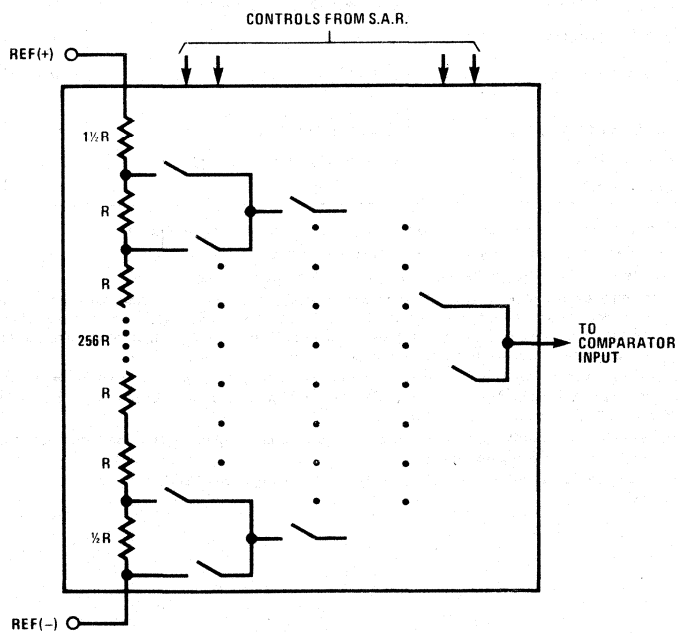


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

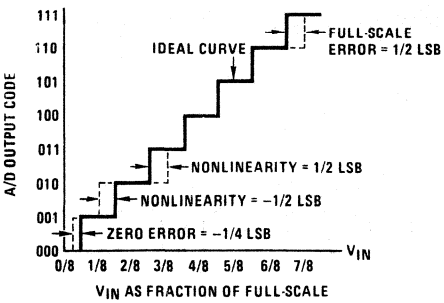


FIGURE 2. 3-Bit A/D Transfer Curve

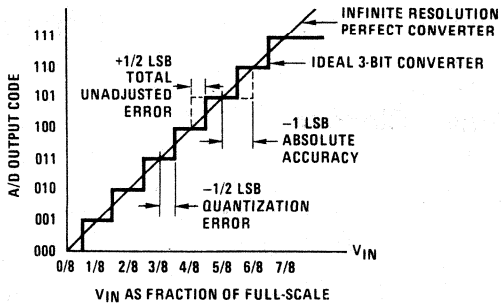


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

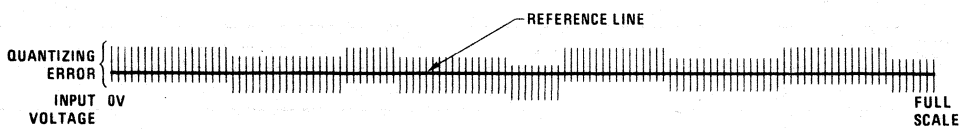
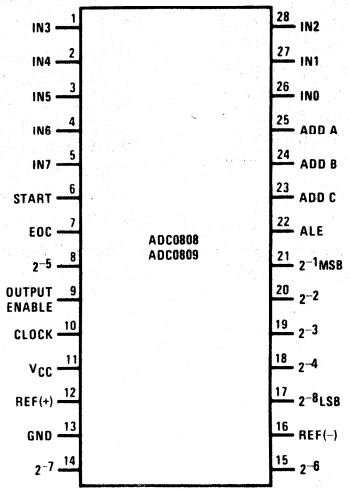


FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



TOP VIEW

Timing Diagram

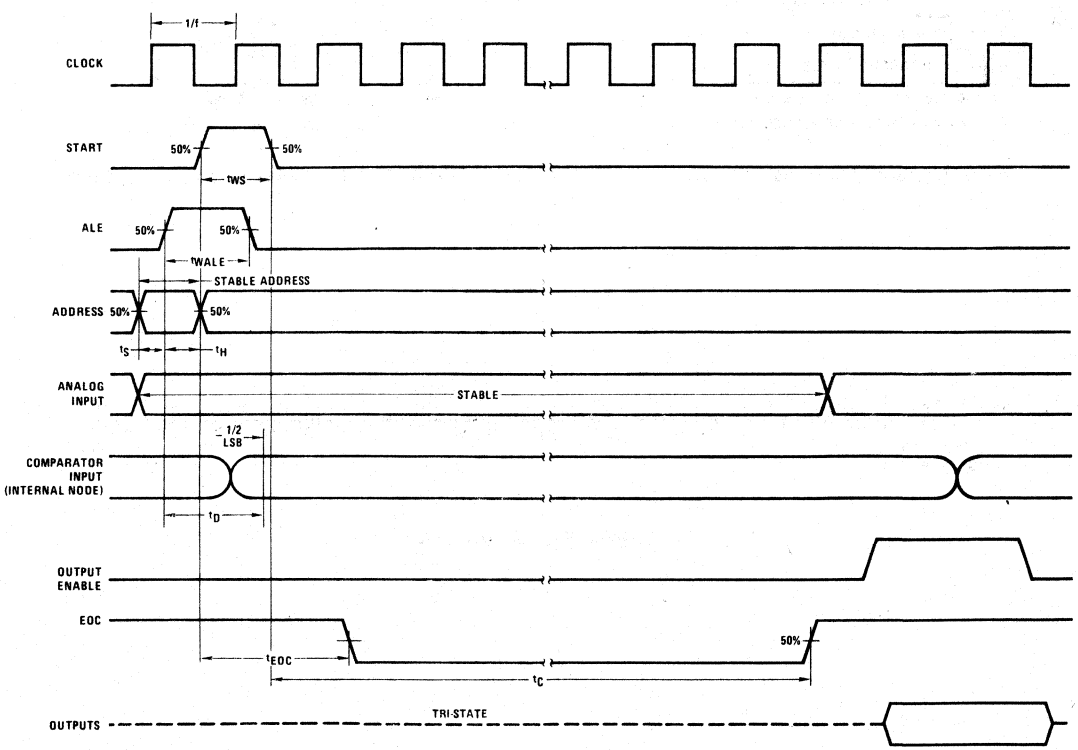


FIGURE 5

Typical Performance Characteristics

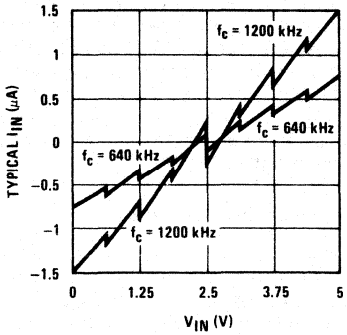


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

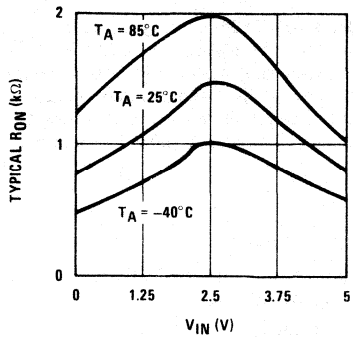


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

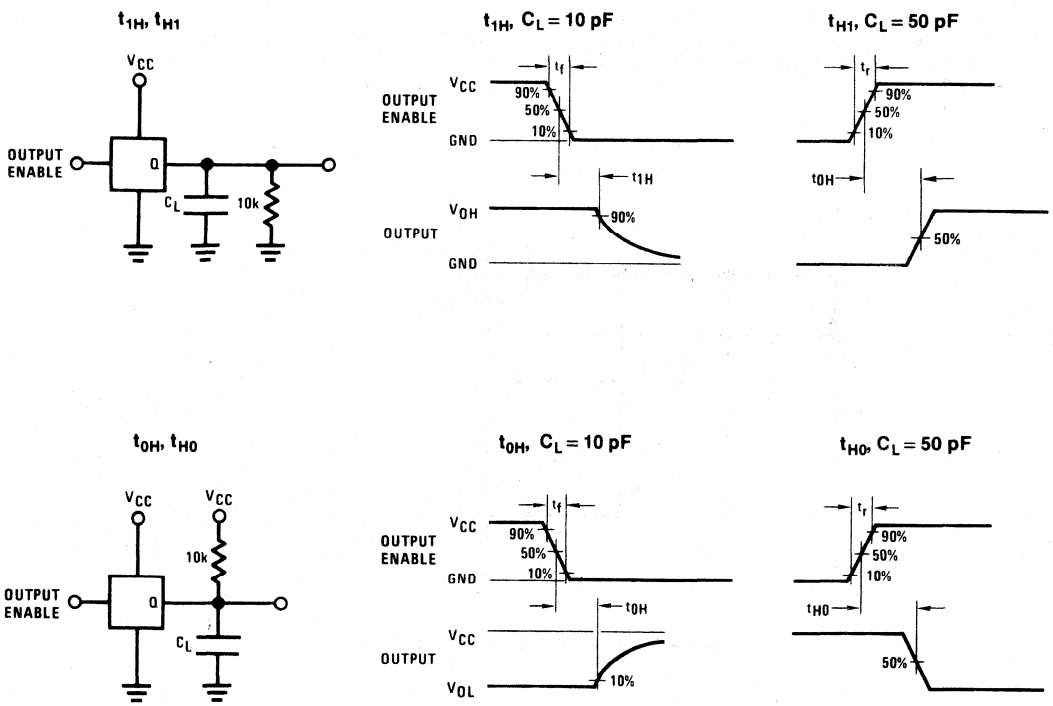


FIGURE 8

Applications Information

OPERATION

1.0 Ratiometric Conversion

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0808
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

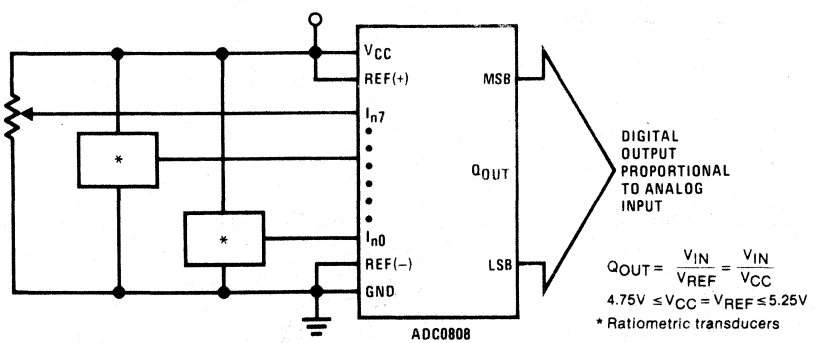


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

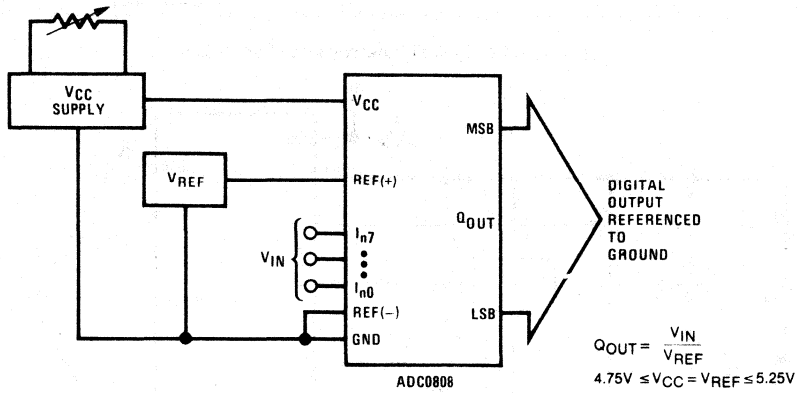


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

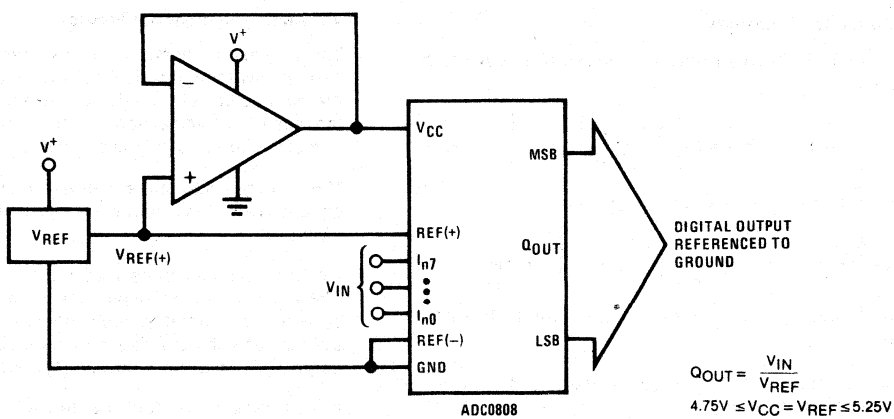


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

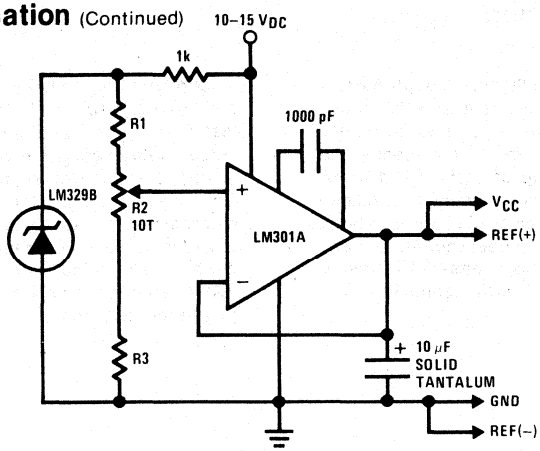


FIGURE 12. Typical Reference and Supply Circuit

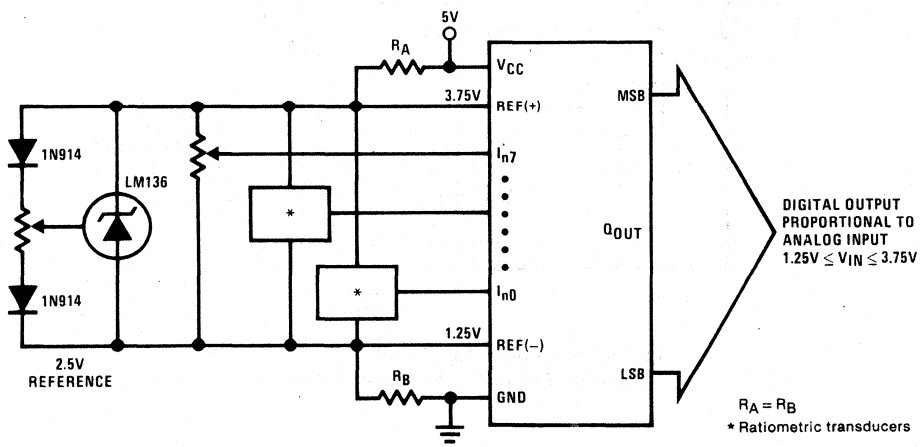


FIGURE 13. Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE}\right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256}\right] \pm V_{TUE}\right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(−)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

4.0 Analog Comparator Inputs

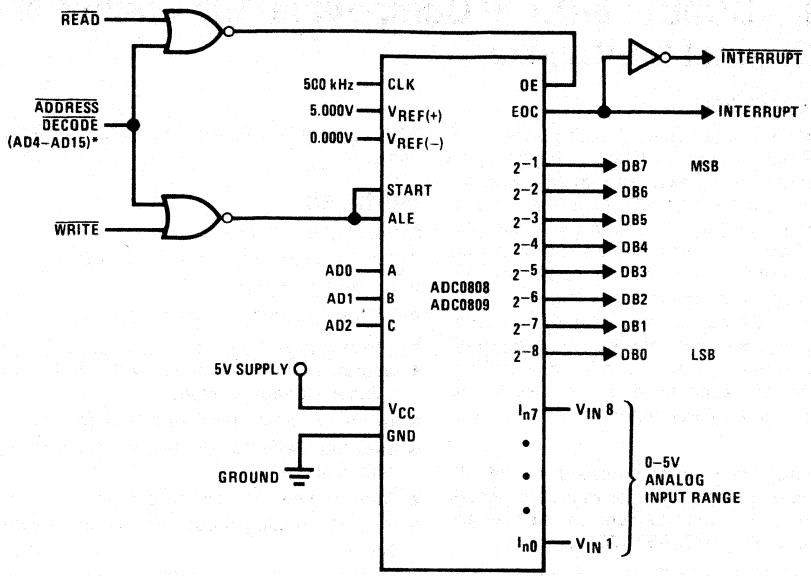
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6.*

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application



* Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA·ϕ2·R/W	VMA·ϕ2·$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	± 1/2 Bit Unadjusted	ADC0808CCN	ADC0808CCJ	ADC0808CJ
	± 1 Bit Unadjusted	ADC0809CCN		
Package Outline		N28A Molded DIP	J28A Hermetic DIP	J28A Hermetic DIP

National Semiconductor

ADC0816, ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

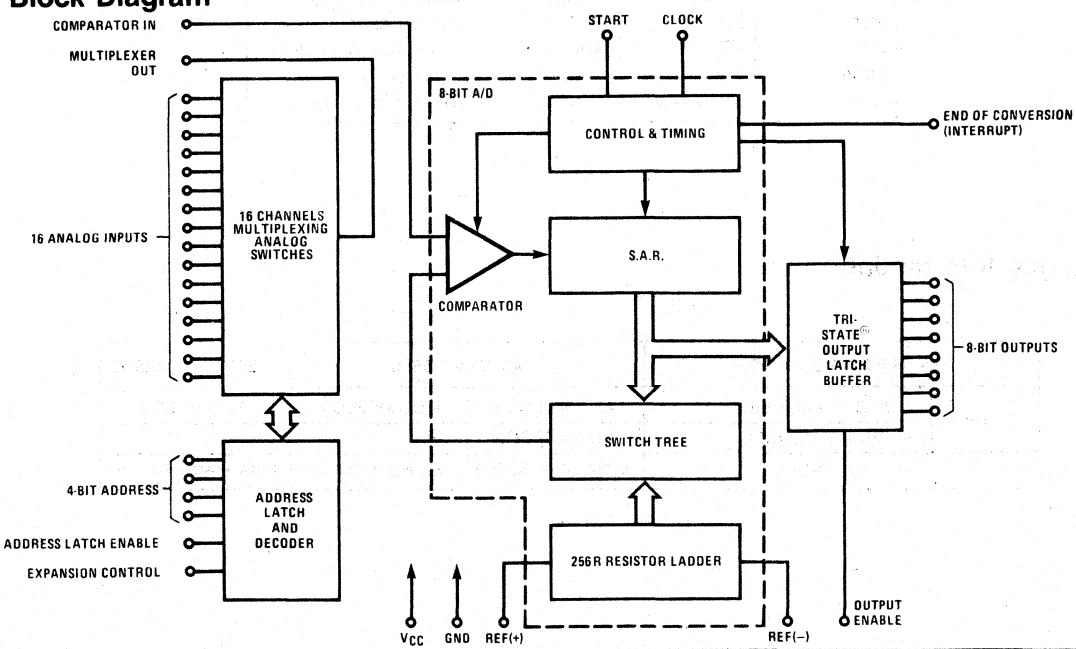
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet.

Features

- Resolution — 8-bits
- Total unadjusted error — ±1/2 LSB and ±1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	−0.3V to 15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0816CJ	−55°C ≤ T_A ≤ +125°C
ADC0816CCJ, ADC0816CCN, ADC0817CCN	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: V_{CC} = 5 V_{DC} = $V_{REF(+)}$, $V_{REF(-)}$ = GND, V_{IN} = $V_{COMPARATOR\ IN}$, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

Parameter		Conditions	Min	Typ	Max	Units
	ADC0816					
	Total Unadjusted Error	25°C			± 1/2	LSB
	(Note 5)	T_{MIN} to T_{MAX}			± 3/4	LSB
	ADC0817					
	Total Unadjusted Error	0°C to 70°C			± 1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			± 1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	4.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2 + 0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CJ 4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN 4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel)				
		T_A = 25°C, R_L = 10k		1.5	3	kΩ
		T_A = 85°C			6	kΩ
		T_A = 125°C			9	kΩ
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) R_L = 10k		75		Ω
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V,				
		T_A = 25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0,				
		T_A = 25°C	−200			nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CJ 4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN 4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA	V_{CC}-0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O = 1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	$V_O = V_{CC}$			3	μA
		V_O = 0	−3			μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)}$ = 5V, $V_{REF(-)}$ = GND, $t_r = t_f$ = 20 ns and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S = 0Ω *(Figure 5)*		1	2.5	μs
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L = 50 pF, R_L = 10k *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L = 10 pF, R_L = 10k *(Figure 8)*		125	250	ns
t_c	Conversion Time	f_c = 640 kHz, *(Figure 5)* (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2 μs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 7)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE				EXPANSION CONTROL
	D	C	B	A	
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs using the expansion control. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + 1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

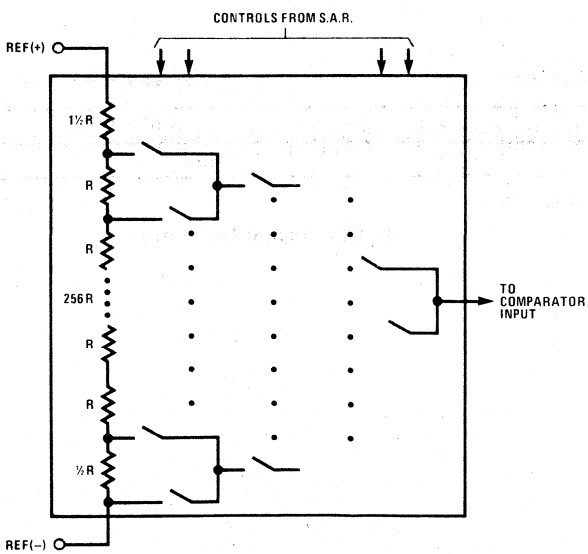


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179.

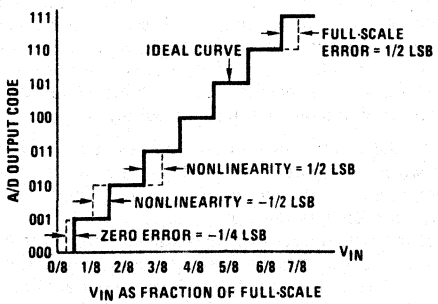


FIGURE 2. 3-Bit A/D Transfer Curve

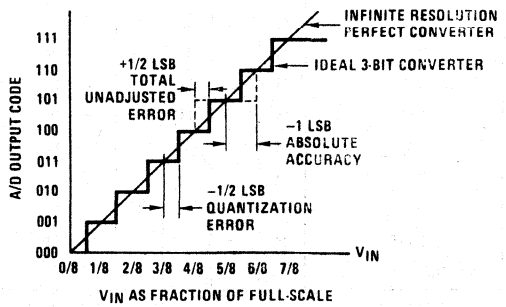


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

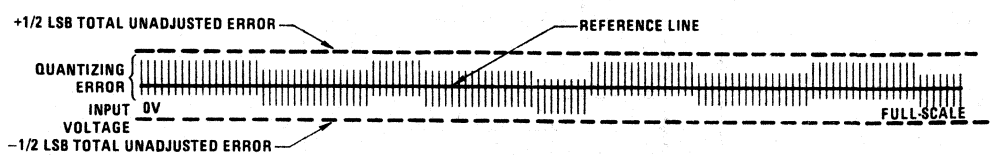
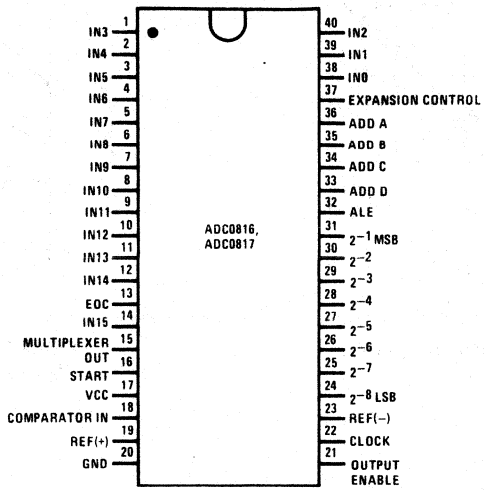


FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



TOP VIEW

Timing Diagram

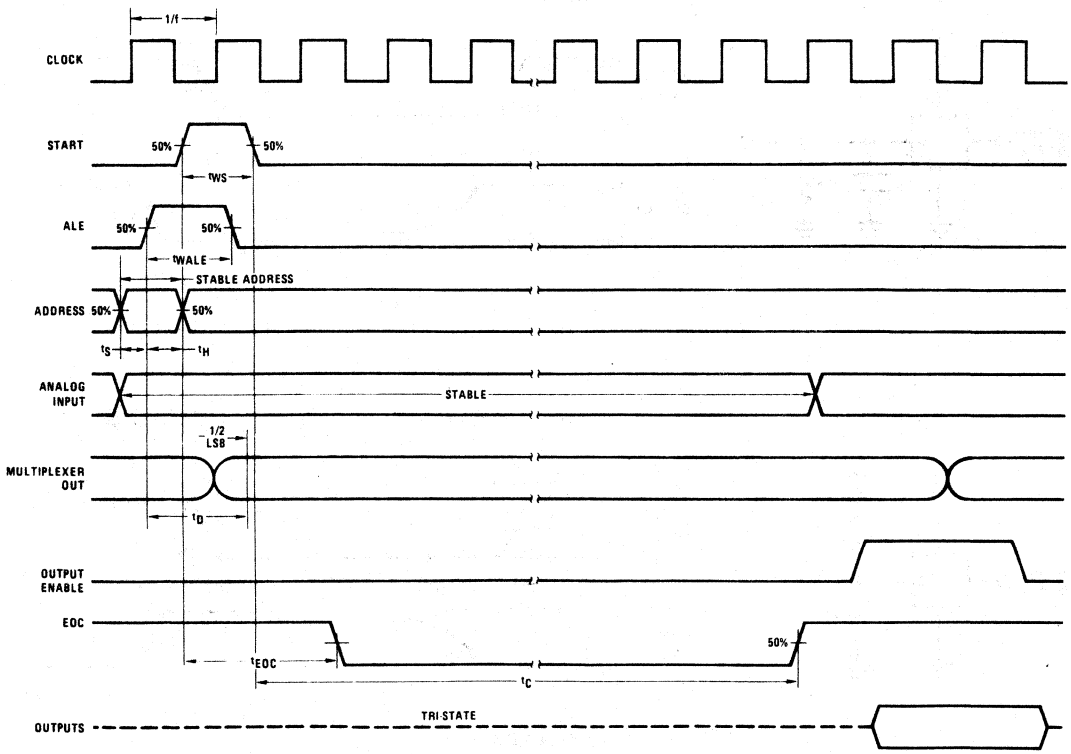


FIGURE 5

Typical Performance Characteristics

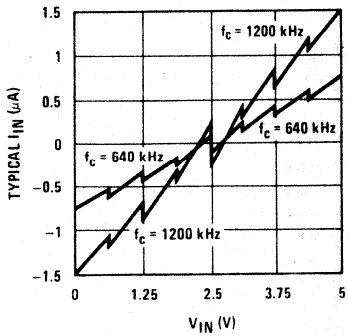


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

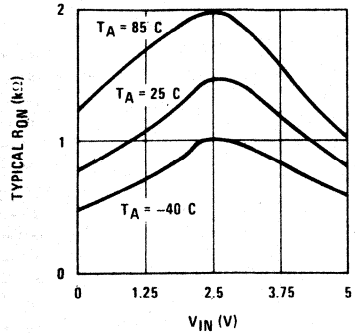


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

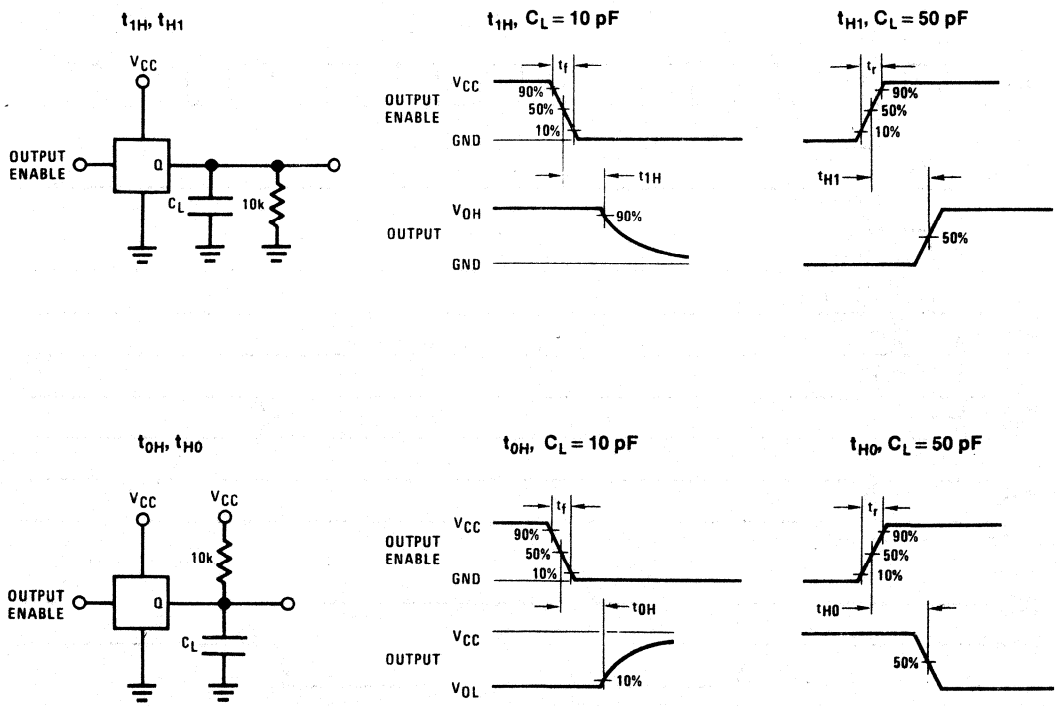


FIGURE 8

Applications Information

OPERATION

1.0 Ratiometric Conversion

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0816
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

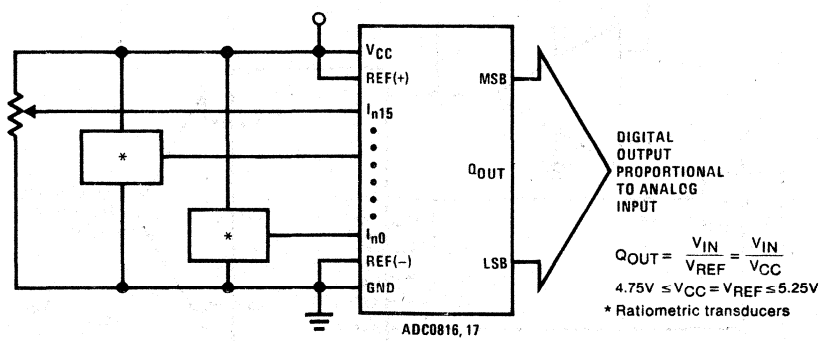


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB to be half the size of the LSB in a 5V reference system.

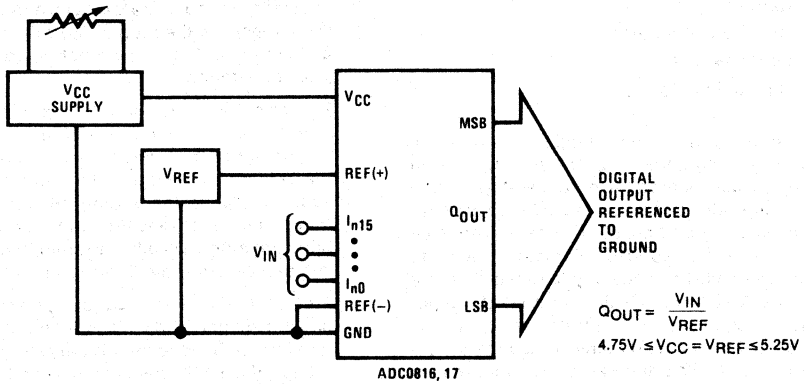


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

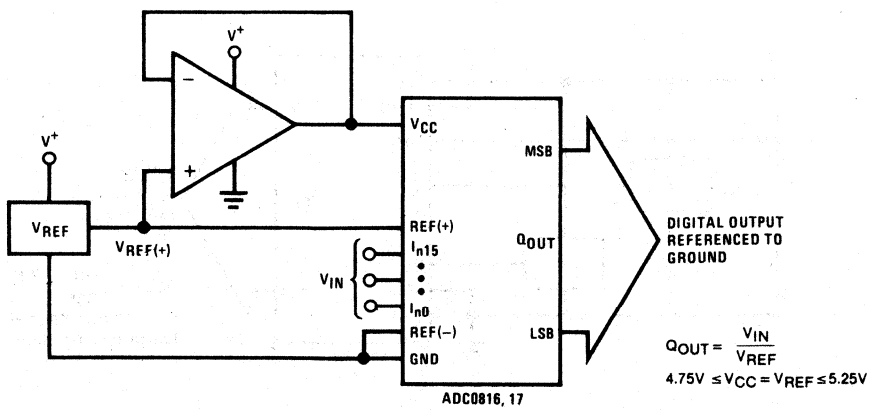


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

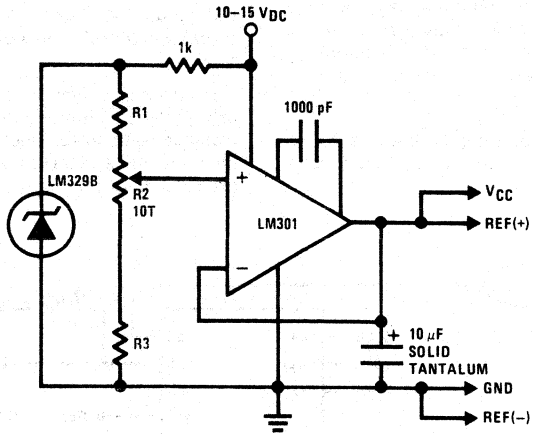


FIGURE 12. Typical Reference and Supply Circuit

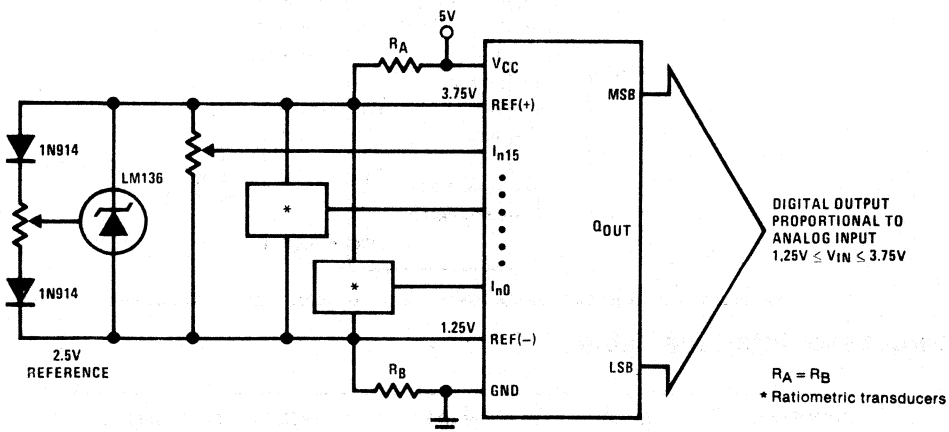


FIGURE 13. Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE}\right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256}\right] \pm V_{TUE}\right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(–)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

Applications Information (Continued)

4.0 Analog Comparator Inputs

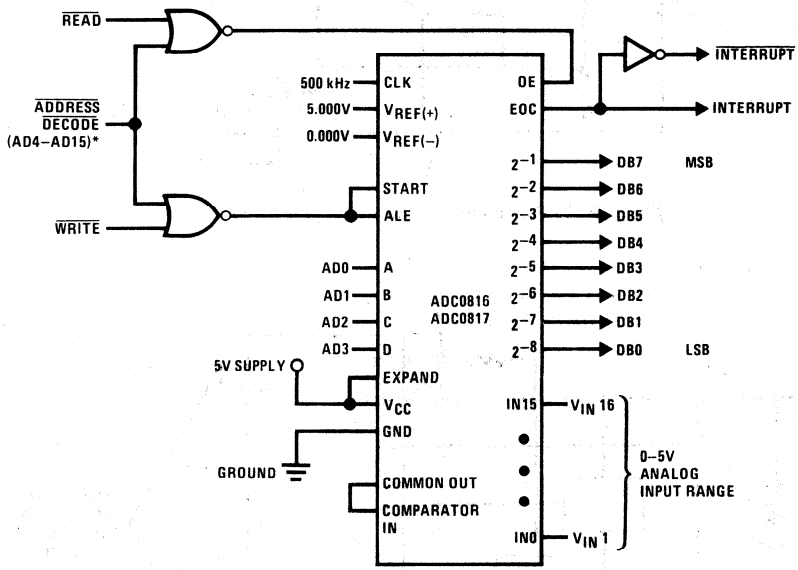
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6.*

If no filter capacitors are used at the analog or comparator inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application



* Address latches needed for 8085 and SC/MP interfacing the ADC0816, 17 to a microprocessor

Microprocessor Interface Table

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA·ϕ2·R/W	VMA·ϕ2·R/W	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	± 1/2 Bit Unadjusted	ADC0816CCN	ADC0816CCJ	ADC0816CJ
	± 1 Bit Unadjusted	ADC0817CCN		
Package Outline		N40A Molded DIP	J40A Hermetic DIP	J40A Hermetic DIP

National Semiconductor

ADC1210, ADC1211 12-Bit CMOS A/D Converters

General Description

The ADC1210, ADC1211 are low power, medium speed, 12-bit successive approximation, analog-to-digital converters. The devices are complete converters requiring only the application of a reference voltage and a clock for operation. Included within the device are the successive approximation logic, CMOS analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator.

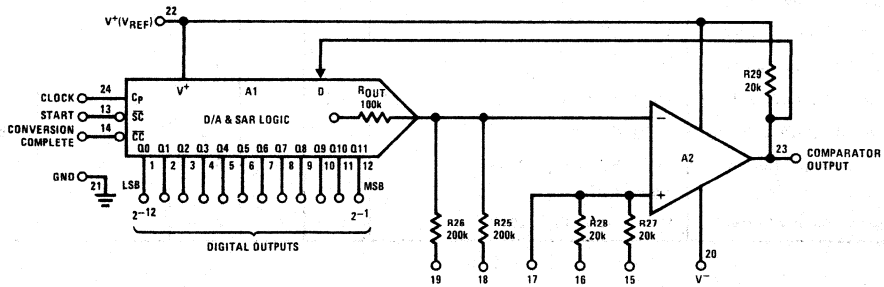
The ADC1210 offers 12-bit resolution and 12-bit accuracy, and the ADC1211 offers 12-bit resolution with 10-bit accuracy. The inverted binary outputs are directly compatible with CMOS logic. The ADC1210, ADC1211 will operate over a wide supply range, convert both bipolar and unipolar analog inputs, and operate in either a continuous conversion mode or logic-controlled START-STOP conversion mode. The devices are capable of making a 12-bit conversion in 100 μs typ, and can be connected to convert 10 bits in 30 μs.

Both devices are available in military and industrial temperature ranges.

Features

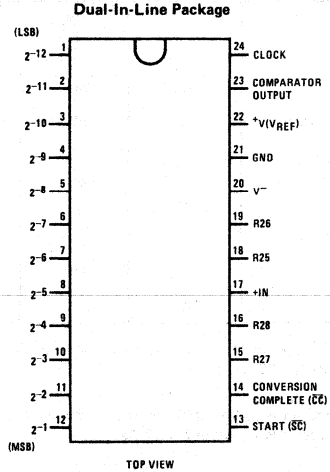
- 12-bit resolution
- ±1/2 LSB linearity
- Single +5V to ±15V supply range
- 100 μs 12-bit, 30 μs 10-bit conversion rate
- CMOS compatible outputs
- Bipolar or unipolar analog inputs
- 200 kΩ analog input impedance
- Low cost

Block Diagram



Connection Diagram

Dual-In-Line Package



Order Number ADC1210HCD, ADC1211HCD, ADC1210HD or ADC1211HD
See NS Package D24D

Absolute Maximum Ratings

Maximum Reference Supply Voltage (V^+)	16V	Power Dissipation	See Curves
Maximum Negative Supply Voltage (V^-)	−20V	Operating Temperature Range	
Voltage At Any Logic Pin	$V^+ + 0.3V$	ADC1210HD, ADC1211HD	−55°C to +125°C
Analog Input Voltage	±15V	ADC1210HCD, ADC1211HCD	−25°C to + 85°C
Maximum Digital Output Current	±10 mA	Storage Temperature Range	−65°C to +150°C
Maximum Comparator Output Current	50 mA	Lead Temperature (Soldering, 10 seconds)	300°C
Comparator Output Short-Circuit Duration	5 Seconds		

DC Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	ADC1210			ADC1211			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		12			12			Bits
Linearity Error	(Note 3)							
	f_{CLK} = 65 kHz, T_A = 25°C			±0.0122			±0.0488	% FS
	f_{CLK} = 65 kHz			±0.0244				% FS
Full Scale Error	T_A = 25°C, Unadjusted			0.1			0.25	% FS
Zero Scale Error	T_A = 25°C, Unadjusted			0.1			0.25	% FS
Quantization Error				±1/2			±1/2	LSB
Input Resistor Values	R27, R28		20			20		kΩ
Input Resistor Values	R25, R26		200			200		kΩ
Input Resistor Ratios	R25/R26, R27/R28			0.1			0.1	%
Logic "1" Input Voltage		8			8			V
Logic "0" Input Voltage				2			2	V
Logic "1" Input Current	V_{IN} = 10.24V			1			1	μA
Logic "0" Input Current	V_{IN} = 0V			−1			−1	μA
Logic "1" Output Voltage	$I_{OUT} \leq -1$ μA	9.2			9.2			V
Logic "0" Output Voltage	$I_{OUT} \leq 1$ μA			0.5			0.5	V
Positive Supply Current	V^+ = 15V, f_{CLK} = 65 kHz, T_A = 25°C		5	8		5	8	mA
Negative Supply Current	V^- = −15V, T_A = 25°C		4	6		4	6	mA

AC Electrical Characteristics T_A = 25°C, (Notes 1 and 2)

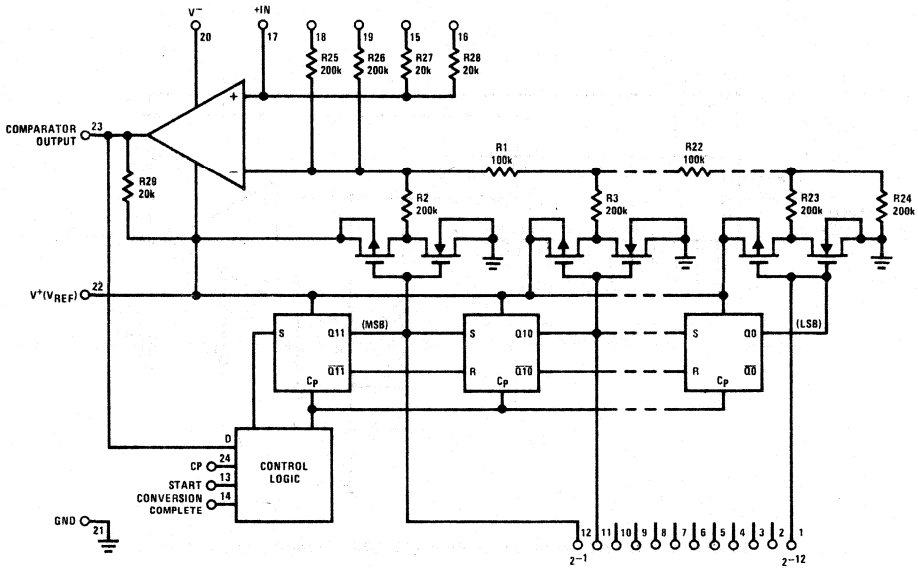
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time			100	200	μs
Maximum Clock Frequency			130	65	kHz
Clock Pulse Width		100	50		ns
Propagation Delay From Clock to Data Output (Q0 to Q11)	$t_r \leq t_f \leq 10$ ns		60	150	ns
Propagation Delay From Clock to Conversion Complete	$t_r \leq t_f \leq 10$ ns		60	150	ns
Clock Rise and Fall Time				5	μs
Input Capacitance			10		pF
Start Conversion Set-Up Time		30			ns

Note 1: Unless otherwise noted, these specifications apply for V^+ = 10.240V, V^- = −15V, over the temperature range −55°C to +125°C for the ADC1210HD, ADC1211HD, and −25°C to +85°C for the ADC1210HCD, ADC1211HCD.

Note 2: All typical values are for T_A = 25°C.

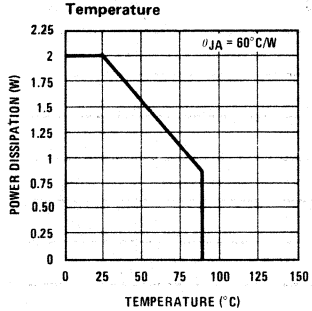
Note 3: Unless otherwise noted, this specification applies over the temperature range −25°C to +85°C. Provision is made to adjust zero scale error to 0V and full-scale to 10.2375V during testing. Standard linearity test circuit is shown in *Figure 5a.*

Schematic Diagram

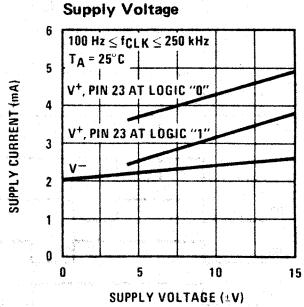


Note: 3 bits shown for clarity

Power Dissipation vs Temperature



Supply Current vs Supply Voltage



1.0 THEORY OF OPERATION

The ADC1210, ADC1211 are successive approximation analog-to-digital converters, i.e., the conversion takes place 1 bit at a time by comparing the output of the internal D/A to the (unknown) input voltage. The START input (pin 13), when taken low, causes the register to reset synchronously on the next CLOCK low-to-high transition. The MSB, Q11 is set to the low state, and the remaining bits, Q0 through Q10, will be set to the high state. The register will remain in this state until the $\overline{SC}$ input is taken high. When START goes high, the conversion will begin on the low-to-high transition of the CLOCK pulse. Q11 will then assume the state of pin 23. If pin 23 is high, Q11 will be high; if pin 23 is low, Q11 will remain low. At the same time, the next bit, Q10 is set low. All remaining bits, Q0–Q9 will remain unchanged (high). This process will continue until the LSB (Q0) is found. When the conversion process is completed, it is indicated by CONVERSION COMPLETE ($\overline{CC}$) (pin 14) going low. The logic levels at the data output pins (pins 1–12) are the complemented-binary representation of the converted analog signal with Q11 being the MSB and Q0 being the LSB. The register will remain in the above state until the $\overline{SC}$ is again taken low.

An application example is shown in *Figure 1*. In this case, a 0 to −10.2375V input is being converted using the ADC1210 with V^+ = 10.240V, V^- = −15V. *Figure 1b* is the timing diagram for full scale input. *Figure 1c* is the timing diagram for zero scale input, *Figure 1d* is the timing diagram for −3.4125V input (010101010101 = output).

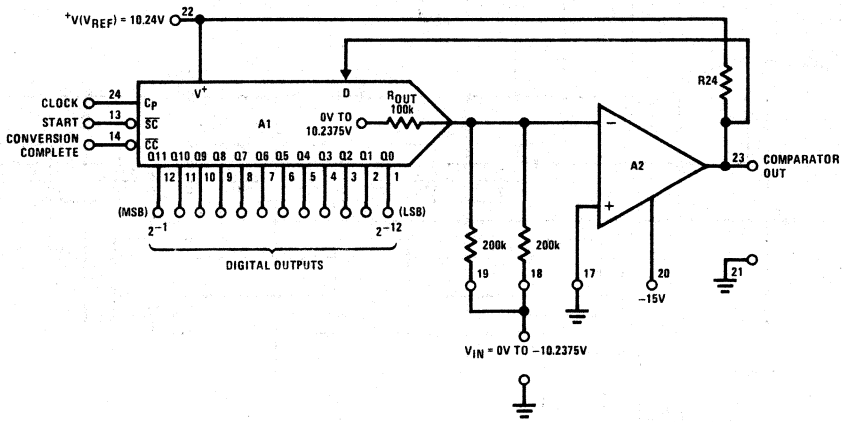


FIGURE 1a. ADC1210 Connected for 0V to −10.2375V (Natural Binary Output)

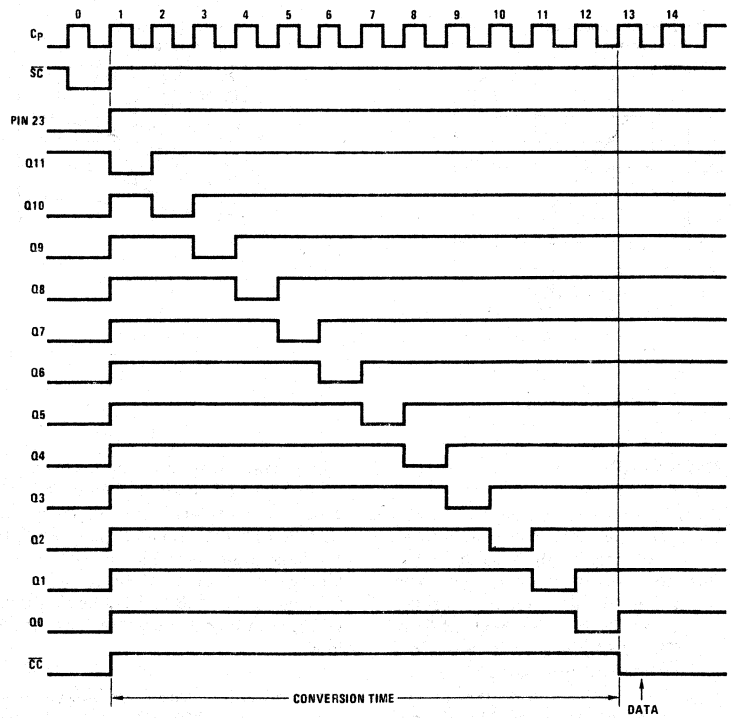


FIGURE 1b. Timing Diagram for V_{IN} = Full Scale Input

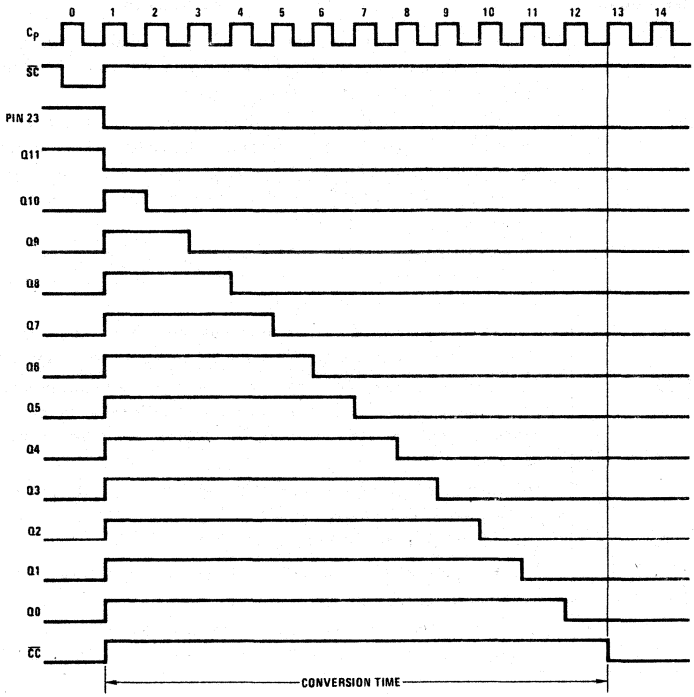


FIGURE 1c. Timing Diagram for V_{IN} = Zero Scale

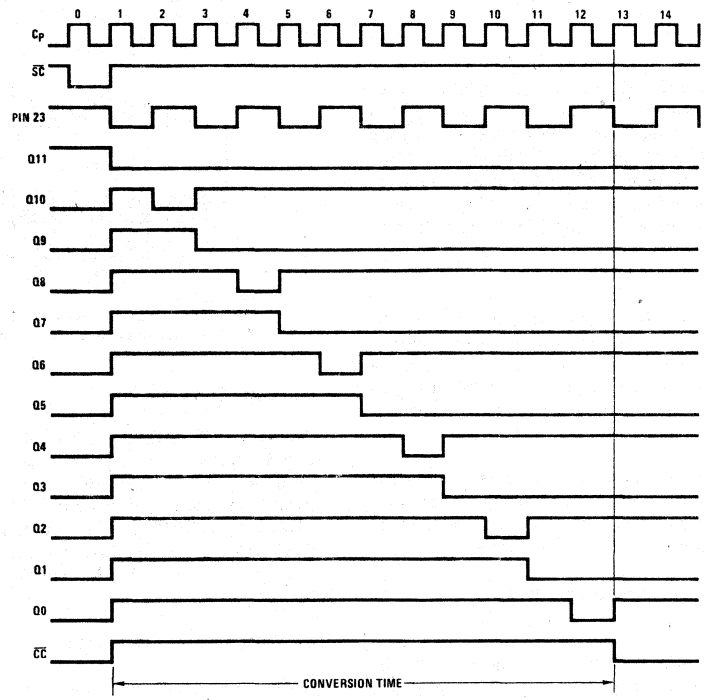


FIGURE 1d. Timing Diagram for V_{IN} = –3.4125V (010101010101)

TABLE I. Pin Assignments and Explanations

PIN NUMBER	MNEMONIC	FUNCTION
1–12	Q11–Q0	Digital (data) output pins. This information is a parallel 12-bit complemented binary representation of the converted analog signal. All data is valid when "Conversion Complete" goes low. Logic levels are ground and V^+.
13	$\overline{SC}$	Start Conversion is a logic input which causes synchronous reset of the successive approximation register and initiates conversion. Logic levels are ground and V^+.
14	$\overline{CC}$	"Conversion Complete" is a digital output signal which indicates the status of the converter. When $\overline{CC}$ is high, conversion is taking place, when low conversion is completed. Logic levels are ground and V^+.
15, 16	R27, R28	R27 and R28 are two application resistors connected to the comparator non-inverting input. The resistors may be used in various modes of operation. Their nominal values are 20 kΩ each. See Applications section.
17	+IN	Non-inverting input of the analog comparator. This node is used in various configurations and for compensation of the loop. See Applications section.
18, 19	R25, R26	R25 and R26 are two application resistors that are tied internally to the inverting input of the comparator. Their nominal values are 200 kΩ each. See Applications section. The R-2R ladder network will have the same temperature coefficient as these resistors.
20	V^-	Negative supply voltage for bias of the analog comparator. Optionally may be grounded or operated with voltages to −20V.
21	GND	Ground for both digital and analog signals.
22	V^+(VREF)	V^+ sets both maximum full scale and input and output logic levels.
23	CO	Comparator output.
24	Cp	Clock is an input which causes the successive approximation (shift) register to advance through the conversion sequence. Logic levels are ground and V^+.

2.0 APPLICATIONS

2.1 Power Supply Considerations and Decoupling

Pin 22 is both the positive supply and voltage reference input to the ADC1210, ADC1211. The magnitude of V^+ determines the input logic "1" threshold and the output voltage from the CMOS SAR. The device will operate over a range of V^+ from 5V to 15V. However, in order to preserve 12-bit accuracy, V^+ should be well regulated (0.01%) and isolated from external switching transients. It is therefore recommended that pin 22 be decoupled with a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic disc capacitor.

The V^- supply (pin 20) provides negative bias for the FET comparator. Although pin 20 may be grounded in some applications, it must be at least 2V more negative than the most negative analog input signal. When a negative supply is used, pin 20 should also be bypassed with 4.7 μF in parallel with 0.1 μF.

Grounding and circuit layout are extremely important in preserving 12-bit accuracy. The user is advised to employ separate digital and analog returns, and to make these PC board traces as "heavy" as practical.

2.2 Short Cycle for Improved Conversion Time (Figure 2)

The ADC1210, ADC1211 counting sequence may be truncated to decrease conversion time. For example, when using the ADC1211, 2 clock intervals may be "saved" if 10-bit conversion accuracy is taking place. The Q2 output should be "OR'd" with CONVERSION COMPLETE ($\overline{CC}$) in order to ensure that the register does not lock-up upon power turn-on.

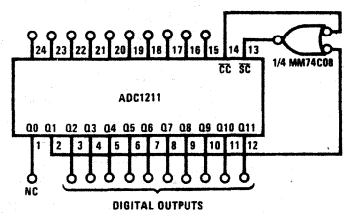


FIGURE 2. Short Cycling the ADC1211 to Improve 10-Bit Conversion Time (Continuous Conversion)

2.3 Logic Compatibility

The ADC1210, ADC1211 is intended to interface with CMOS logic levels: i.e., the logic inputs and outputs are directly compatible with series 54C/74C and CD4000 family of logic components. The outputs of the ADC1210, ADC1211 will not drive LPTTL, TTL or PMOS logic directly without degrading accuracy. Various recommended interface techniques are shown in *Figures 3 and 4.*

2.4 Operating Configurations

Several recommended operating configurations are shown in *Figure 5.*

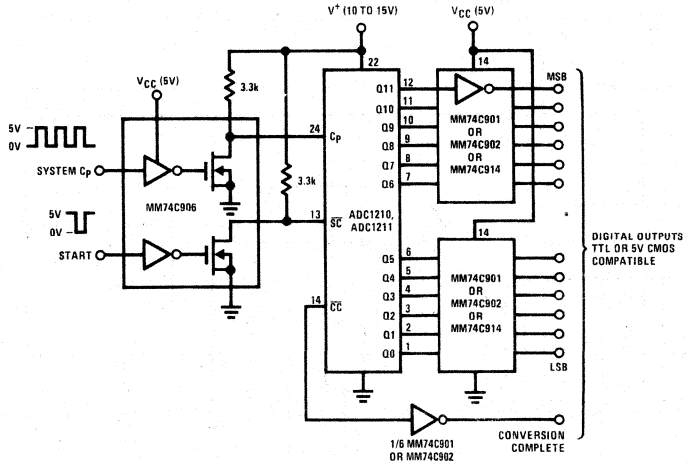


FIGURE 3. Interfacing an ADC1210, ADC1211 Running on $V^+ > V_{CC}$. Example: $V^+ = 10.24V$, System $V_{CC} = 5V$

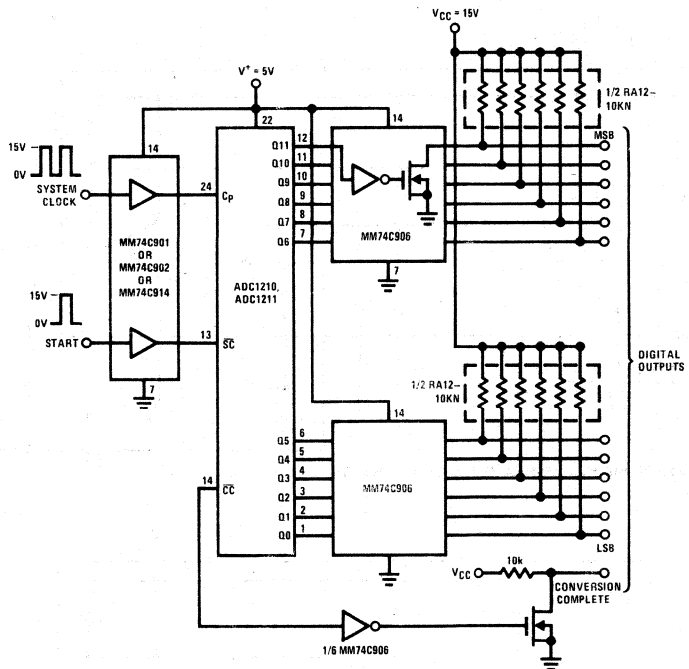


FIGURE 4. Interfacing an ADC1210, ADC1211 Running on $V^+ < V_{CC}$. Example: $V^+ = 5V$, $V_{CC} = 15V$

2.5 Offset and Full Scale Adjust

A variety of techniques may be employed to adjust Offset and Full Scale on the ADC1210, ADC1211. A straight-forward Full Scale Adjust is to incrementally vary V^+ (V_{REF}) to match the analog input voltage. A recommended technique is shown in *Figure 6*. An LM199 and low drift op amp (e.g., the LH0044) are used to provide the precision reference. The ADC1210, ADC1211 is put in the continuous convert mode by shorting pins 13 and 14. An analog voltage equal to V_{REF} minus 1 1/2 LSB (10.23625V) is applied to pins 18 and 19, and R1 is adjusted until the LSB flickers equally between logic "1" and logic "0" (all other outputs must be stable logic "0"). Offset Null is accomplished by then applying an analog input voltage equal to 1/2 LSB at pins 18 and 19. R2 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other bits are stable). In the circuit of *Figure 6*, the ADC1210, ADC1211 is configured for Complementary Binary logic and the values shown are for $V^+ = 10.240V$, $V_{FS} = 10.2375V$, LSB = 2.5 mV.

An alternate technique is shown in *Figure 7*. In this instance, an LH0071 is used to provide the reference voltage. An analog input voltage equal to V_{REF} minus 1 1/2 LSB (10.23625V) is applied to pins 18 and 19.

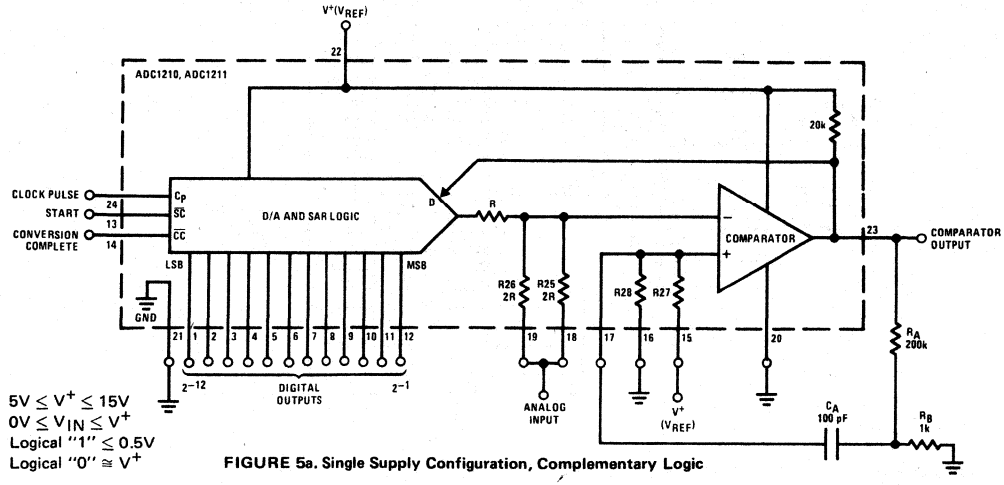


FIGURE 5a. Single Supply Configuration, Complementary Logic

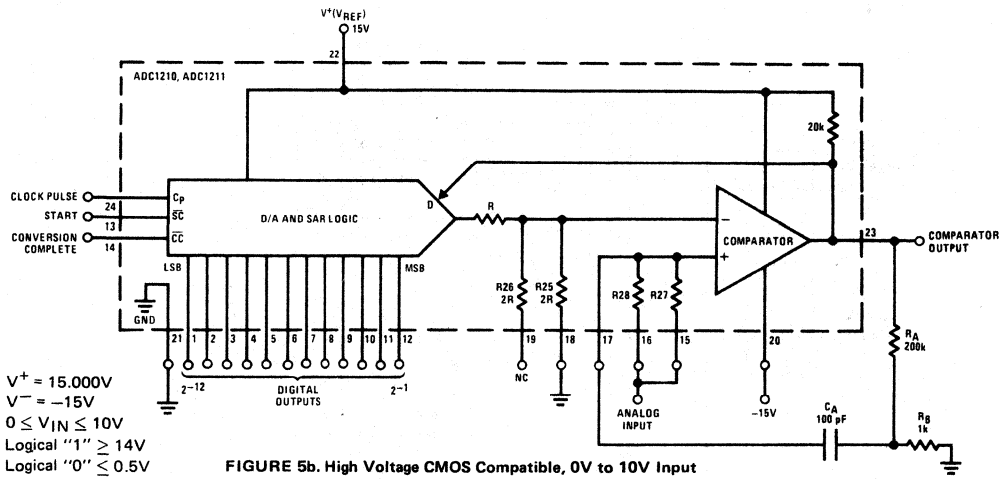


FIGURE 5b. High Voltage CMOS Compatible, 0V to 10V Input

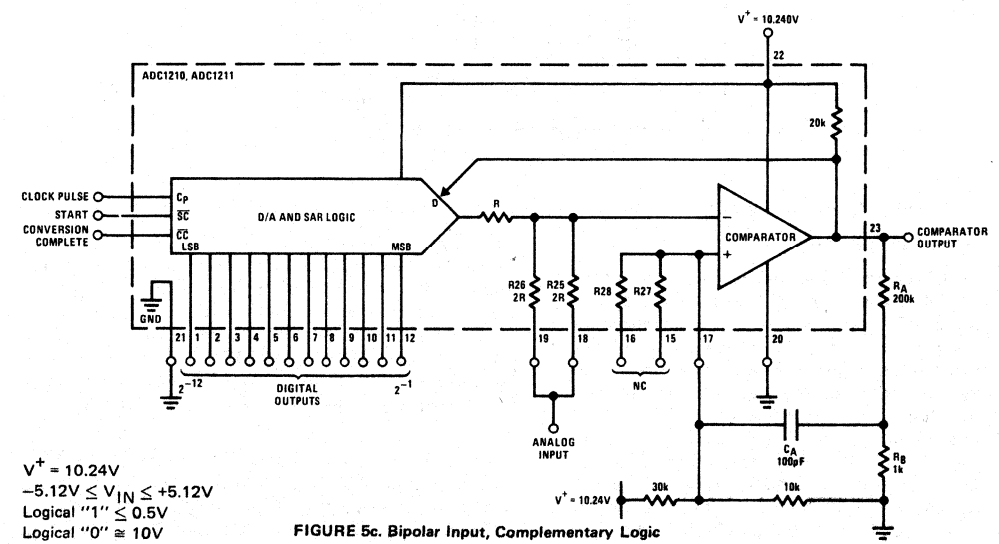


FIGURE 5c. Bipolar Input, Complementary Logic

Applications Information (Continued)

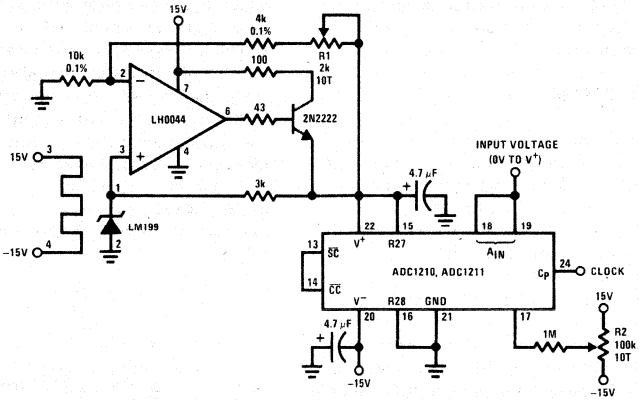


FIGURE 6. Offset and Full Scale Adjustment for Complementary Binary

R1 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other outputs must be a stable logic "0"). For Offset Null, an analog voltage equal to 1/2 LSB (1.25 mV) is then applied to pins 18 and 19, and R2, is adjusted until the LSB output flickers equally between logic "1" and "0".

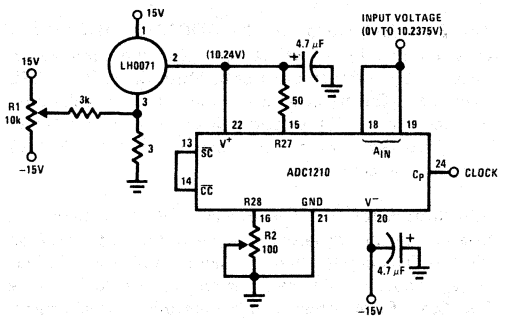


FIGURE 7. Offset and Full-Scale Adjustment Technique Using LH0071

In both techniques shown, adjusting the Full-Scale first and then Offset minimizes adjustment interaction. At least one iteration is recommended as a self-check.

2.6 Start Pulse Considerations

To assure reliable conversion accuracy, the $\overline{\text{START}}$ ($\overline{\text{SC}}$) pulse applied to pin 13 of the ADC1210 should be synchronized to the conversion clock. One simple way to do that is the circuit shown in *Figure 8.* Note that once a conversion cycle is initiated, the $\overline{\text{START}}$ signal cannot effect the conversion operation until it is completed.

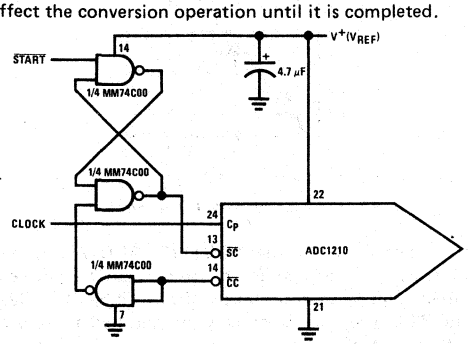


FIGURE 8. Synchronizing the $\overline{\text{START}}$ Pulse

The circuit insures that in no case can the ADC1210 make an error in the Most Significant Bit (MSB) decision. Without the circuit, it is possible for energy from the trailing edge of an asynchronous $\overline{\text{START}}$ pulse to be coupled into the ADC1210's comparator. If the analog input is near half-scale, the charge injected can force an error in the MSB decision. The circuit allows one clock period for this energy to dissipate before the decision is recorded.

2.7 ADC1210 Conversion at 26 µs

The ADC1210 can run at 500 kHz clock frequency, or 12-bit conversion time of 26 µs *(Figure 9)*. The comparator output is clamped low until the successive approximation register (SAR) is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions, eliminating the need for the AC hysteresis circuit above clock frequency of 65 kHz that is recommended.

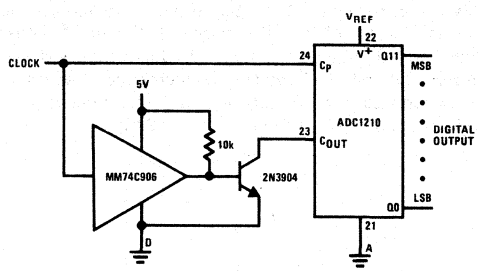


FIGURE 9. Conversion at 26 µs

A complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The same signal is buffered and inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in normal working order. The last half cycle of the clock unclamps the comparator output. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propogation delay such that the comparator output data is held long enough to resolve any internal logic set-up time requirements.

The 500 kHz clock implies that the absolute min[illegible]n amount of time for the comparator output is *uncla[illegible]* is 1 μs. Therefore, if the clock is not 50% duty cycle, 1 μs requirement must be observed.

3.0 DEFINITION OF TERMS

Resolution: The Resolution of an A/D is an expression of the smallest change in input which will increment (or decrement) the output from one code to the next adjacent code. It is defined in number of bits, or 1 part in 2^n. The ADC1210 and ADC1211 have a resolution of 12 bits or 1 part in 4,096 (0.0244%).

Quantization Uncertainty: Quantization Uncertainty is a direct consequence of the resolution of the converter. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an inherent conversion error even for a perfect A/D. As an example, the transfer characteristic of a perfect 3-bit A/D is shown in *Figure 10.*

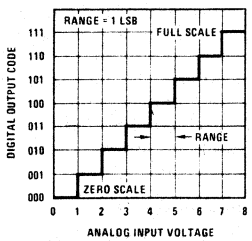


FIGURE 10. Quantization Uncertainty of a Perfect 3-Bit A/D

As can be seen, all input voltages between 0V and 1V are represented by an output code of 000. All input voltages between 1V and 2V are represented by an output code of 001, etc. If the midpoint of the range is assumed to be the nominal value (e.g., 0.5V), there is an Uncertainty of ±1/2 LSB. It is common practice to offset the converter 1/2 LSB in order to reduce the Uncertainty to ±1/2 LSB is shown in *Figure 11*, rather than +1, −0 shown in *Figure 10*. Quantization Uncertainty can only be reduced by increasing Resolution. It is expressed as ±1/2 LSB or as an error percentage of full scale (±0.0122% FS for the ADC1210).

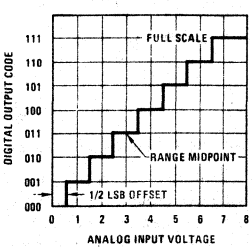


FIGURE 11. Transfer Characteristic Offset 1/2 LSB to Minimize Quantizing Uncertainty

Linearity Error: Linearity Error is the maximum deviation from a straight line passing through the end points of the A/D transfer characteristic. It is measured after calibrating Zero and Full Scale Error. The Linearity Error of the ADC1210 is guaranteed to be less than ±1/2 LSB or ±0.0122% of FS and ±0.0488% of FS for the AD1211. Linearity is a performance characteristic intrinsic to the device and cannot be externally adjusted.

[illegible] Scale Error (or Offset): Zero Scale Error is a [illegible]asure of the difference between the output of an ideal and the actual A/D for zero input voltage. As shown in *Figure 12*, the effect of Zero Scale Error is to shift the transfer characteristic to the right or left along the abscissa. Any voltage more negative than the LSB transition gives an output code of 000. In practice, therefore, the voltage at which the 000 to 001 transition takes place is ascertained, this input voltage's departure from the ideal value is defined as the Zero Scale Error (Offset) and is expressed as a percentage of FS. In the example of *Figure 12*, the offset is 2 LSB's or 0.286% of FS.

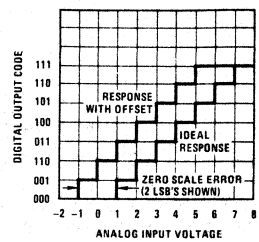


FIGURE 12. A/D Transfer Characteristic with Offset

The Zero Scale Error of the ADC1210, ADC1211 is caused primarily by offset voltage in the comparator. Because it is common practice to offset the A/D 1/2 LSB to minimize Quantization Error, the offsetting techniques described in the Applications Section may be used to null Zero Scale Error and accomplish the 1/2 LSB offset at the same time.

Full Scale Error (or Gain Error): Full Scale Error is a measure of the difference between the output of an ideal A/D converter and the actual A/D for an input voltage equal to full scale. As shown in *Figure 13*, the Full Scale Error effect is to rotate the transfer characteristic angularly about the origin. Any voltage more positive than the Full Scale transition gives an output code of 111. In practice, therefore, the voltage at which the transition from 111 to 110 occurs is ascertained. The input voltage's departure from the ideal value is defined as Full Scale Error and is expressed as a percentage of FS. In the example of *Figure 13*, Full Scale Error is 1 1/2 LSB's, or 0.214% of FS.

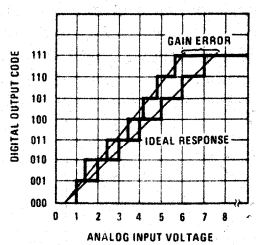


FIGURE 13. Full Scale (Gain Error)

Full Scale Error of the ADC1210, ADC1211 is due primarily to mismatch in the R-2R ladder equivalent output impedance and input resistors R25, R26, R27, and R28. The gain error may be adjusted to zero as outlined in section 2.5.

Monotonicity and Missing Codes: Monotonicity is a property of a D/A which requires an increasing or constant output voltage for an increasing digital input code. Monotonicity of a D/A converter does not, in itself, guarantee that an A/D built with that D/A will not have missing codes. However, the ADC1210 and ADC1211 are guaranteed to have no missing codes.

Conversion Time: The ADC1210, ADC1211 are successive approximation A/D converters requiring 13 clock intervals for a conversion to specified accuracy for the ADC1210 and 11 clocks for the ADC1211. There is a trade-off between accuracy and clock frequency due to settling time of the ladder and propagation delay through the comparator. By modifying the hysteresis network around the comparator, conversions with 10-bit accuracy can be made in 30 μs. Replace R_A, R_B and C_A in *Figure 5* with a 10 MΩ resistor between pin 23 (Comparator Output) and pin 17 (+ IN), and increase the clock rate to 366 kHz.

In order to prevent errors during conversion, the analog input voltage should not be allowed to change by more than ±1/2 LSB. This places a maximum slew rate of 12.5 μV/μs on the analog input voltage. The usual solution to this restriction is to place a Sample and Hold in front of the A/D.

National Semiconductor

ADC3511
3 1/2-Digit Microprocessor Compatible A/D Converter
ADC3711
3 3/4-Digit Microprocessor Compatible A/D Converter

General Description

The ADC3511 and ADC3711 (MM74C937-1, MM74C938-1) monolithic A/D converter circuits are manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and indicated on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available.

The ADC3511 and ADC3711 have been designed to provide addressed BCD data and are intended for use with microprocessors and other digital systems. BCD digits are selected on demand via 2 Digit Select (D0, D1) inputs. Digit Select inputs are latched by a low-to-high transition on the Digit Latch Enable (DLE) input and will remain latched as long as DLE remains high. A start conversion input and a conversion complete output are included on both the ADC3511 and the ADC3711.

Features

- Operates from single 5V supply
- ADC3511 converts 0 to ±1999 counts
- ADC3711 converts 0 to ±3999 counts
- Addressed BCD outputs
- No external precision components necessary
- Easily interfaced to microprocessors or other digital systems
- Medium speed—200 ms/conversion
- TTL compatible
- Internal clock set with RC network or driven externally
- Overflow indicated by hex "EEEE" output reading as well as an overflow output

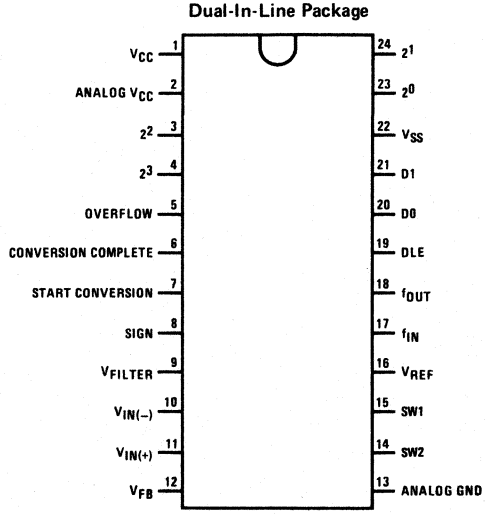
Applications

- Low cost analog-to-digital converter
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram

Order Number ADC3511CCN or ADC3711CCN
See NS Package N24A

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range (T_A)	−40°C to +85°C
Package Dissipation at T_A = 25°C	500 mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics ADC3511CC, ADC3711CC

4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage (Except f_{IN})		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage (Except f_{IN})				1.5	V
$V_{IN(1)}$	Logical "1" Input Voltage (f_{IN})		V_{CC}−0.6			V
$V_{IN(0)}$	Logical "0" Input Voltage (f_{IN})				0.6	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Except 2^0, 2^1, 2^2, 2^3)	I_O = 360μA	V_{CC}−0.4			V
$V_{OUT(1)}$	Logical "1" Output Voltage (2^0, 2^1, 2^2, 2^3)	I_O = 360μA	V_{CC}−1.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
$I_{IN(1)}$	Logical "1" Input Current (SC, DLE, D0, D1)	V_{IN} = V_{CC}		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (SC, DLE, D0, D1)	V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	All Outputs Open		0.5	5.0	mA

AC Electrical Characteristics ADC3511CC, ADC3711CC

V_{CC} = 5V; T_A = 25°C; C_L = 50 pF; t_r = t_f = 20 ns; unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
f_{OSC}	Oscillator Frequency			0.6/RC		Hz
f_{IN}	Clock Frequency		100		640	kHz
f_{CONV}	Conversion Rate	ADC3511CC		f_{IN}/64,512		conversions/sec
		ADC3711CC		f_{IN}/129,024		conversions/sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns
t_{pd0}, t_{pd1}	Propagation Delay D0, D1, to 2^0, 2^1, 2^2, 2^3	DLE = 0V		2.0	5.0	μs
t_{pd0}, t_{pd1}	Propagation Delay DLE to 2^0, 2^1, 2^2, 2^3			2.0	5.0	μs
t_{SET-UP}	Set-Up Time D0, D1, to DLE	t_{HOLD} = 0 ns		100	200	ns
t_{PWDLE}	Minimum Pulse Width Digit Latch Enable (Low)			100	200	ns

Converter Characteristics

ADC3511CC, ADC3711CC $4.75V \leq V_{CC} \leq 5.25V$; $-40°C \leq T_A \leq +85°C$, f_C = 5 conv./sec (ADC3511CC); 2.5 conv./sec (ADC3711CC); unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
	Non-Linearity	V_{IN} = 0–2V Full Scale V_{IN} = 0–200 mV Full Scale	–0.05	±0.025	+0.05	% of Full-Scale (Note 3)
	Quantization Error		–1		+0	Counts
	Offset Error	V_{IN} = 0V	–0.5	+1.0	+3.0	mV (Note 4)
	Rollover Error		–0		+0	Counts
$V_{IN}+$, $V_{IN}-$	Analog Input Current	T_A = 25°C	–5	±1	+5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

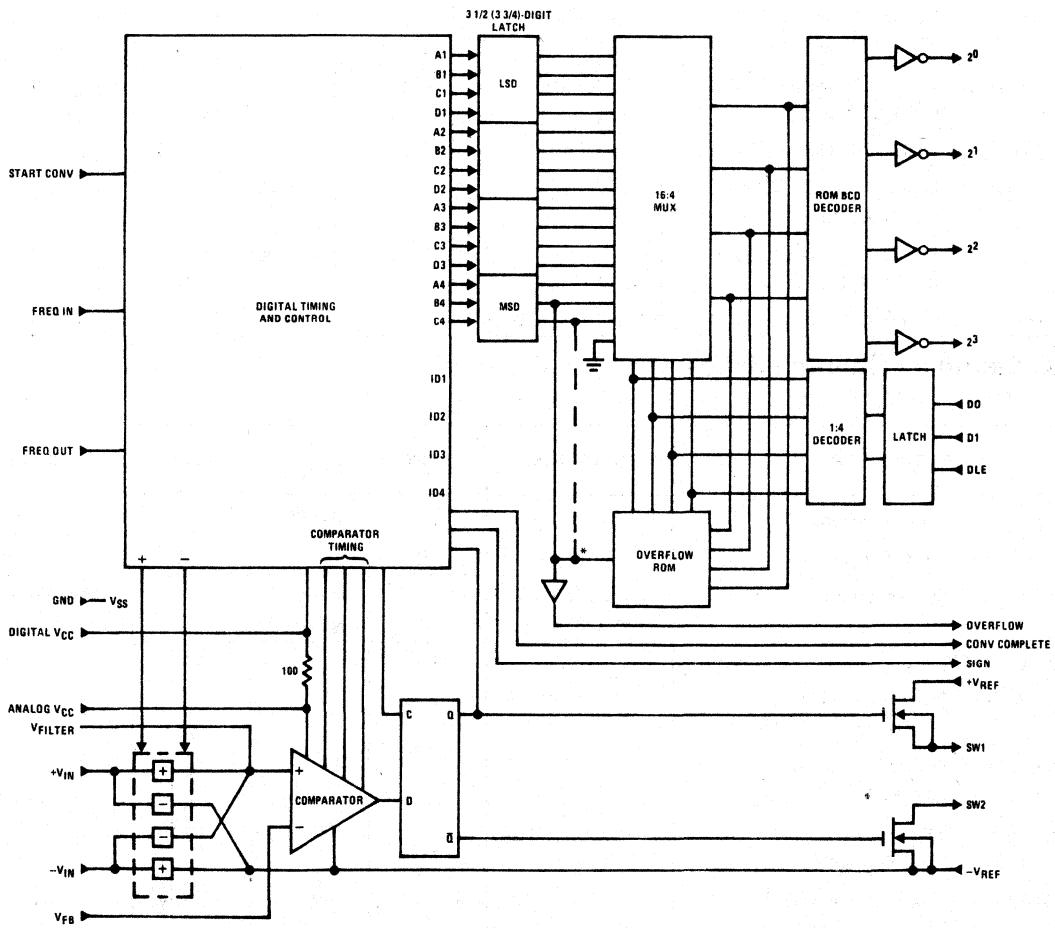
Note 2: All typicals are given for T_A = 25°C.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore 0.025% of full-scale = 1/2 count and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 count.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

Block Diagram

ADC3511 3 1/2-Digit A/D (*ADC3711 3 3/4-Digit A/D)



Applications Information

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure 1.* The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

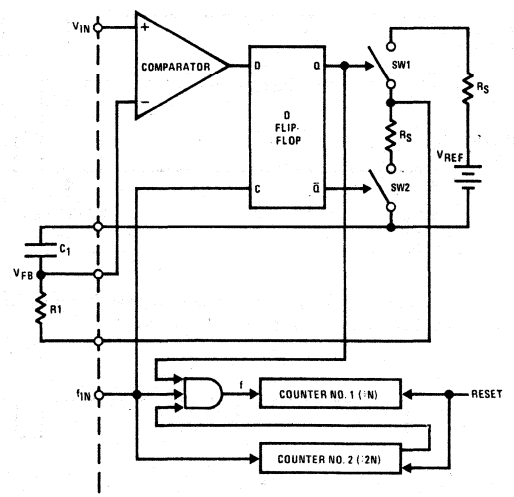
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{(count)} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.

For the ADC3711 N = 4000.



$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in counter no. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE 1. Analog Loop Schematic Pulse Modulation A/D Converter

Applications Information (Continued)

GENERAL INFORMATION

The timing diagram, shown in *Figure 2,* gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the digit latches are updated at a rate equal to 64,512 x $1/f_{IN}$ for the ADC3511, or 129,024 for the ADC3711.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the digit latches. This information will remain in the digit latches until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 64 x $1/f_{IN}$ on the ADC3511, or 128 x $1/f_{IN}$ on the ADC3711.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADC3511 and ADC3711 are always continuously converting the analog voltage present at their inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the digit latches.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3,* the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 x $1/f_{IN}$ (129,024 x $1/f_{IN}$ for the ADC3711) and the minimum time is 256 x $1/f_{IN}$ (512 x $1/f_{IN}$ for the ADC3711).

SYSTEM DESIGN CONSIDERATIONS

The ADC3511 and ADC3711 have reduced the problem of high resolution, high accuracy analog-to-digital conversion to nearly the level of simplicity, economy, and compactness usually associated with digital logic circuitry. However, they are truly high precision analog devices, and require the same kind of design considerations given to all analog circuits. While great care has been taken in the design of the ADC3511 and ADC3711 to make their application as easy as possible, in order to utilize them to their full performance potential, good grounding, power supply distribution, decoupling, and regulation techniques should be exercised.

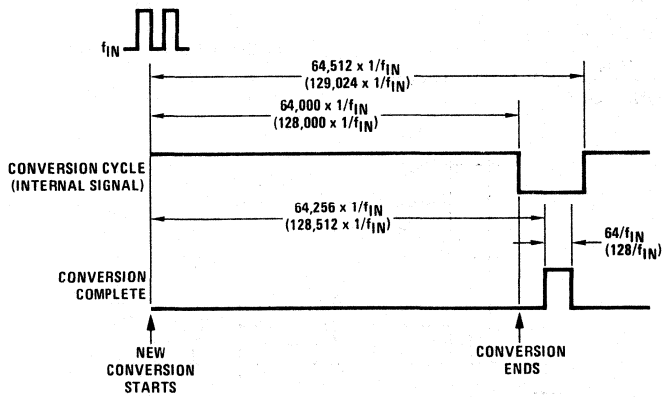


FIGURE 2. Conversion Cycle Timing Diagram for Free Running Operation (Times Shown in Parentheses are for the ADC3711)

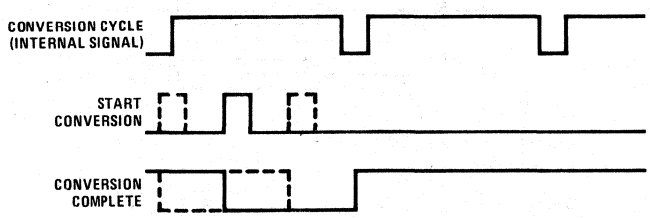


FIGURE 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Truth Table

DIGIT SELECT INPUTS			SELECTED DIGIT
DLE	D1	D0	
L	L	L	Digit 0 (LSD)
L	L	H	Digit 1
L	H	L	Digit 2
L	H	H	Digit 3 (MSD)
H	X	X	Unchanged

L = Low logic level
H = High logic level
X = Irrelevant logic level

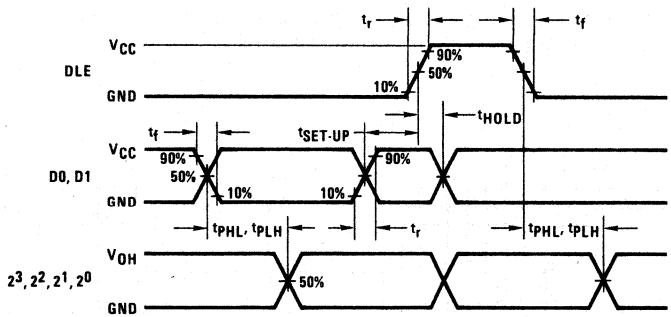
The value of the Selected Digit is presented at the 2^3, 2^2, 2^1 and 2^0 outputs in BCD format.

Note 1: If the value of a digit changes while it is selected, that change *will* be reflected at the outputs.

Note 2: An overflow condition will be indicated by a high level on the OVERFLOW output (pin 5) and E16 in all digits.

Note 3: The sign of the input voltage, when these devices are operated in the bipolar mode, is indicated by the SIGN output (pin 8). A high level indicates a positive voltage, a low level a negative.

Timing Diagrams



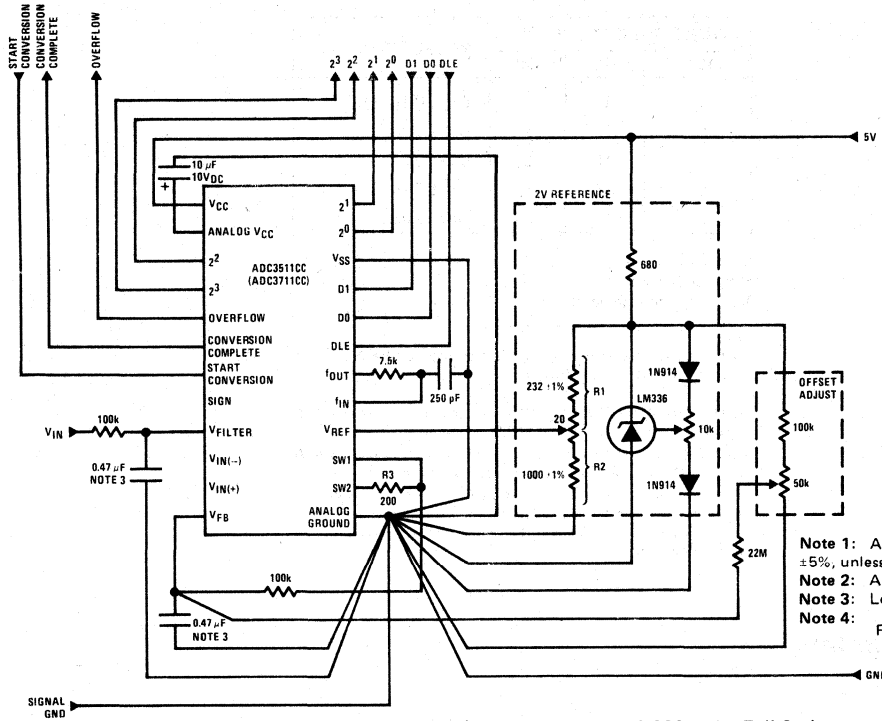
Typical Applications

Figure 4 shows the ADC3511 and ADC3711 connected to convert 0 to +2.000 volts full scale operating from a non-isolated power supply. (Note that the ADC3511 converts 0 to +1999 counts full scale, while the ADC3711 converts 0 to +3999 counts full scale.) In this configuration the SIGN output (pin 8) should be ignored. Higher voltages can, of course, be converted by placing fixed dividers in the inputs, while lower voltages can be converted by placing fixed dividers in the feedback loop, as shown in *Figure 6*.

Figures 5 and 6 show systems operating with isolated supplies that will convert both polarities of inputs. 60 Hz common-mode noise can become a problem in these configurations, so shielded transformers have been shown in the figures. The necessity for, and the type of shielding needed depends on the performance requirements, and the actual applications.

The filter capacitors connected to V_{FB} (pin 12) and V_{FILTER} (pin 11) should be of a low leakage variety. In the examples shown every 1.0 nA of leakage will cause approximately 0.1 mV error (1.0×10^{-9}A x 100 kΩ = 0.1 mV). If the currents in both capacitors are exactly equal however, little error will result since the source impedances driving both capacitors are approximately matched.

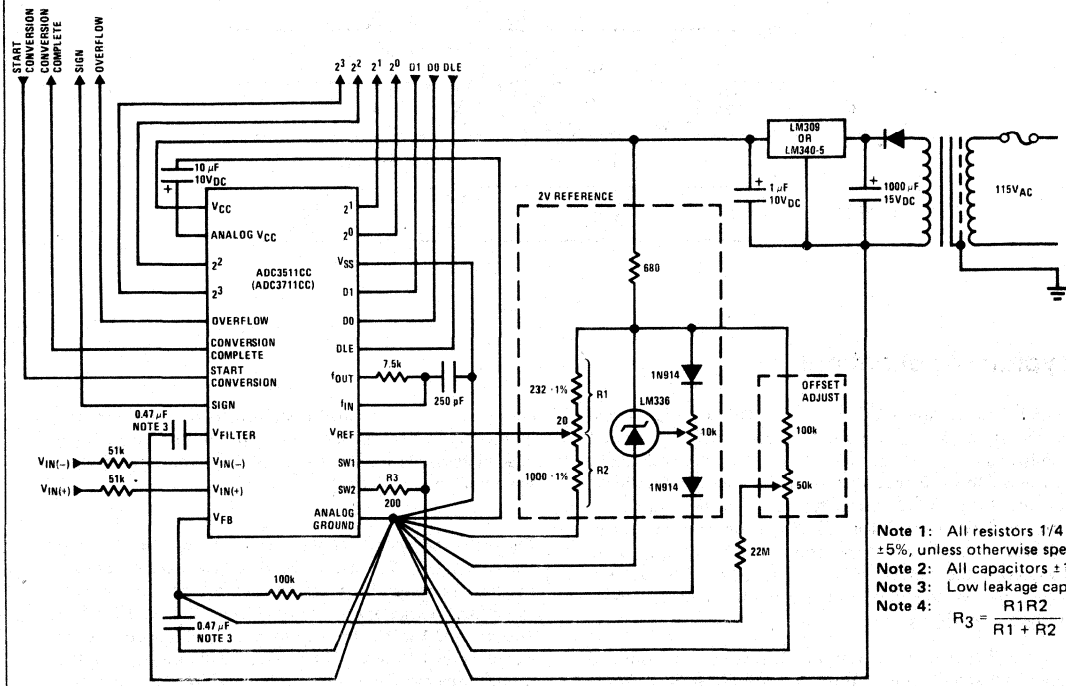
Typical Applications (Continued)



Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4:

$$R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega.$$

FIGURE 4. 3 1/2-Digit A/D; +1999 Counts, +2.000 Volts Full Scale
(3 3/4-Digit A/D; +3999 Counts, +2.000 Volts Full Scale)

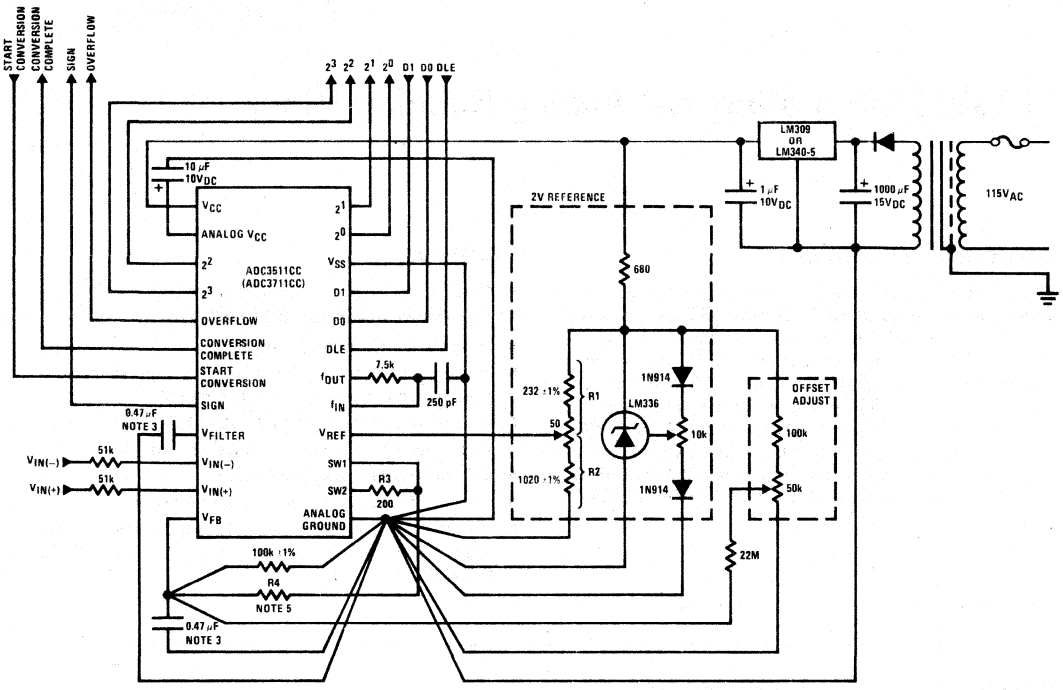


Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4:

$$R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega.$$

FIGURE 5. 3 1/2-Digit A/D; ±1999 Counts, ±2.000 Volts Full Scale
(3 3/4-Digit A/D; ±3999 Counts, ±2.000 Volts Full Scale)

Typical Applications (Continued)

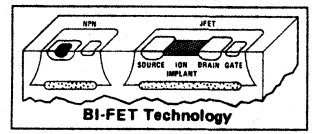


Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 50\Omega$.
Note 5: R4 = 900k ±1% for the ADC3511CC, 200.0 mV Full-Scale.
R4 = 400k ±1% for the ADC3711CC, 400.0 mV Full-Scale.

FIGURE 6. 3 1/2-Digit A/D; ±1999 Counts, ±200.0 mV Full Scale (3 3/4-Digit A/D; ±3999 Counts, ±400.0 mV Full-Scale)

National Semiconductor

Analog-to-Digital Converters



LF13300 Integrating A/D Analog Building Block

General Description

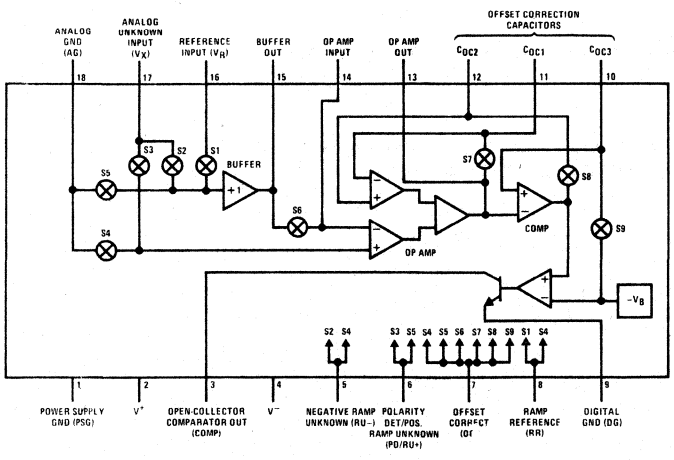
The LF13300 is the analog section of a precision integrating analog-to-digital (A/D) system. JFET and bipolar transistors (BI-FET) are combined on the same chip to provide a high input impedance unity gain buffer, comparator and integrator, along with 9 JFET analog switches. The LF13300 has sufficient resolution to construct up to a 4 1/2-digit Digital Panel Meter (DPM) or a 12-bit (plus sign) Data Acquisition System and is specifically designed for use with either the ADB4510 BCD digital building block or the ADB1200 (MM5863)* 12-bit binary building block.

*See ADB1200 (MM5863) data sheet for more information.

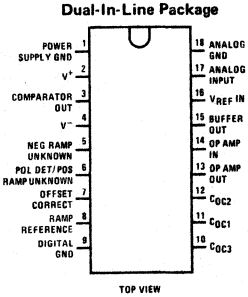
Features

- Rugged JFETs allow blow-out free handling
- High input impedance 10,000 MΩ typ
- Automatic offset correction
- Analog circuitry can be physically and electrically isolated from high noise digital circuits
- Analog input range of ±11V with ±15V supplies
- Wide power supply voltage range ±5V to ±18V
- TTL and CMOS compatible logic
- Can interface directly with microprocessors
- Versatile: can be used as a 12-bit plus sign binary A/D, 4 1/2-digit, 3 3/4-digit and 3 1/2-digit Digital Panel Meter (DPM)
- Low cost

Block and Connection Diagrams



Dual-In-Line Package



Order Number LF13300D
See NS Package D18A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation, (Note 1)	570 mW
Junction Temperature	110°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

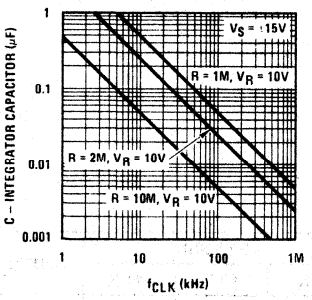
Electrical Characteristics (V_S = ±15V, T_A = 25°C, unless otherwise noted)

PARAMETER	CONDITIONS	TEST CIRCUIT	LF13300 MIN	LF13300 TYP	LF13300 MAX	UNITS
Analog Input Current, I_{IN}	V_X = 0	1, 2		80	500	pA
	$T_{MIN} \leq T_A \leq T_{MAX}$				5	nA
Analog Input Voltage Range	V_X Adjusted until $\|I_{IN}\| \geq$ 10 nA	1, 2			±11	V
Analog Input Resistance	V_X = 0	1, 2		10,000		MΩ
Reference Input Currents, I_R	V_R = 10V			1	100	nA
	$T_{MIN} \leq T_A \leq T_{MAX}$	3			10	μA
Reference Input Voltage Range	V_R Adjusted until $\|I_{Ri}\| \geq 10\ \mu A$	3	0		11	V
Reference Input Resistance	V_R = 10V	3		1000		MΩ
Offset Correction Voltage, $-V_B$		4		−12		V
Offset Correction		5		20	2000	pA
Input Current, I_{OC}		5			20	nA
Op Amp Slew Rate		6		10		V/μs
Op Amp Bandwidth		7		3		MHz
Buffer Slew Rate		9		25		V/μs
Comparator Response Time	200 μV Input Stop, 100 μV Overdrive	11		2.5		μs
Comparator Output Saturation Voltage	V_{CC} = 5V, R_L = 2k, $T_{MIN} \leq T_A \leq T_{MAX}$	11		0.25	0.4	V
Logic "1" Input Voltage	All Switching Input Pins 5, 6, 7, 8, $T_{MIN} \leq T_A \leq T_{MAX}$		2.0		5.0	V
Logic "0" Input Voltage	All Switching Input Pins 5, 6, 7, 8, $T_{MIN} \leq T_A \leq T_{MAX}$		−2.0		0.8	V
Logic Input Current	All Switching Input Pins 5, 6, 7, 8, $0 \leq V_L \leq 5V$, $T_{MIN} \leq T_A \leq T_{MAX}$			15	50	μA
Power Supply Voltage Range ±V_S	$V_R \leq V^+ - 3V$, V_{IN} = 0V		±4.75		±18	V
				3.0		mA
				−5.5		mA
	$T_{MIN} \leq T_A \leq T_{MAX}$				±11	mA

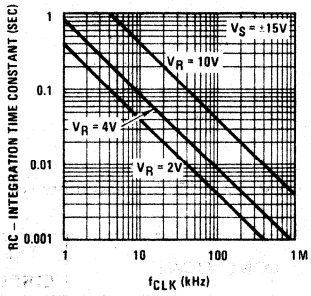
Note 1: For operating at elevated temperatures, the LF13300 in the dual-in-line package must be derated based on the thermal resistance of 100°C/W junction to ambient.

Typical Performance Characteristics

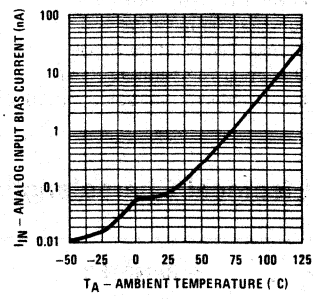
Integrator Capacitance, C vs f_{CLK} for Different Integrator Resistances, R



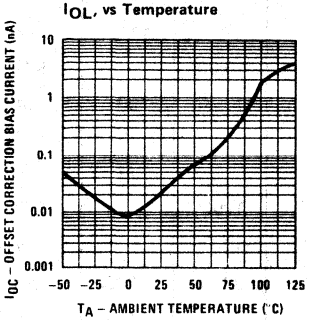
Integration Time Constant (RC) vs f_{CLK} for Different Reference Voltages, V_R



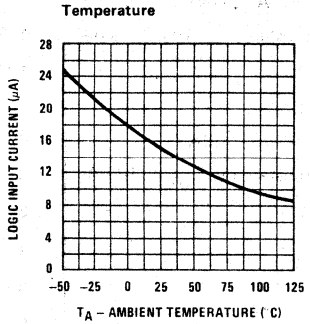
Analog Input Bias Current, I_{IN}, V_X = 0V, vs Temperature



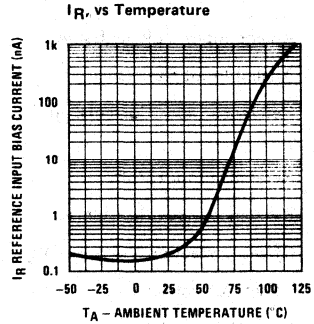
Offset Correction Bias Current, I_{OL}, vs Temperature



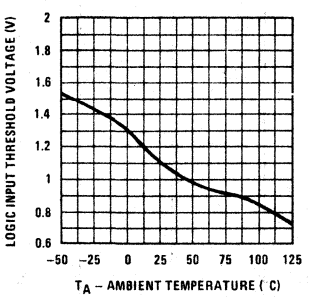
Logic Input Current vs Temperature



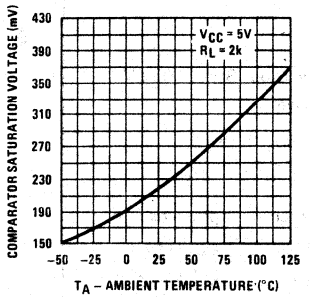
Reference Input Bias Current, I_R, vs Temperature



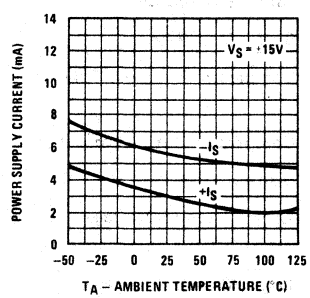
Logic Input Threshold Voltage vs Temperature



Comparator Saturation Voltage vs Temperature



Power Supply Current vs Temperature



Functional Description

The LF13300 goes through the following 5 states during normal cycle: 1) Offset Correction; 2) Polarity Determination; 3) Initialization; 4) Ramp Unknown; 5) Ramp Reference

Offset Correction Description *(Figure 1)*

The Offset Correction scheme will drive the input of the comparator to its switching threshold when the analog input is zero and the timing components, RC, are bypassed.

The Offset Correction input (OC) is driven high, closing switches S4–S9.

The offset voltages are assigned as follows: V_{OS1} – the input offset voltage of the buffer; V_{OS2} – the input offset voltage of A1; V_{OS3} – the input offset voltage of A2; V_{OS4} – the input offset voltage of the comparator.

S5 grounds the input of the buffer so that its output voltage is simply V_{OS1}. S6 bypasses R to keep the integration time constant, RC, from affecting the circuit operation. S4 makes the total equivalent input voltage to A1 be $-V_{OS1} - V_{OS2}$. S7 puts the op amp in a unity gain configuration with respect to the input of A2. S8 keeps the output voltage of the op amp at $-V_B + V_{OS4} = -V_B'$ (the Offset Correction potential) since the comparator is placed inside the loop. C3 samples the output of the $-V_B$ generator. The voltage at the non-inverting input of A2 is $-V_B - V_{OS1} -$

Functional Description (Continued)

$V_{OS2} - V_{OS3} + V_{OS4} = V1$. Thus, the sum of the offsets is stored on C1, and the differential voltage across the comparator is zero.

Polarity Determination *(Figure 2)*

The simplified diagram of the LF13300 in the Polarity Determination state is shown in *Figure 2*. S5 and S3 are closed during this period. S5 grounds the buffer input and V_X (the unknown voltage) is applied through S3 to the non-inverting input of A1. The equation that describes the op amp output voltage is given in *Figure 2*. When V_X is applied to A1 at t_1, the output of the op amp slews to V_X and is integrated until t_2, when S3 opens and S4 closes. At t_2, V_{OUT} slews down by $-V_X$ leaving $\frac{1}{RC}\int_{t_2}^{t_2} V_X dt - V_B'$ at the op amp output.

Just before t_2, the comparator senses the op amp output with respect to $-V_B$; the comparator output goes high if $V_X > 0$ and remains low if $V_X \leq 0$.

Initialization *(Figure 1)*

During initialization, the configuration is the same way as it is in the Offset Correction state and the op amp output is brought back to the Offset Correction potential $-V_B'$.

Ramp Unknown *(Figures 2 and 3)*

In the Ramp Unknown state, if $V_X \geq 0$, S3 and S5 are closed, as shown in *Figure 2*, and V_X is applied to the + input of the integrator. If $V_X < 0$, the device is connected as in *Figure 3* with S2 and S4 closed. V_X is now applied through the buffer to the − input of the integrator. In either Ramp Unknown case, the op amp output ramps in the positive direction and V_X is applied to a high impedance JFET input.

Ramp Reference *(Figure 4)*

In this state, the LF13300 is configured with switches S1 and S4 closed. The reference voltage, V_R, a positive voltage, is applied to the buffer input and the op amp output ramps down until $V_{OUT} = -V_B'$ where the comparator will trip.

If V_X and V_R are assumed to be constant over their respective integration periods, the integrals of *Figure 4* are reduced to,

$$\frac{V_X (t_4 - t_3)}{RC} = \frac{V_R (t_5 - t_4)}{RC}$$

or

$$\frac{V_X}{V_R} = \frac{t_5 - t_4}{t_4 - t_3}.$$

Since $t_4 - t_3 = 4096$ clock periods and $t_5 - t_4$ can be measured in clock periods, $V_X/V_R = X/2^{12}$, where X is a digital binary output representing an analog input V_X with respect to V_R.

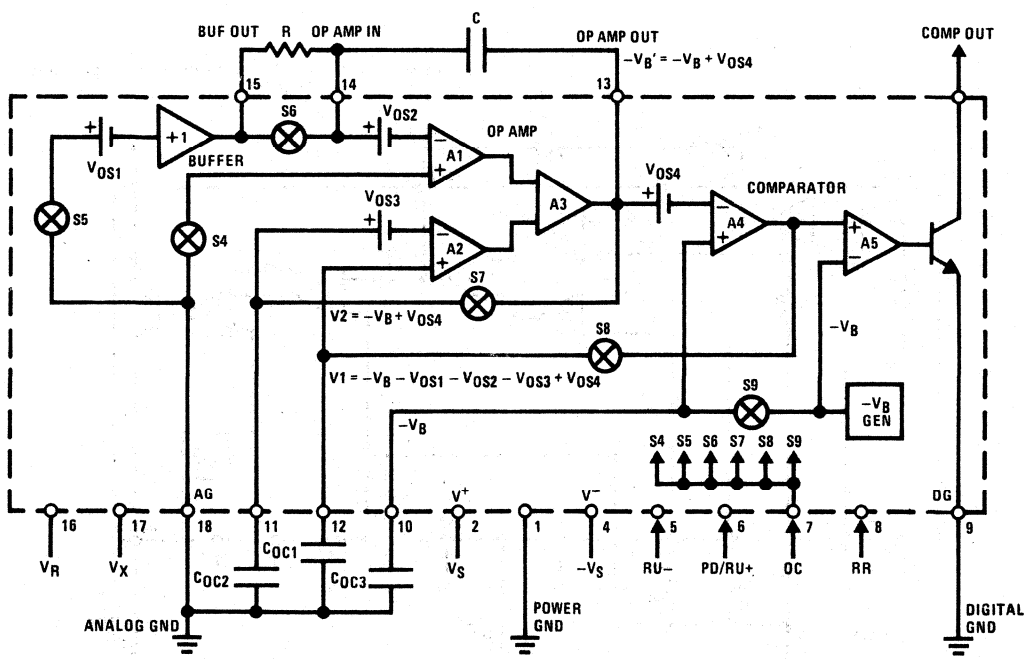


FIGURE 1. Offset Correction Circuit

Functional Description (Continued)

$$V_{OUT} = \begin{cases} -V_B' + V_X + \frac{1}{RC}\int_{t_3}^{t_4} V_X\,dt: \text{Ramp Unknown for } V_X \geq 0 \\ -V_B' + V_X + \frac{1}{RC}\int_{t_1}^{t_2} V_X\,dt: \text{Polarity Determination} \end{cases}$$

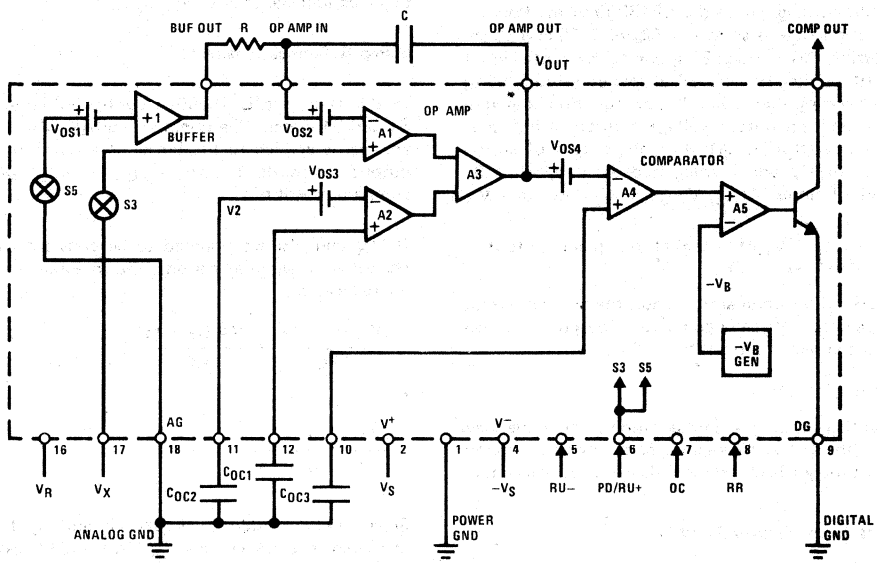


FIGURE 2. Polarity Determination Circuit or Ramp Unknown Circuit for $V_X \geq 0$

$$V_{OUT} = -V_B' + \frac{1}{RC}\int_{t_3}^{t_4} V_X\,dt: \text{Ramp Unknown for } V_X < 0$$

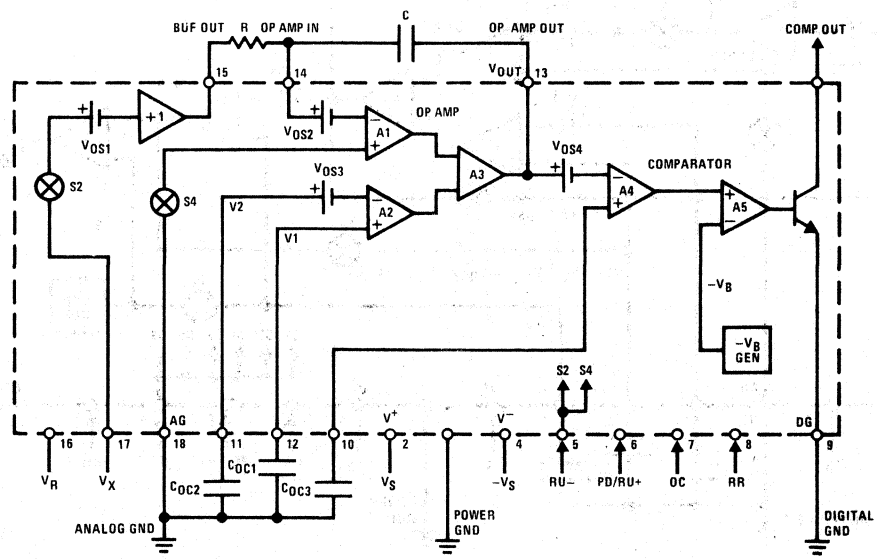
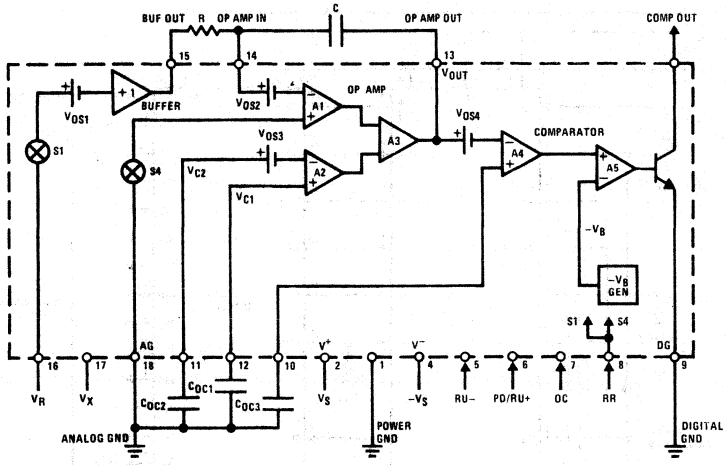


FIGURE 3. Ramp Unknown for $V_X < 0$

Functional Description (Continued)

$$V_{OUT}^{*} = -V_B' + \frac{1}{RC}\left(\int_{t_3}^{t_4} V_X\,dt - \int_{t_4}^{t_5} V_R\,dt\right)$$



*More accurately

$$V_{OUT} = -V_B' + \frac{1}{RC}\left(\int_{t_4}^{t_5+\Delta} V_R\,dt + \int_{t_3}^{t_4} V_X\,dt\right) + \delta$$

Where δ is the incremental voltage overdrive needed to fully switch the comparator and Δ is the sum of the additional time required to develop δ and the comparator propagation delay.

FIGURE 4. Ramp Reference Circuit

12-Bit A/D Converter Electrical Characteristics

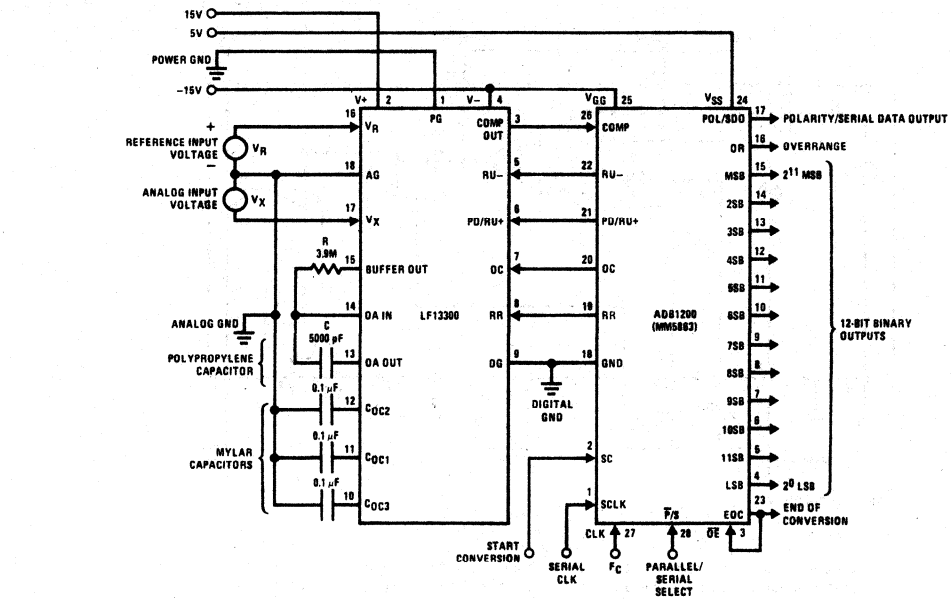
12-bit plus sign. (LF13300 with ADB1200 (MM5863)). (V_R = 10.000V, F_C = 250 kHz, 0°C ≤ T_A ≤ +70°C unless otherwise noted.)

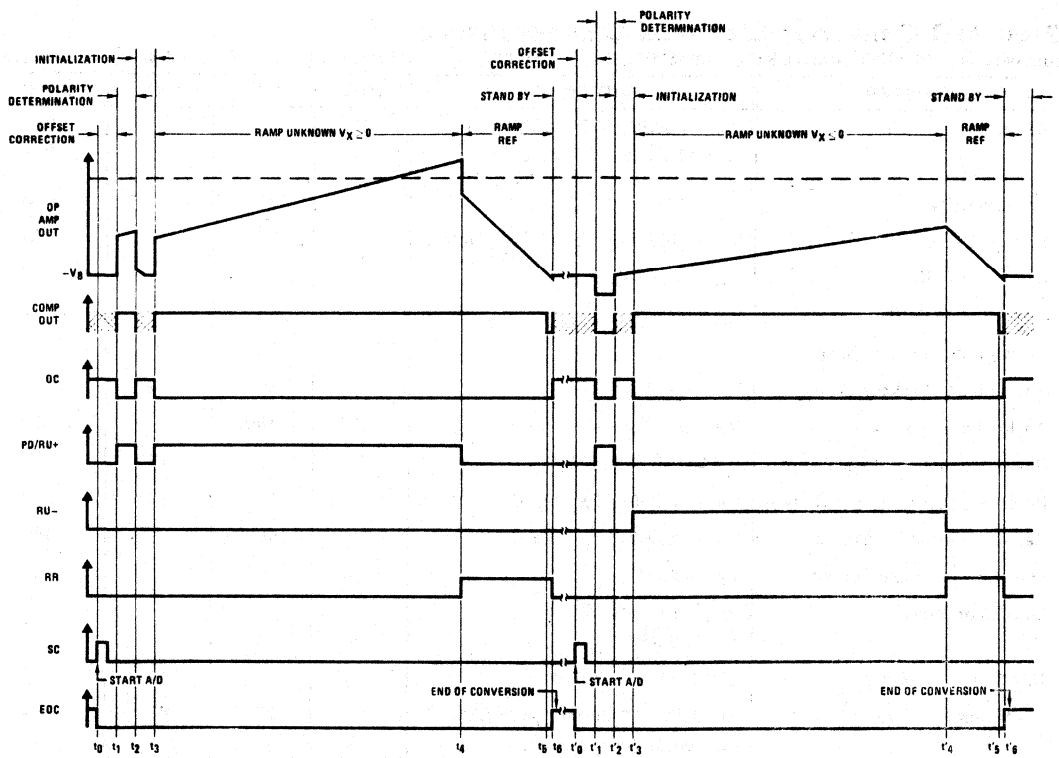
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution (Note 3)	V_R = 5.000V, −10V ≤ V_X ≤ +10V	13			Bits
	F_C = 125 kHz, T_A = 25°C	14			Bits
Non-Linearity			±1/8	±1/2	LSB
Ratiometric Gain Error (Def.)	V_X = ±10.000V, T_A = 25°C, (Note 2)		±1/2	±2	LSB
Gain Error Drift	V_X = 10.000V		±1		ppm/°C
Zero Reading Drift	V_X = 0V		±0.5		ppm/°C
Analog Input Voltage Range		±11	±12		V
Analog Input Leakage Current	V_X = 0V, T_A = 25°C		80	500	pA
Analog Input Resistance	V_X = 0V, T_A = 25°C	100	1000		MΩ
Reference Input Voltage Range	V_R Varied, T_A = 25°C	4		12	V
Reference Input Leakage Current	V_R = 10.000V, T_A = 25°C		1	100	nA
Reference Input Resistance	V_R = 10.000V, T_A = 25°C	100	1000		MΩ
Start Conversion Pulse Width	V_{SC} = 2.4V	2.4			μs
Conversion Time	V_{IN} = 10.000V t_c = 8960/F_C			36	ms
15V Supply Currents	LF13300, V^+ Current			11	mA
−15V Supply Currents	LF13300, V^- Current, ADB1200 (MM5863), V_{GG} Current		27	45	mA
5V Supply Currents	V_{IN} = 0V, ADB1200 (MM5863), V_{SS} Current		23	39	mA

Note 2: The A/D converter system must have been operational for a minimum of 30 seconds before this measurement is made. This is to relax the dielectric absorption effects of the integration capacitor, C.

Note 3: Polarity and Overrange outputs are considered as additional output bits.

12-Bit A/D Converter Circuit and Timing Diagrams





*Note. All TTL signal level.

FIGURE 5.

Application Hints

Increasing the Input Impedance of the LF13300, MM5863 12-Bit A/D Converter

The input impedance of the LF13300, ADB1200 (MM5863) A/D converter can be increased 1 to 2 orders of magnitude over the typical 1000 MΩ cited in the 12-bit A/D specifications by insuring that the signals that switch the LF13300 do not overlap. A circuit that eliminates switching overlap by introducing a Delay (t_d) ≈ 3.3k x 100 pF ≈ 300 ns to the rising edge of the signals from the ADB1200 (MM5863) is shown in *Figure 6. Figure 7* shows the operation of this circuit. The total delay time t_r' of the output will be equal to the inherent gate rise time, t_r, plus the RC delay, t_d. The fall time, t_f will be the basic gate delay.

Nulling the Residual Offset

The residual offset is < 200 μV which is negligible for most applications. This can be reduced to < 40 μV by lowering the clock frequency from 250 kHz to about 75 kHz. If a lower residual offset is required, we may trim out the remainder as shown in *Figure 8*. This circuit applies a negative step to the offset correction capacitor, C_{OC2}, by means of a variable capacitor which is adjusted until charge injection imbalance of the offset correction switches are cancelled.

Eliminating Errors Due to Power Supply Noise

For many applications, power supply noise (f ≥ 10 Hz) causes errors which reduces the accuracy of the system. In most applications, noise can be adequately eliminated by putting a series resistor (100Ω) in the power supply line with a 10 μF tantalum capacitor connected at the power supply pins *(Figure 9)*. The 10 μF capacitor is, in addition to the normal 0.1 μF ceramic disc capacitors, used as supply bypass capacitors.

Errors caused by noise on the negative supply, $-V_S$, can be further reduced by replacing, C_{OC3} with a 10 μF low leakage tantalum capacitor. Since $-V_B$ is 3V above $-V_S$, any noise appearing at $-V_S$ appears at $-V_B$; the 10 μF capacitor eliminates this noise.

Continuous Conversion Mode

For using the MM5863 in the continuous conversion mode, connect the end of conversion output, EOC (pin 23), to the output enable input, OE (pin 3), and connect the start conversion input, SC (pin 2) to 5V.

Miscellaneous

Since none of the output pins employ short-circuit protection, extreme care should be taken when breadboarding or troubleshooting with the power ON.

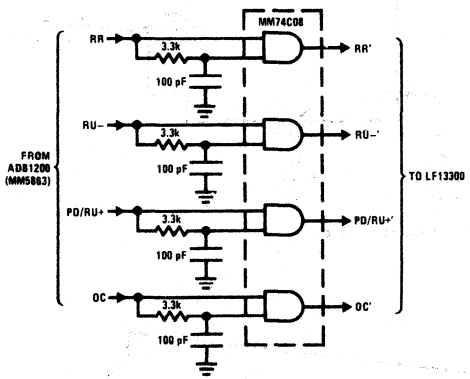


FIGURE 6. Overlap Elimination Circuit

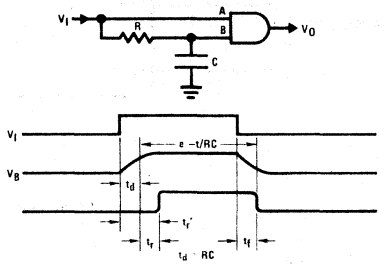


FIGURE 7. Rise Time Delay Circuit

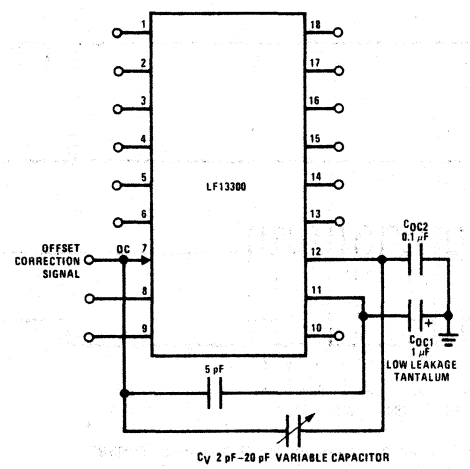


FIGURE 8. Residual Offset Nulling Circuit

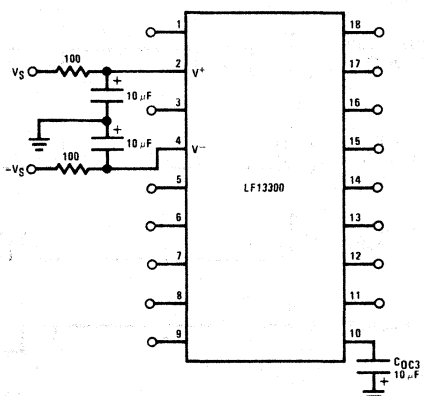
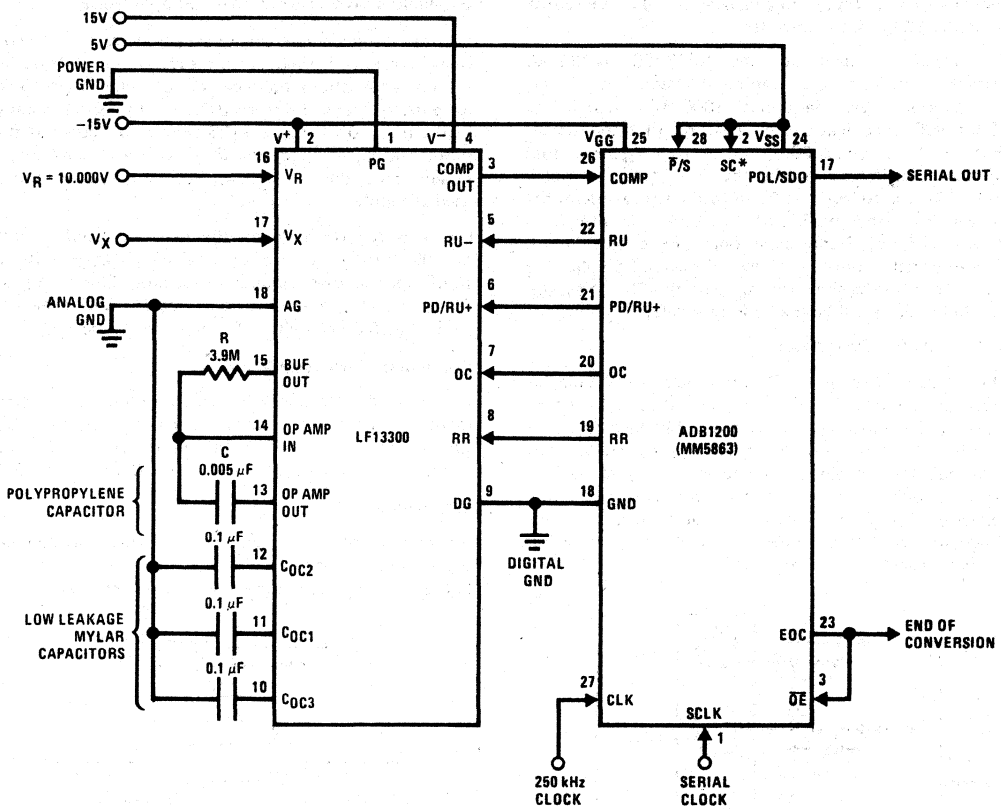


FIGURE 9. Power Supply Noise Reduction Circuit

Typical Applications



*SC at logic "1" for continuous conversion mode

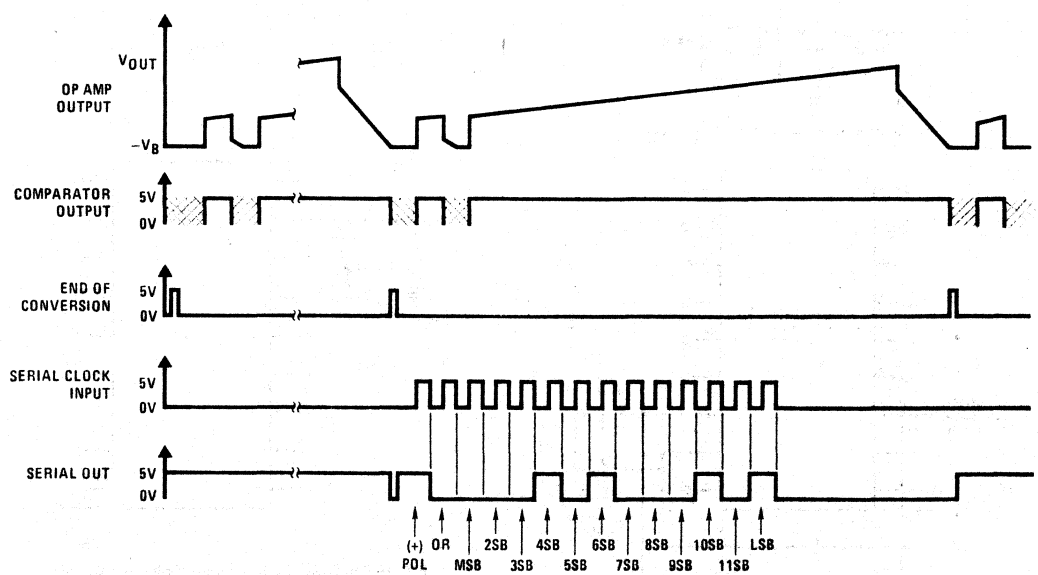
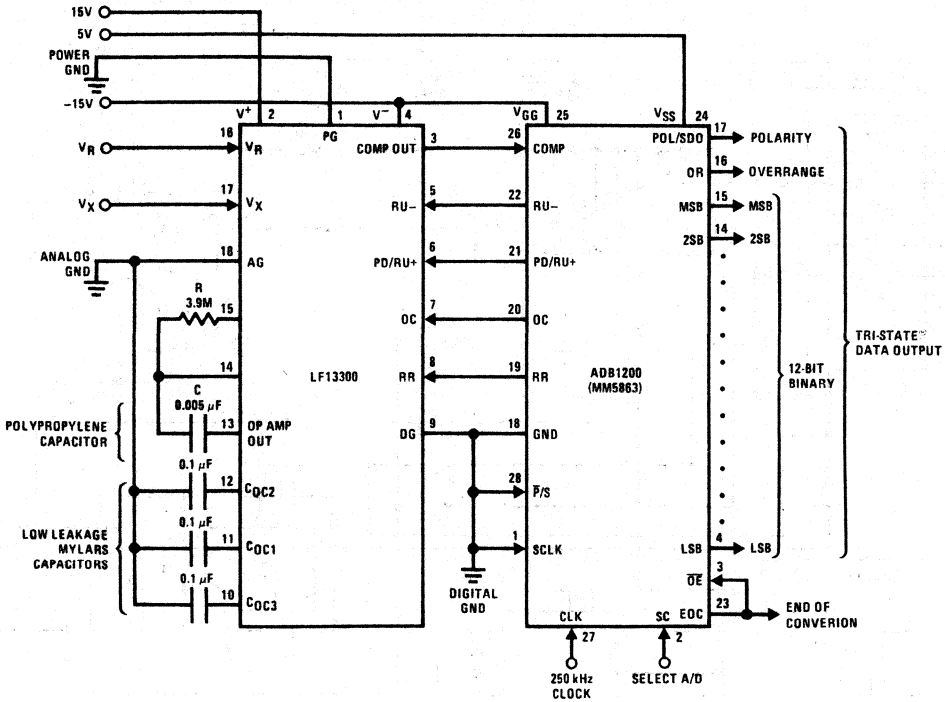
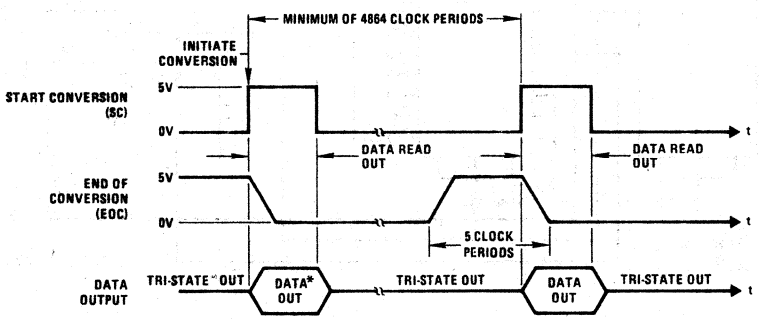


FIGURE 10. Continuous Conversion 12-Bit Plus Sign Serial Output A/D Using the LF13300 and the MM5863

Typical Applications (Continued)





* Note. Prior to the first conversion cycle, the data outputs will all be in a "1" state when the outputs are enabled ($\overline{OE}$ in "0" state).

FIGURE 11. 12-Bit Plus Sign A/D in Command Conversion Mode

4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

Figure 12 shows a low speed, high accuracy, data acquisition unit where the analog input signal is acquired differentially and preconditioned through an LF352 monolithic instrumentation amplifier. To eliminate amplifier offset errors, autozeroing circuitry is added around the LF352 and is timed through the ADB1200 and flip-flop C. Flip-flops A and B form a 2-bit up counter for channel select.

The instrumentation amplifier is zeroed at power-up and after each conversion as shown in the timing diagram; during autozero the multiplexer is disabled. When the system does polarity detection and A/D conversion, the LF352 is active and the multiplexer is enabled. The zeroing cycle for the LF13300 and the LF352 lasts for 256 clock periods, so the maximum clock frequency will depend upon the required accuracy and the minimum zeroing time of the instrumentation amplifier. Notice here that the system accuracy will be less than 12 bits since it will be affected by the gain linearity of the instrumentation amplifier.

For more details concerning data acquisition, see AN-156 and LF11508/LF11509 data sheet. For details on the instrumentation amplifier, see the LF352 data sheet.

Typical Applications (Continued)

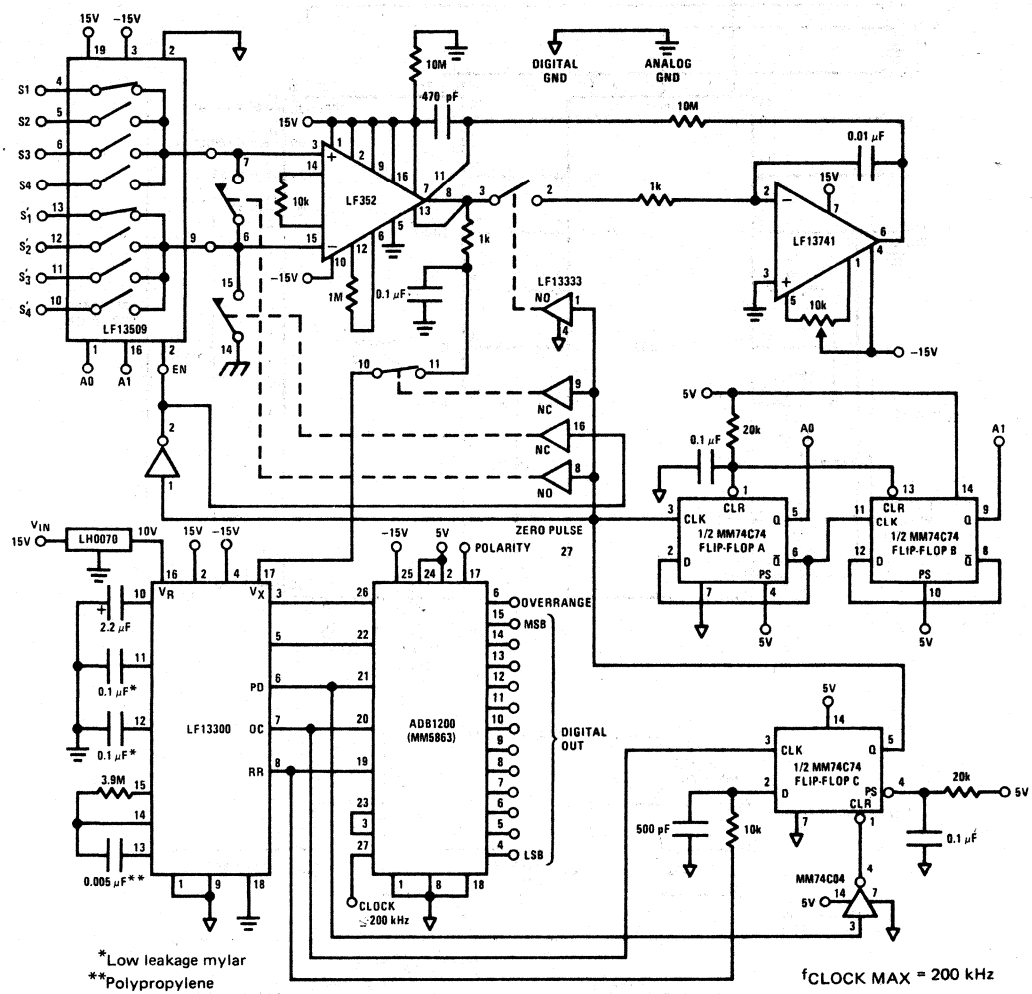


FIGURE 12. 4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

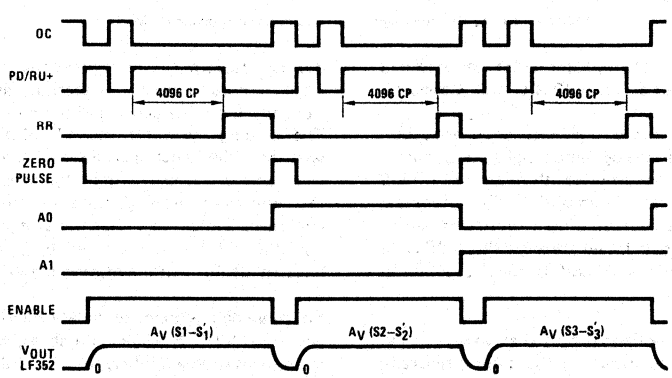
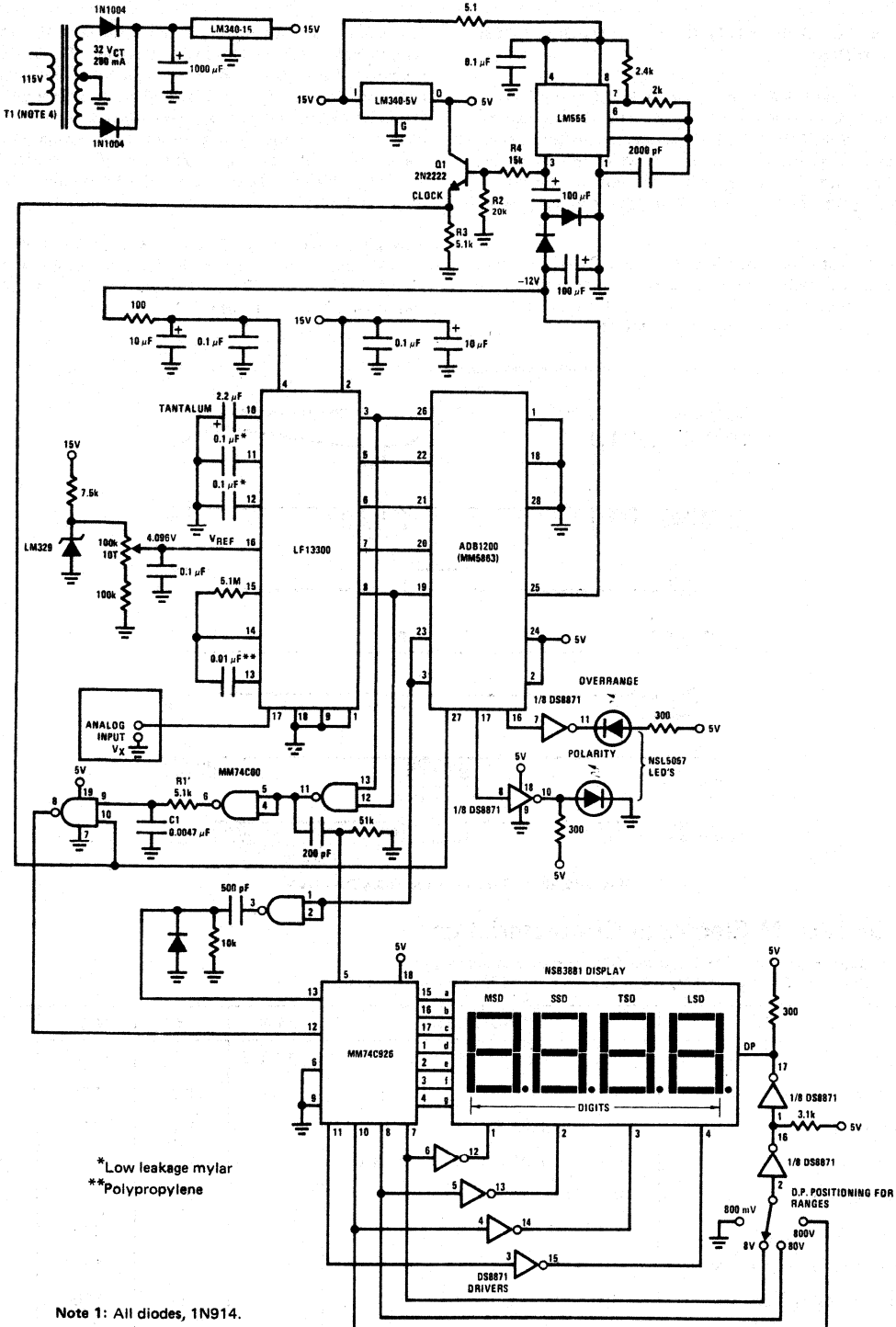


FIGURE 13. Timing Diagram for *Figure 12*

Typical Applications (Continued)



*Low leakage mylar
**Polypropylene

Note 1: All diodes, 1N914.
Note 2: All resistors 1/4W, 5% tolerance.
Note 3: Circuit drawn for 8V full scale operation input scaling not shown.
Note 4: Inductive components U4X003 or Microtran PC6714.

FIGURE 19. 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM Schematic Diagram

Typical Applications (Continued)

3 3/4 Plus Digit (±8191 Counts)/3 1/2-Digit (±1999 Counts) DPM

In this circuit of *Figure 19*, the LF13300 and ADB1200 interact as previously described. The CMOS counter (MM74C926, MM74C928) is connected to count clock pulses during the ramp reference cycle. The counts are latched into the display when the comparator output trips, (goes low), as shown in the timing diagram *Figure 20*.

The RC network consisting of R1 and C1 is a low pass filter that prohibits the fast transients that occur on the comparator output during Offset Correction from loading any erroneous counts into the counter.

The DPM is able to operate from a single 15V power supply with the aid of a dc-dc converter. The LM555 generates the negative voltages required in the circuit and also doubles as the clock. The combination of Q1, R2, R3 and R4 forms a level shift to convert the output swing of the LM555 to a 0V–5V swing that is compatible with the logic. The LM340–5 drops the incoming 15V to 5V for use by the logic circuits and the LED display.

This circuit can be a 3 3/4 plus digit DPM if the MM74C926 is used or a 3 1/2-digit DPM if the MM74C928 is used. These counters are pin compatible and physically interchangeable.

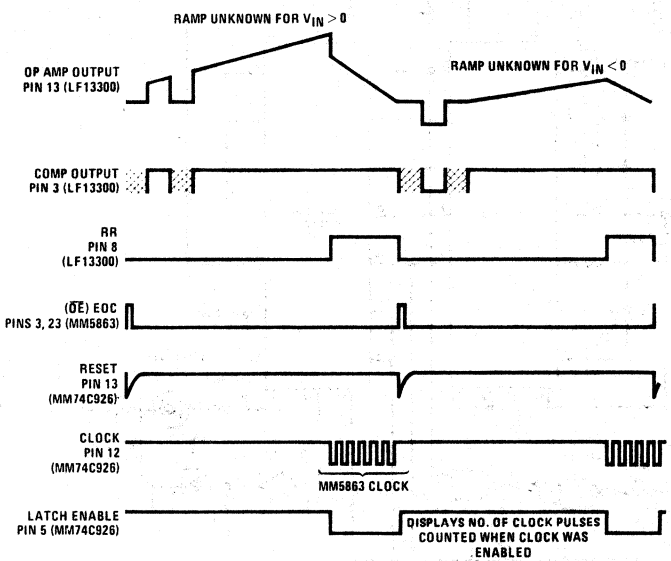


FIGURE 20. Timing Diagram for 3 3/4-Digit DVM

3 3/4-Digit DPM Electrical Characteristics

3 3/4 plus digits plus sign (±8191 counts) DPM system characteristics.
(Circuit as in *Figure 18*, $V_S = \pm 15V$, $V_R = 4.096V$, $T_A = 25^\circ C$, unless otherwise noted).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	$-8.2V \leq V_X \leq +8.2V$	16,382			Counts
Nonlinearity	$V_{IN} = 4.000V$		±1/8	±1/2	Counts
Ratiometric Gain Error	$V_{IN} = 4.000V$		±1/2	±2	Counts
Gain Error Drift	$V_{IN} = 4.000V$, $0^\circ C \leq T_A \leq +70^\circ C$		±1		ppm/°C
Zero Reading Drift	$V_{IN} = 0V$		±1		ppm/°C
Analog Input Voltage Range				±11	V
Reference Input Voltage Range	Reference Varied	0		+12	V
Analog Input Leakage Current	$V_{IN} = 0V$		80	500	pA
Reference Input Leakage Current			1	100	nA
Analog Input Resistance	$V_{IN} = 0V$		1000		MΩ
Conversion Time	$V_{IN} = 4.000V$, $f_C = 125$ kHz			74	ms

Typical Applications (Continued)

Component Side Foil

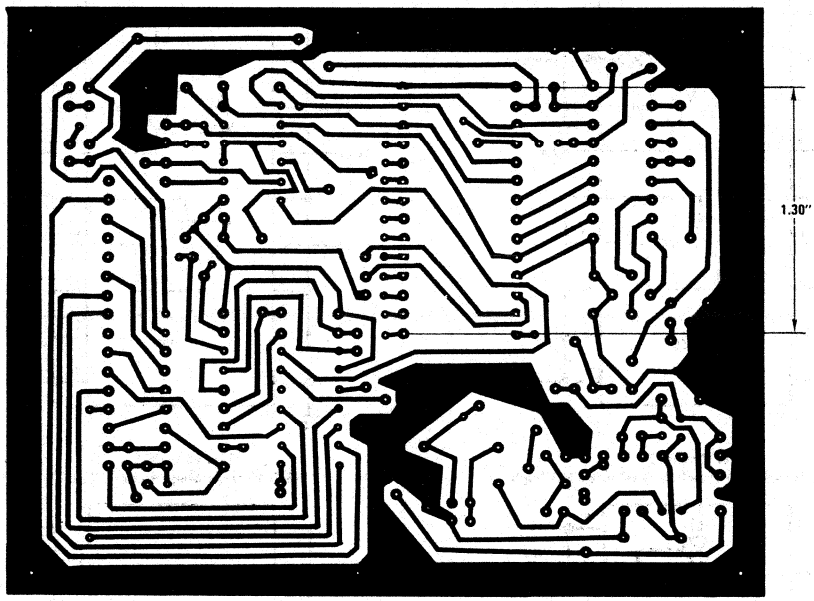


FIGURE 21. PC Board for 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM

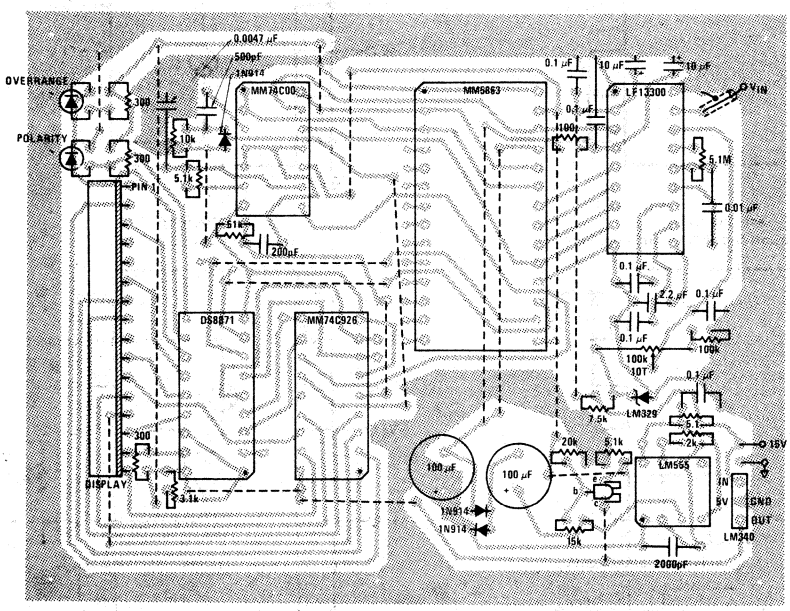
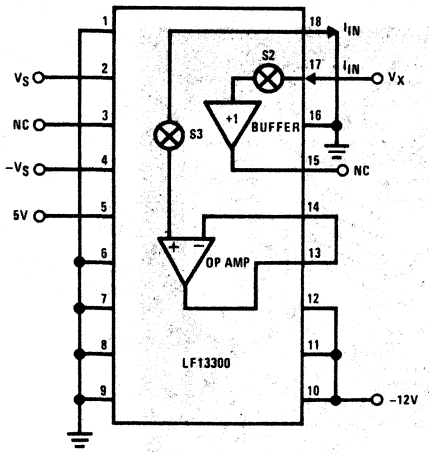


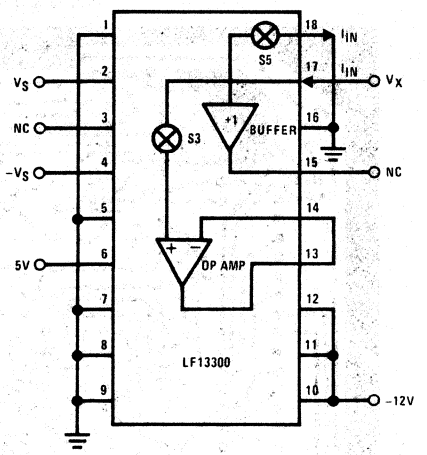
FIGURE 22. Stuffing Diagram for 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM

AC Test Circuits

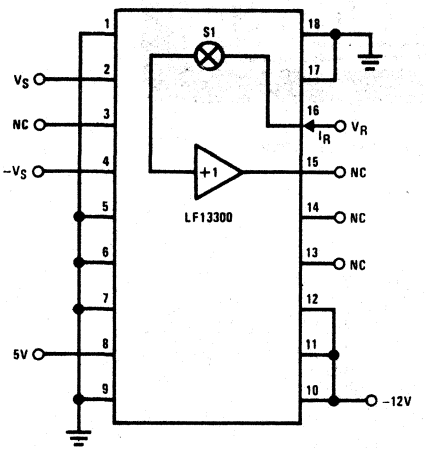
Test Circuit 1
Analog Input Characteristics Test with RU – High



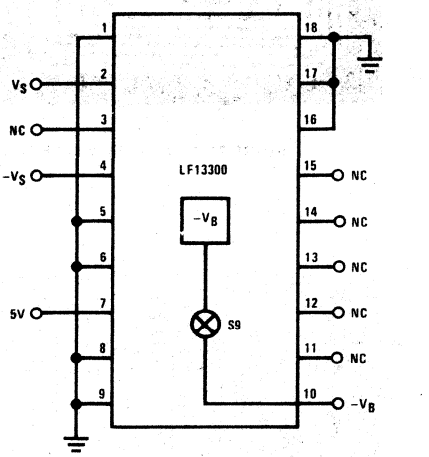
Test Circuit 2
Analog Input Characteristics Test with PD/RU+ High



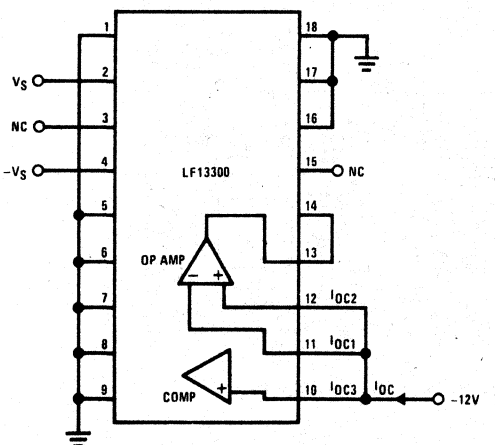
Test Circuit 3
Reference Input Characteristic Test with RR High



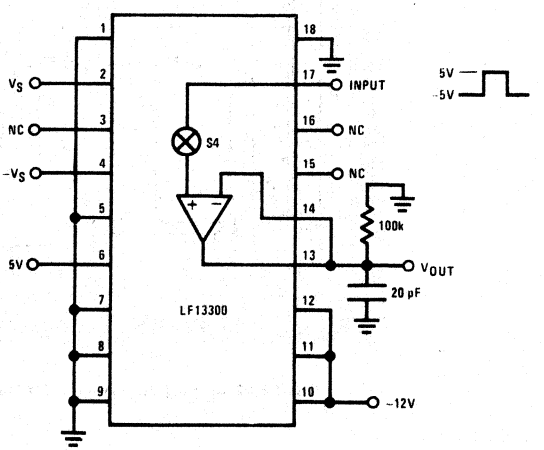
Test Circuit 4
–VB Voltage Measurement Test



Test Circuit 5
Offset Correction Input Current, I_{OC} Test

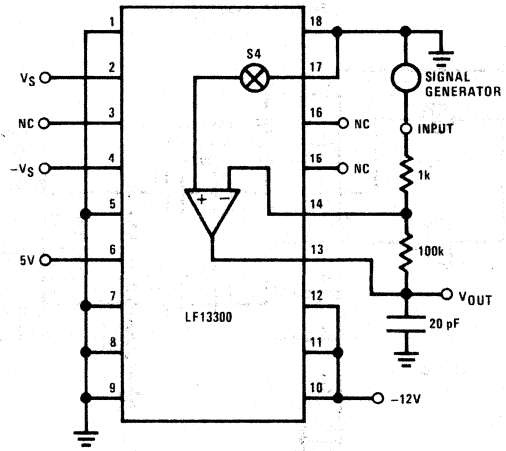


Test Circuit 6
Op Amp Slew Rate Test

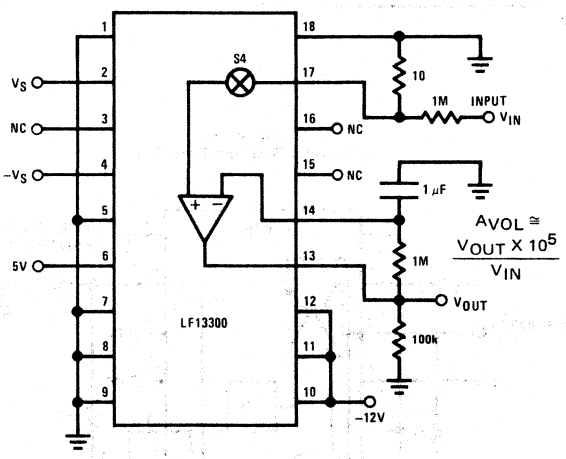


AC Test Circuits (Continued)

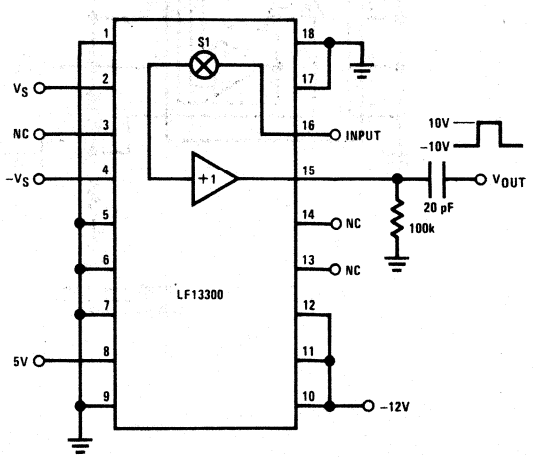
Test Circuit 7
Frequency Response Test



Test Circuit 8
Open Loop Gain Test

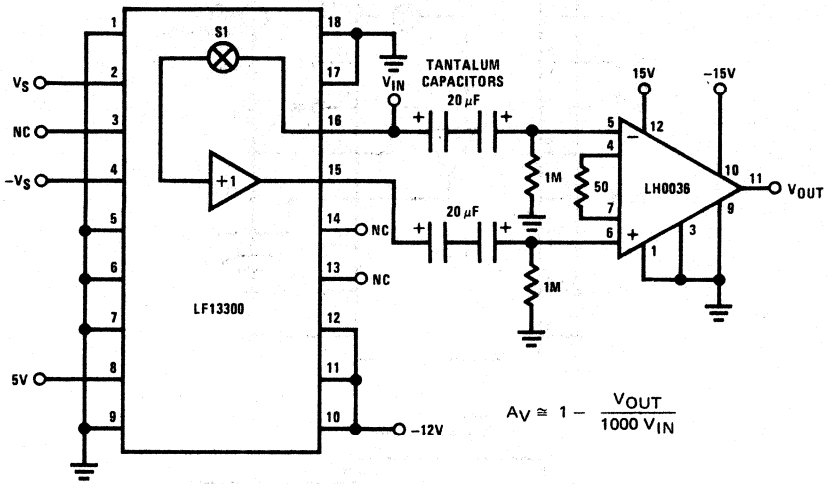


Test Circuit 9
Buffer Slew Rate Test

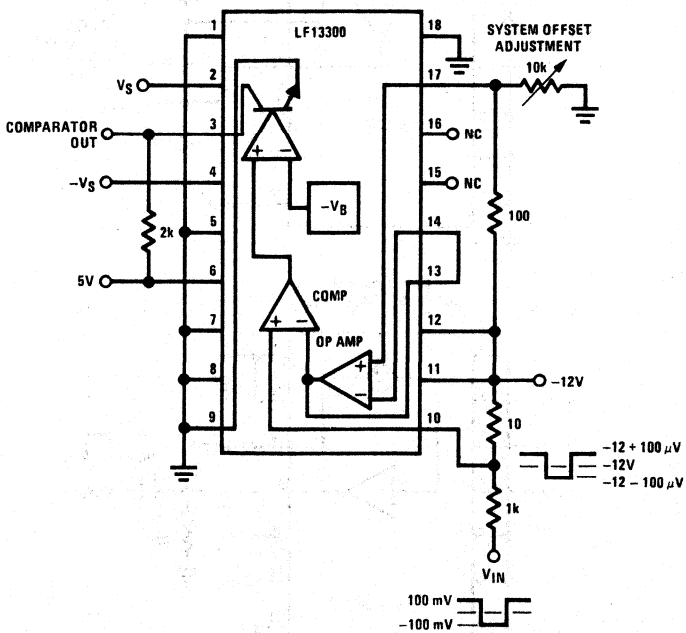


AC Test Circuits (Continued)

Test Circuit 10
Buffer Voltage Gain Test



Test Circuit 11
Comparator Response Time Test



National Semiconductor

Analog-to-Digital Converters

LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

General Description

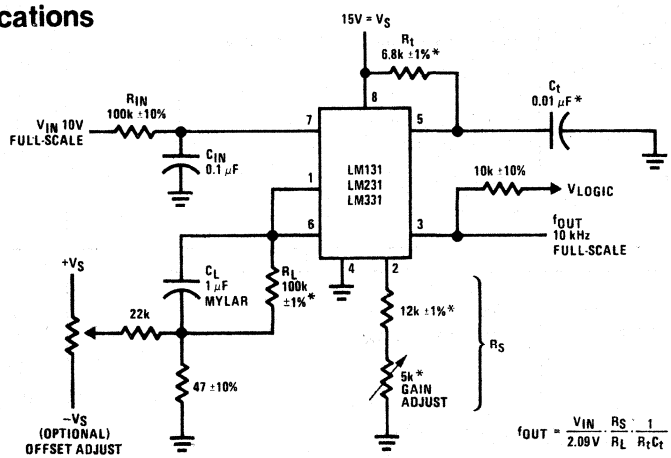
The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

Typical Applications



*Use stable components with low temperature coefficients. See Typical Applications section.

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

Absolute Maximum Ratings

	LM131A/LM131	LM231A/LM231	LM331A/LM331
Supply Voltage	40V	40V	40V
Output Short Circuit to Ground	Continuous	Continuous	Continuous
Output Short Circuit to V_{CC}	Continuous	Continuous	Continuous
Input Voltage	−0.2V to +V_S	−0.2V to +V_S	−0.2V to +V_S
	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}
Operating Ambient Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA})			
(H Package) P_D	670 mW	570 mW	570 mW
θ_{jA}	150°C/W	150°C/W	150°C/W
(N Package) P_D		500 mW	500 mW
θ_{jA}		155°C/W	155°C/W

Electrical Characteristics T_A = 25°C unless otherwise specified. (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VFC Non-Linearity (Note 2)	4.5V ≤ V_S ≤ 20V		±0.003	±0.01	% Full-Scale
	T_{MIN} ≤ T_A ≤ T_{MAX}		±0.006	±0.02	% Full-Scale
In Circuit of *Figure 1*	V_S = 15V, f = 10 Hz to 11 kHz		±0.024	±0.14	% Full-Scale
Conversion Accuracy Scale Factor (Gain)	V_{IN} = −10V, R_S = 14 kΩ				
LM131, LM131A, LM231, LM231A		0.95	1.00	1.05	kHz/V
LM331, LM331A		0.90	1.00	1.10	kHz/V
Temperature Stability of Gain	T_{MIN} ≤ T_A ≤ T_{MAX}, 4.5V ≤ V_S ≤ 20V				
LM131/LM231/LM331			±30	±150	ppm/°C
LM131A/LM231A/LM331A			±20	±50	ppm/°C
Change of Gain with V_S	4.5V ≤ V_S ≤ 10V		0.01	0.1	%/V
	10V ≤ V_S ≤ 40V		0.006	0.06	%/V
Rated Full-Scale Frequency	V_{IN} = −10V	10.0			kHz
Overrange (Beyond Full-Scale) Frequency	V_{IN} = −11V	10			%
INPUT COMPARATOR					
Offset Voltage			±3	±10	mV
LM131/LM231/LM331	T_{MIN} ≤ T_A ≤ T_{MAX}		±4	±14	mV
LM131A/LM231A/LM331A	T_{MIN} ≤ T_A ≤ T_{MAX}		±3	±10	mV
Bias Current			−80	−300	nA
Offset Current			±8	±100	nA
Common-Mode Range	T_{MIN} ≤ T_A ≤ T_{MAX}	−0.2		V_{CC}−2.0	V
TIMER					
Timer Threshold Voltage, Pin 5		0.63	0.667	0.70	x V_S
Input Bias Current, Pin 5	V_S = 15V				
All Devices	0V ≤ $V_{PIN\ 5}$ ≤ 9.9V		±10	±100	nA
LM131/LM231/LM331	$V_{PIN\ 5}$ = 10V		200	1000	nA
LM131A/LM231A/LM331A	$V_{PIN\ 5}$ = 10V		200	500	nA
$V_{SAT\ PIN\ 5}$ (Reset)	I = 5 mA		0.22	0.5	V

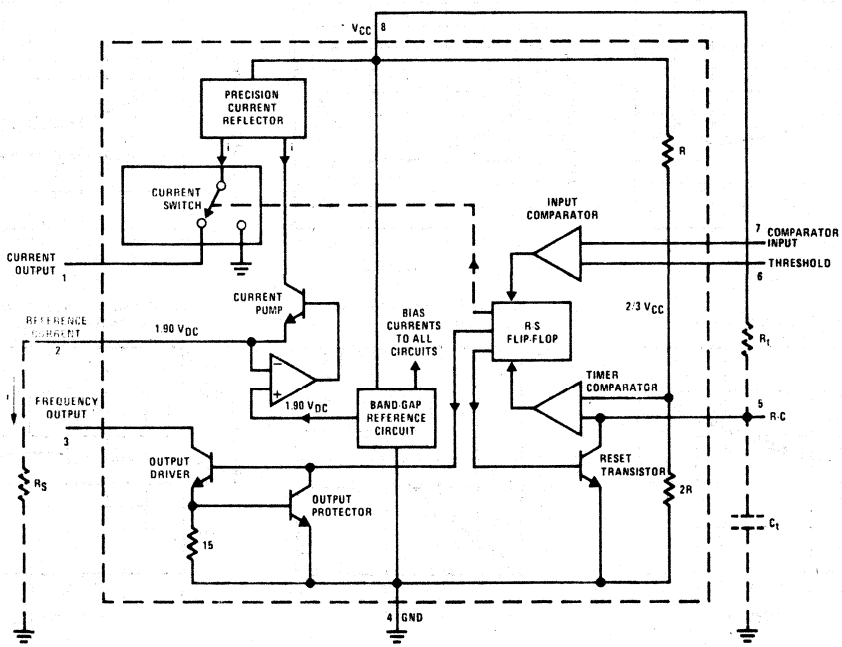
Electrical Characteristics (Continued) $T_A = 25°C$ unless otherwise specified (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT SOURCE (Pin 1)					
Output Current	$R_S = 14\ k\Omega$, $V_{PIN\ 1} = 0$				
LM131, LM131A, LM231, LM231A		126	135	144	μA
LM331, LM331A		116	136	156	μA
Change with Voltage	$0V \leq V_{PIN\ 1} \leq 10V$		0.2	1.0	μA
Current Source OFF Leakage					
LM131, LM131A			0.01	1.0	nA
LM231, LM231A, LM331, LM331A			0.02	10.0	nA
All Devices	$T_A = T_{MAX}$		2.0	50.0	nA
Operating Range of Current (Typical)			(10 to 500)		μA
REFERENCE VOLTAGE (Pin 2)					
LM131, LM131A, LM231, LM231A		1.76	1.89	2.02	V_{DC}
LM331, LM331A		1.70	1.89	2.08	V_{DC}
Stability vs Temperature			±60		ppm/°C
Stability vs Time, 1000 Hours			±0.1		%
LOGIC OUTPUT (Pin 3)					
V_{SAT}	$I = 5\ mA$		0.15	0.50	V
	$I = 3.2\ mA$ (2 TTL Loads), $T_{MIN} \leq T_A \leq T_{MAX}$		0.10	0.40	V
OFF Leakage			±0.05	1.0	μA
SUPPLY CURRENT					
LM131, LM131A, LM231,	$V_S = 5V$	2.0	3.0	4.0	mA
LM231A	$V_S = 40V$	2.5	4.0	6.0	mA
LM331, LM331A	$V_S = 5V$	1.5	3.0	6.0	mA
	$V_S = 40V$	2.0	4.0	8.0	mA

Note 1: All specifications apply in the circuit of *Figure 3*, with $4.0V \leq V_S \leq 40V$, unless otherwise noted.

Note 2: Nonlinearity is defined as the deviation of f_{OUT} from $V_{IN} \times (10\ kHz/-10\ V_{DC})$ when the circuit has been trimmed for zero error at 10 Hz and at 10 kHz, over the frequency range 1 Hz to 11 kHz. For the timing capacitor, C_T, use NPO ceramic, Teflon*, or polystyrene.

Functional Block Diagrams



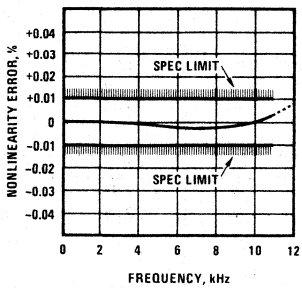
*Registered trademark of DuPont

FIGURE 1a

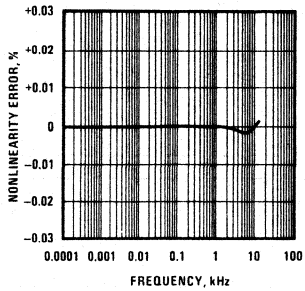
Typical Performance Characteristics

(All electrical characteristics apply for the circuit of *Figure 3*, unless otherwise noted.)

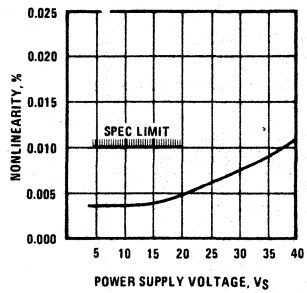
Nonlinearity Error, LM131 Family, as Precision V-to-F Converter *(Figure 3)*



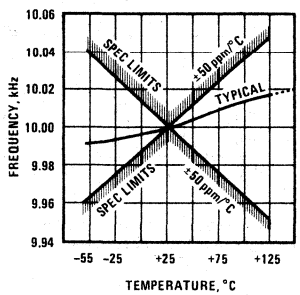
Nonlinearity Error, LM131 Family



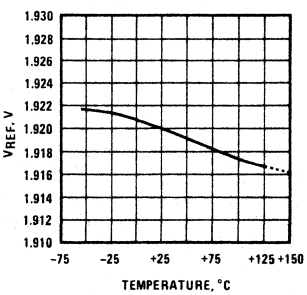
Nonlinearity vs Power Supply Voltage



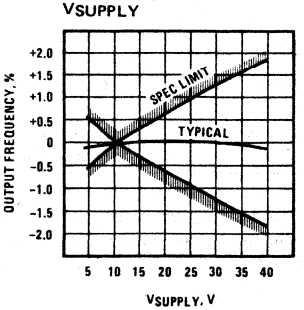
Frequency vs Temperature, LM131A



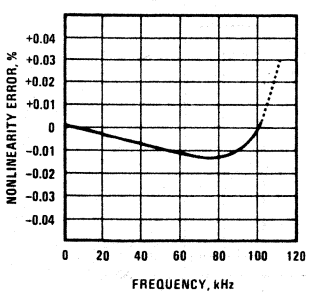
VREF vs Temperature, LM131A



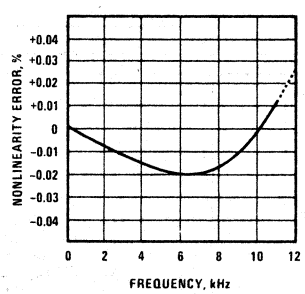
Output Frequency vs VSUPPLY



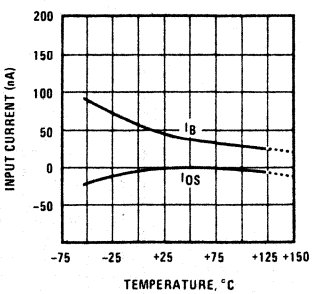
100kHz Nonlinearity Error, LM131 Family *(Figure 4)*



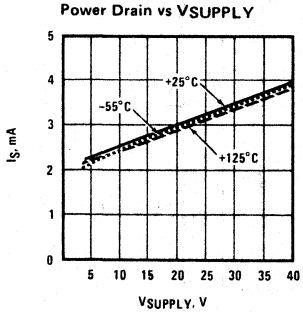
Nonlinearity Error, LM131 *(Figure 1)*



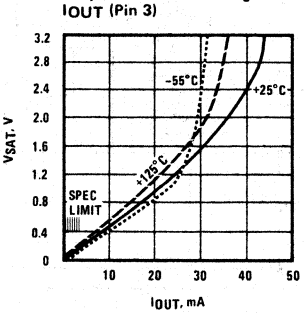
Input Current (Pins 6, 7) vs Temperature



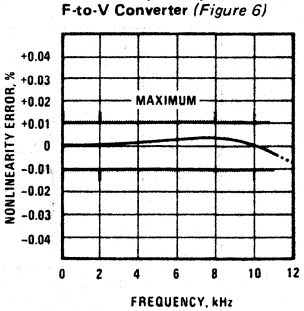
Power Drain vs VSUPPLY



Output Saturation Voltage vs IOUT (Pin 3)



Nonlinearity Error, Precision F-to-V Converter *(Figure 6)*



Typical Applications (Continued)

PRINCIPLES OF OPERATION OF A SIMPLIFIED VOLTAGE-TO-FREQUENCY CONVERTER

The LM131 is a monolithic circuit designed for accuracy and versatile operation when applied as a voltage-to-frequency (V-to-F) converter or as a frequency-to-voltage (F-to-V) converter. A simplified block diagram of the LM131 is shown in *Figure 2* and consists of a switched current source, input comparator, and 1-shot timer.

The operation of these blocks is best understood by going through the operating cycle of the basic V-to-F converter, *Figure 2*, which consists of the simplified block diagram of the LM131 and the various resistors and capacitors connected to it.

The voltage comparator compares a positive input voltage, V1, at pin 7 to the voltage, V_X, at pin 6. If V1 is greater, the comparator will trigger the 1-shot timer. The output of the timer will turn ON both the frequency output transistor and the switched current source for a period $t = 1.1\ R_tC_t$. During this period, the current i will flow out of the switched current source and provide a fixed amount of charge, $Q = i \times t$, into the capacitor, C_L. This will normally charge V_X up to a higher level than V1. At the end of the timing period, the current i will turn OFF, and the timer will reset itself.

Now there is no current flowing from pin 1, and the capacitor C_L will be gradually discharged by R_L until V_X falls to the level of V1. Then the comparator will trigger the timer and start another cycle.

The current flowing into C_L is exactly $I_{AVE} = i \times (1.1 \times R_tC_t) \times f$, and the current flowing out of C_L is exactly $V_X/R_L \cong V_{IN}/R_L$. If V_{IN} is doubled, the frequency will double to maintain this balance. Even a simple V-to-F converter can provide a frequency precisely proportional to its input voltage over a wide range of frequencies.

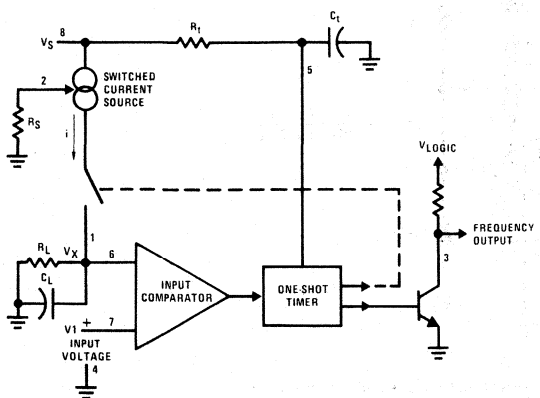


FIGURE 2. Simplified Block Diagram of Stand-Alone Voltage-to-Frequency Converter Showing LM131 and External Components

DETAIL OF OPERATION, FUNCTIONAL BLOCK DIAGRAM *(FIGURE 1a)*

The block diagram shows a band gap reference which provides a stable 1.9 V_{DC} output. This 1.9 V_{DC} is well regulated over a V_S range of 3.9V to 40V. It also has a flat, low temperature coefficient, and typically changes less than 1/2% over a 100°C temperature change.

The current pump circuit forces the voltage at pin 2 to be at 1.9V, and causes a current $i = 1.90V/R_S$ to flow. For $R_S = 14k$, $i = 135\ \mu A$. The precision current reflector provides a current equal to i to the current switch. The current switch switches the current to pin 1 or to ground depending on the state of the R_S flip-flop.

The timing function consists of an R_S flip-flop, and a timer comparator connected to the external R_tC_t network. When the input comparator detects a voltage at pin 7 higher than pin 6, it sets the R_S flip-flop which turns ON the current switch and the output driver transistor. When the voltage at pin 5 rises to 2/3 V_{CC}, the timer comparator causes the R_S flip-flop to reset. The reset transistor is then turned ON and the current switch is turned OFF.

However, if the input comparator still detects pin 7 higher than pin 6 when pin 5 crosses 2/3 V_{CC}, the flip-flop will not be reset, and the current at pin 1 will continue to flow, in its attempt to make the voltage at pin 6 higher than pin 7. This condition will usually apply under start-up conditions or in the case of an overload voltage at signal input. It should be noted that during this sort of overload, the output frequency will be 0; as soon as the signal is restored to the working range, the output frequency will be resumed.

The output driver transistor acts to saturate pin 3 with an ON resistance of about 50Ω. In case of overvoltage, the output current is actively limited to less than 50 mA.

The voltage at pin 2 is regulated at 1.90 V_{DC} for all values of i between 10 μA to 500 μA. It can be used as a voltage reference for other components, but care must be taken to ensure that current is not taken from it which could reduce the accuracy of the converter.

PRINCIPLES OF OPERATION OF BASIC VOLTAGE-TO-FREQUENCY CONVERTER *(FIGURE 1)*

The simple stand-alone V-to-F converter shown in *Figure 1* includes all the basic circuitry of *Figure 2* plus a few components for improved performance.

A resistor, $R_{IN} = 100\ k\Omega \pm 10\%$, has been added in the path to pin 7, so that the bias current at pin 7 (−80 nA typical) will cancel the effect of the bias current at pin 6 and help provide minimum frequency offset.

The resistance R_S at pin 2 is made up of a 12 kΩ fixed resistor plus a 5 kΩ (cermet, preferably) gain adjust rheostat. The function of this adjustment is to trim out the gain tolerance of the LM131, and the tolerance of R_t, R_L and C_t. For best results, all the components

Typical Applications (Continued)

should be stable low-temperature-coefficient components, such as metal-film resistors. The capacitor should have low dielectric absorption; depending on the temperature characteristics desired, NPO ceramic, polystyrene, Teflon* or polypropylene are best suited.

A capacitor is added from pin 7 to ground to act as a filter for V_{IN}. A value of 0.01 μF to 0.1 μF will be adequate in most cases; however, in cases where better filtering is required, a 1 μF capacitor can be used. When the RC time constants are matched at pin 6 and pin 7, a voltage step at V_{IN} will cause a step change in f_{OUT}. If C_{IN} is much less than C_L, a step at V_{IN} may cause f_{OUT} to stop momentarily.

A 47Ω resistor, in series with the 1 μF C_L, is added to give hysteresis effect which helps the input comparator provide the excellent linearity (0.03% typical).

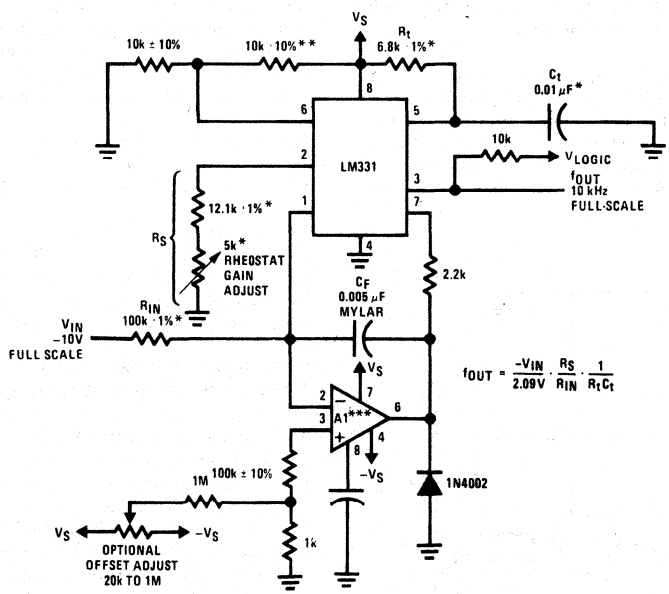
DETAIL OF OPERATION OF PRECISION V-TO-F CONVERTER *(FIGURE 3)*

In this circuit, integration is performed by using a conventional operational amplifier and feedback capacitor, C_F. When the integrator's output crosses the nominal threshold level at pin 6 of the LM131, the timing cycle is initiated. The average current fed into the op amp's summing point (pin 2) is i x (1.1 R_tC_t) x f which is perfectly balanced with $-V_{IN}/R_{IN}$. In this circuit, the voltage offset of the LM131 input comparator does not affect the offset or accuracy of the V-to-F converter as it does in the stand-alone V-to-F converter; nor does the LM131 bias current or offset current. Instead, the offset voltage and offset current of the operational amplifier are the only limits on how small the signal can be accurately converted. Since op amps with voltage offset well below 1 mV and offset currents well below 2 nA are available at low cost, this circuit is recommended for best accuracy for small signals. This circuit also responds immediately to any change of input signal (which a stand-alone circuit does not) so that the output frequency will be an accurate representation of V_{IN}, as quickly as 2 output pulses' spacing can be measured.

In the precision mode, excellent linearity is obtained because the current source (pin 1) is always at ground potential and that voltage does not vary with V_{IN} or f_{OUT}. (In the stand-alone V-to-F converter, a major cause of non-linearity is the output impedance at pin 1 which causes i to change as a function of V_{IN}).

The circuit of *Figure 4* operates in the same way as *Figure 3*, but with the necessary changes for high speed operation.

*Registered trademark of DuPont



*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8 V to 22 V, but must be 10 kΩ for V_S = 4.5 V to 8 V.

***Use low offset voltage and low offset current op amps for A1: recommended types LM108, LM308A, LF351B

FIGURE 3. Standard Test Circuit and Applications Circuit, Precision Voltage-to-Frequency Converter

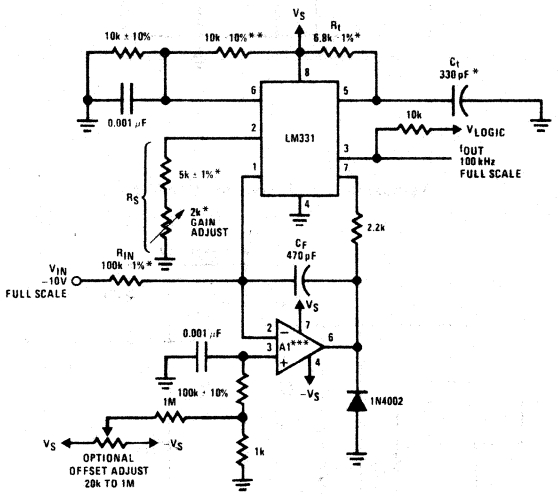
Typical Applications (Continued)

DETAILS OF OPERATION, FREQUENCY-TO-VOLTAGE CONVERTERS *(FIGURES 5 AND 6)*

In these applications, a pulse input at f_{IN} is differentiated by a C-R network and the negative-going edge at pin 6 causes the input comparator to trigger the timer circuit. Just as with a V-to-F converter, the average current flowing out of pin 1 is $I_{AVERAGE} = i \times (1.1\ R_tC_t) \times f$.

In the simple circuit of *Figure 5*, this current is filtered in the network R_L = 100 kΩ and 1 μF. The ripple will be less than 10 mV peak, but the response will be slow, with a 0.1 second time constant, and settling of 0.7 second to 0.1% accuracy.

In the precision circuit, an operational amplifier provides a buffered output and also acts as a 2-pole filter. The ripple will be less than 5 mV peak for all frequencies above 1 kHz, and the response time will be much quicker than in *Figure 5*. However, for input frequencies below 200 Hz, this circuit will have worse ripple than *Figure 5*. The engineering of the filter time-constants to get adequate response and small enough ripple simply requires a study of the compromises to be made. Inherently, V-to-F converter response can be fast, but F-to-V response can not.

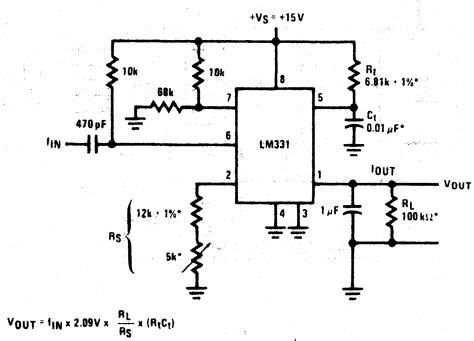


*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

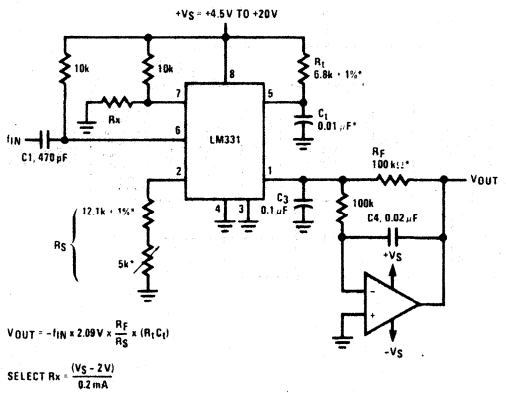
***Use low offset voltage and low offset current op amps for A1: recommended types LF351B or LF356.

FIGURE 4. Precision Voltage-to-Frequency Converter, 100 kHz Full-Scale, ±0.03% Non-Linearity



*Use stable components with low temperature coefficients.

FIGURE 5. Simple Frequency-to-Voltage Converter, 10 kHz Full-Scale, ±0.06% Non-Linearity

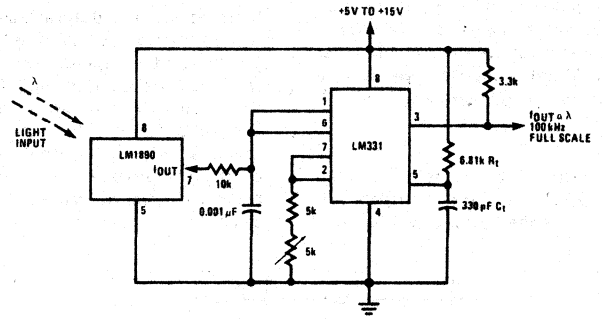


*Use stable components with low temperature coefficients.

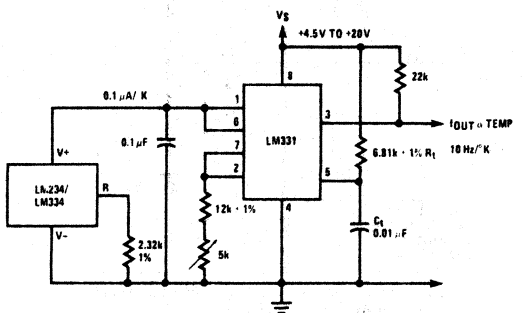
FIGURE 6. Precision Frequency-to-Voltage Converter, 10 kHz Full-Scale with 2-Pole Filter, ±0.01% Non-Linearity Maximum

Typical Applications (Continued)

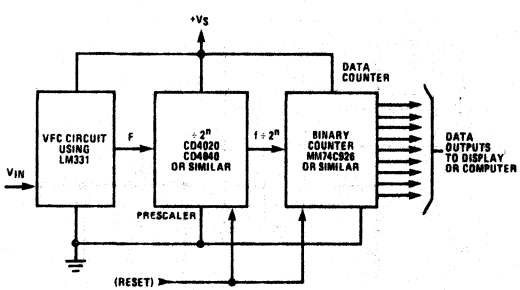
Light Intensity to Frequency Converter



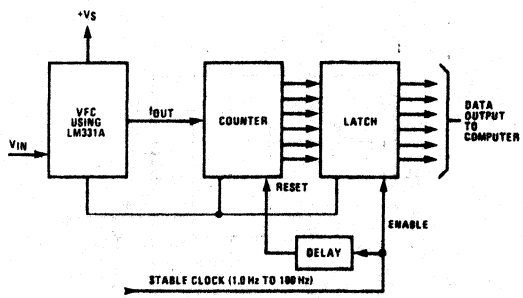
Temperature to Frequency Converter



Long-Term Digital Integrator Using VFC

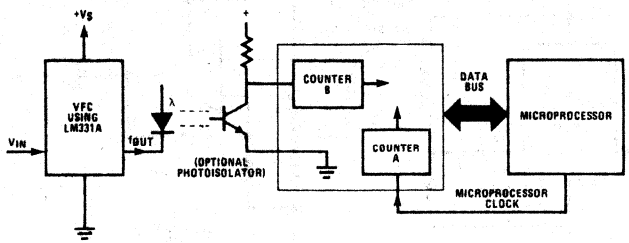


Basic Analog-to-Digital Converter Using Voltage-to-Frequency Converter

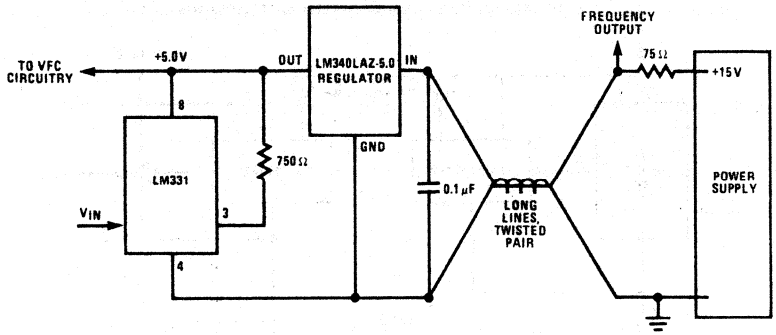


Typical Applications (Continued)

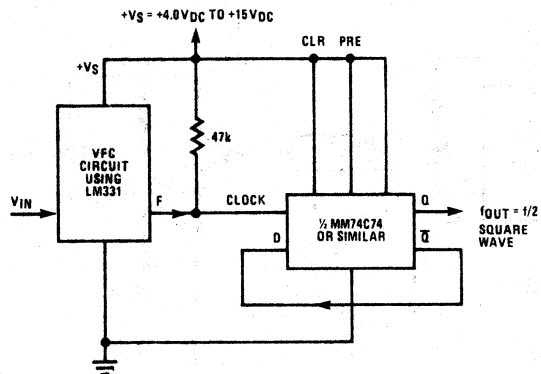
Analog-to-Digital Converter with Microprocessor



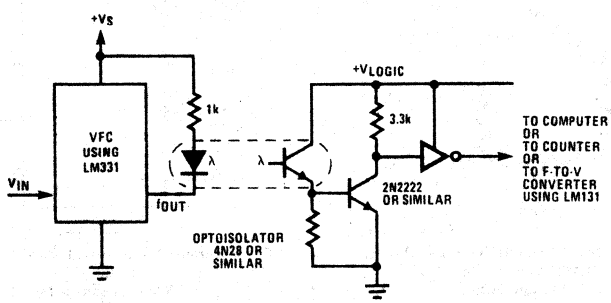
Remote Voltage-to-Frequency Converter with 2-Wire Transmitter and Receiver



Voltage-to-Frequency Converter with Square-Wave Output Using ÷2 Flip-Flop

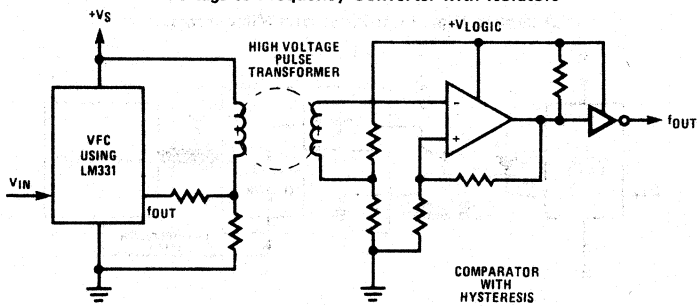


Voltage-to-Frequency Converter with Isolators

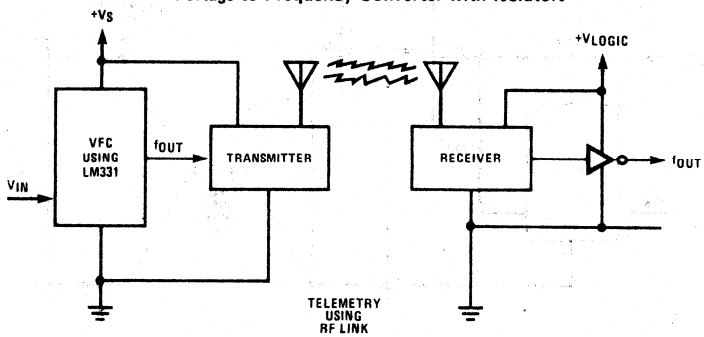


Typical Applications (Continued)

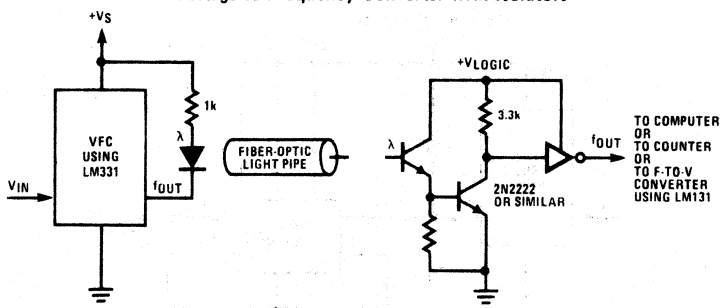
Voltage-to-Frequency Converter with Isolators



Voltage-to-Frequency Converter with Isolators

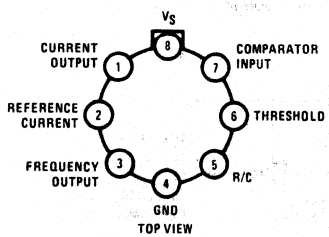


Voltage-to-Frequency Converter with Isolators



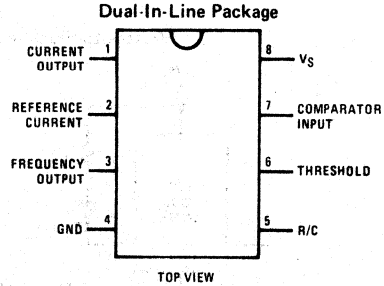
Connection Diagrams

Metal Can Package



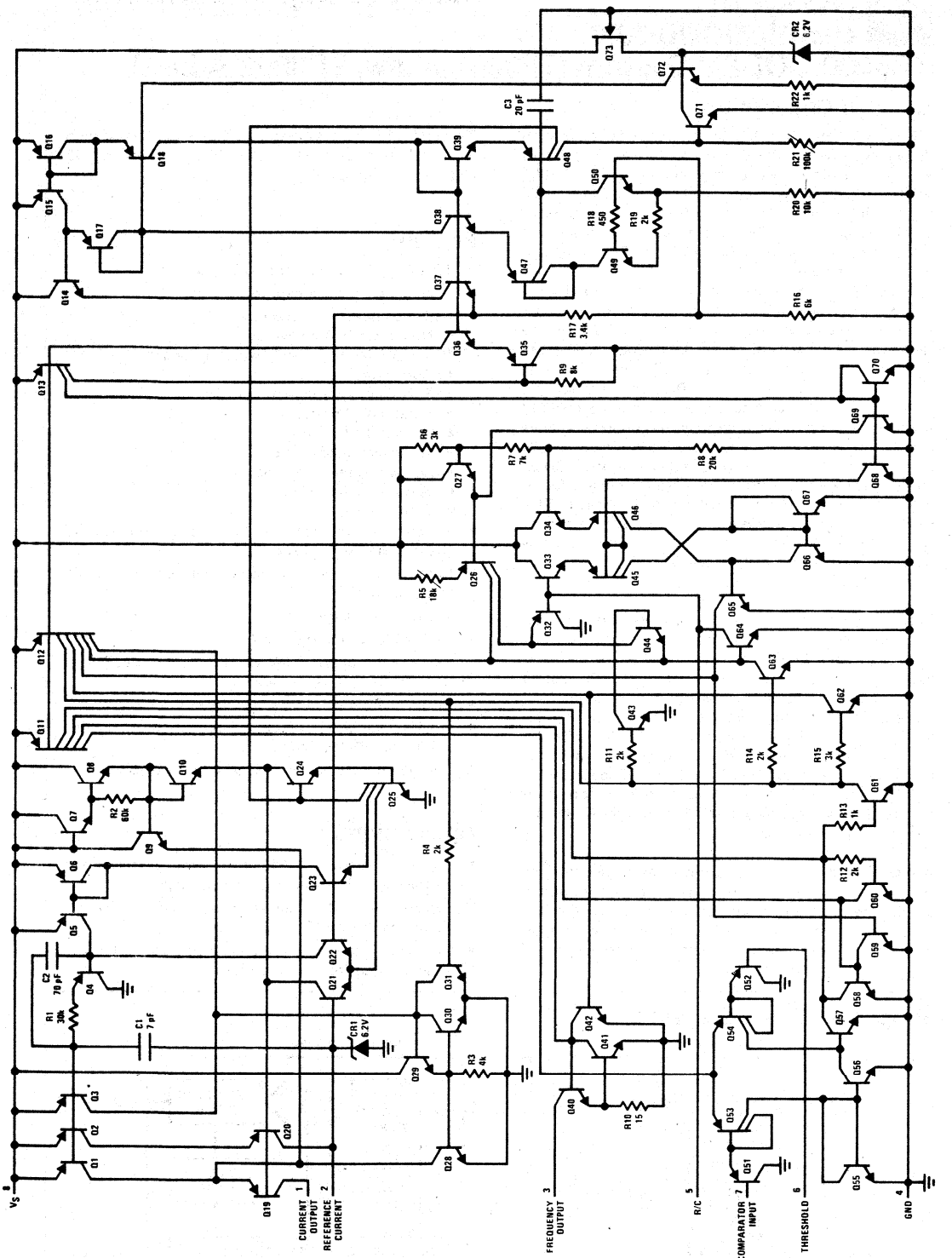
Order Number LM131AH, LM131H, LM231AH, LM231H, LM331AH or LM331H
See NS Package H08C

Dual-In-Line Package



Order Number LM231AN, LM231N, LM331AN, or LM331N
See NS Package N08B

Schematic Diagram



National Semiconductor

Analog-to-Digital Converters

TP3000 CODEC System (TP3001 μ-Law, TP3002 A-Law)

General Description

The TP3001 and TP3002 are Pulse Code Modulation (PCM) systems for the digital coding and decoding of analog signals in the voice frequency band. The TP3001 system utilizes μ-law coding of the analog signals while the TP3002 is an A-law system. Each system consists of 2 IC packages. The TP3001 system uses linear part LF3700 and CMOS part MM58100. The TP3002 system uses the same linear part and a different CMOS part (MM58150). Each system samples a filtered (300 Hz $\leq$ f $\leq$ 3.4 kHz) analog signal at an 8 kHz rate, converts this sampled voltage to an 8-bit companded digital code (μ-law or A-law) and loads this code into a high speed serial output buffer. This output buffer will operate at any speed between 64 and 2100 kilobits per second. Either system will also accept an incoming 8-bit PCM word (again, at any speed between 64 and 2100 kilobits per second) and will automatically interrupt the encode cycle to decode the PCM word and update the CODEC output sample and hold. After decoding, the systems will automatically return to the encoding cycle. This interrupt capability allows either CODEC system to send and receive PCM data asynchronously. These systems were specifically designed for low cost "per line" or per channel CODEC applications.

These IC's contain all the necessary elements required for a complete CODEC system—both the input and output sample and hold, comparator, stable voltage reference, non-linear D/A converter, successive approximation logic, control logic and digital input and output PCM buffers. The user must provide an input aliasing filter (300 Hz $\leq$ f $\leq$ 3.4 kHz) such as the AF133 or similar filter. The AF134, or similar filter, is available for use as the output filter (300 Hz $\leq$ f $\leq$ 3.4 kHz) which is needed to reject sidebands around 8 kHz and provide correction for the sinx/x frequency distortion introduced by the output sample and hold.

A special auto-zero circuit insures an extremely low idle channel noise and low crosstalk enhancement. During the decode cycle, the non-linear D/A converter is shifted 1/2 LSB, thereby achieving a typical signal to total distortion performance of at least 3 dB better than the D3 channel bank specifications.

The TP3001 system also includes 4 pins for the insertion and extraction of the signaling bits required for D3 channel bank operation.

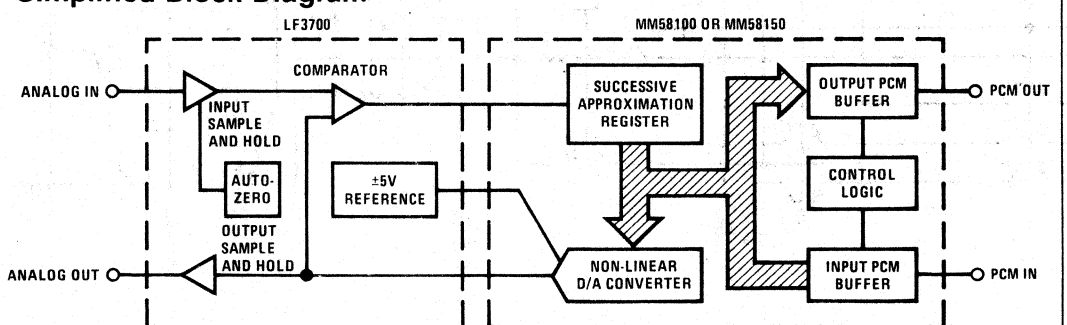
Features

- TP3001 uses the standard μ-255 code
- TP3002 uses the standard A-law code
- Each 2-chip system includes:
  - Non-linear D/A converter
  - Voltage reference with excellent long term stability
  - Comparator
  - Successive approximation logic
  - Input digital buffer
  - Output digital buffer
  - Input sample and hold
  - Output sample and hold
  - Auto-zero circuit
  - Control logic
- TP3001 system meets or exceeds all relevant D3 channel bank specifications
- Both systems meet or exceed all relevant CCITT specifications
- Analog input range of ±5V
- Analog output range of ±5V
- Input and output PCM words can be clocked at 64 to 2100 kilobits per second
- Incoming PCM word may be asynchronous
- Provision for the insertion and extraction of signaling bits in the TP3001 system
- Open drain PCM out for TRI-STATE® capability

Applications

- Use with digital switching systems in telephone central office or private branch exchange
- Replace 24 or 32-channel shared CODEC in telephone channel bank
- Use to digitize voice and similar analog signals for low noise transmission and reception

Simplified Block Diagram



Absolute Maximum Ratings

V^+ to Gnd	15V
V^- to Gnd	−15V
Voltage at Any Pin Except Digital Inputs or Digital Outputs	V^+ to V^-
Voltage at Any Digital Input or Output	−0.3 to +5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$V^+ = 12V$, $V^- = -12V$, $V_{EE} = -12V$ (Note 4) over operating temperature range, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Distortion	Method 1:				
TP3001 or TP3002 Either Encoding or Decoding	A Suitable Noise Signal Applied to the Coder Input Between −55 dBm0 and −3 dBm0 (Refer to CCITT Rec. G712, Paragraph 9, Method 1), *(Figure 4)*		2		dB Above the CCITT Limits Shown in *Figure 1.*
	Method 2: Measured with C Message Weighting Filter, 1020 Hz Input Signal				
	0 dBm0 to −30 dBm0	36			dB
	−40 dBm0	30			dB
	−45 dBm0	25			dB
	(Figure 5)				
Gain Tracking Error	Method 1:				
TP3001 or TP3002 Either Encoding or Decoding	Deviation From Gain at −10 dBm0 A Suitable Noise Signal Applied to the Coder Input Between −60 dBm0 and −10 dBm0 (Refer to CCITT Rec. G712, Paragraph 11, Method 1, *(Figure 4)*				Within Limits Shown in *Figure 2* (Note that *Figure 2* is 1/2 of the Limits Set By CCITT.)
	Method 2: Deviation From Gain at 0 dBm0 1020 Hz Input Signal				
	3 dBm0 to −37 dBm0	−0.25		+0.25	dB
	−37 dBm0 to −50 dBm0	−0.50		+0.50	dB
	(Figure 6)				
Idle Channel Noise	Input Terminated with 600Ω				
TP3001	*(Figure 7)*		12		dBrnc0
TP3002			−72		dBm0p
Single Frequency Distortion	1020 Hz Input Signal at 0 dBm0, *(Figure 8)*			−40	dBm0
Reference Voltage	(Note 1)	5.25	5.50	5.75	V
Temperature Coefficient of Reference Voltage			±1.5		mV/°C
Decoder 0 dBm0 Output Level	(Note 1)	2.58	2.70	2.82	Vrms
Intrachannel Crosstalk					
Go-to-Return Crosstalk	Level at Decoder Output Due to a 0 dBm0 Signal Being Encoded *(Figure 9)*		−62		dBm0
Return-to-Go Crosstalk	Level at Encoder Output (Measured Via Independent Decoder) Due to a 0 dBm0 Signal Being Decoded *(Figure 10)*		−70		dBm0

Electrical Characteristics (Continued)

$V^+ = 12V$, $V^- = -12V$, $V_{EE} = -12V$ (Note 4) over operating temperature range, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Interchannel Crosstalk (TP3001 Only)	Level at Decoder Output When a −80 dBm0 Signal is Applied to Encoder Input *(Figure 11)*		−83		dBm0
Analog Output Frequency Response	$300 \leq f \leq 3.4$ kHz		±0.05		dB Deviation From Theoretical sinx/x Response *(Figure 3)*
Logical "1" Input Voltage	(Note 5)	4.0			V
Logical "1" Input Current	Digital $V_{IN} = 5V$			1	μA
Logical "0" Input Voltage				0.8	V
Logical "0" Input Current	Digital $V_{IN} = 0V$			−1	μA
Master Clock Frequency, F_C	For Proper Operation: Duty Cycle = 50% ±10%		128		kHz
Input and Output PCM Buffer Clocks (F_{bo} and F_{bi})	F_o and F_i = 8 kHz F_{bo}, F_{bi} Duty Cycle = 40–60%	64		2100	kHz
Propagation Delay F_{bo} to Valid PCM Out		50	150	250	ns
PCM Out Pin Capacitance			4		pF
PCM Out Fall Time	1 kΩ Resistor to V_{DD} 100 pF Capacitor to V_{SS}		50	150	ns
System Power Dissipation	F_{bo}, F_{bi} = 1.544 MHz		250	300	mW
Shutdown Mode (LF3701 Only)	Pin 3 at Logic High		10	20	mW

Note 1: The relationship between the digital coding and the relative audio signal level is fixed as follows: a sine wave of 1 kHz and a nominal level of 0 dBm0 should be present at the audio output of the decoder when the appropriate character sequence shown below is applied to the decoder input.

TP3001 SYSTEM μ-LAW							
MSB	2	3	4	5	6	7	LSB
0	0	0	1	1	1	1	0
0	0	0	0	1	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	1	1	1	0
1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	1	1	1	0

TP3002 SYSTEM A-LAW							
MSB	2	3	4	5	6	7	LSB
0	0	1	1	0	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	0	0
1	0	1	1	0	1	0	0
1	0	1	0	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	0	0

The resulting theoretical load capacity (T_{MAX}) is 3.17 dBm0 for the TP3001 system (μ-law) and 3.14 dBm0 for the TP3002 system (A-law).

Note 2: The PCM transmit filter must be AC coupled to the CODEC and a resistor of 24 kΩ or lower must be tied between analog in and analog ground. CODEC input impedance will then appear as 24 kΩ.

Note 3: PCM OUT and S_i are open drain outputs and will require external pull-up resistors to +6V maximum. 1 kΩ for PCM OUT and 10 kΩ for S_i are recommended when $F_{bo} = F_{bi} = 2.1$ MHz.

Note 4: Special care must be taken to assure that the substrate to ground pn junction is never forward biased. In cases where the negative power must be open circuited, it is recommended that a high current diode (1 amp Schottky) be placed between V^- and ground. It is further recommended that the power supply turn-on sequence be as follows: V^- or ground first, followed by V^+. Power supply turn-off should reverse the procedure.

Note 5: For TTL or LS compatibility, external pull-up resistors are required between the digital inputs and the TTL or LS logic power supply.

System Description (Refer to block diagrams)

The master clock for the system is F_C and must be run at 128 kHz which divides the 125 μs (1/8 kHz) time-frame into 16 time slots. The rising edge of the Output Sync (F_O) initiates the encoding cycle. The Input Sample and Hold Control (IN S/H CNTL) will go high for 19 μs thereby causing the input sample and hold to acquire a new input analog voltage. This acquired analog voltage is presented to a UNITY GAIN BUFFER located on the CMOS chip and then forwarded to the positive comparator input on the linear chip. The successive approximation will then begin. The SUCCESSIVE APPROXIMATION REGISTER will first load a zero code into the NON-LINEAR D/A CONVERTER. The output of the D/A converter goes to a second unity gain buffer and then to the negative input of the comparator on the linear chip. The comparator will then decide if the sampled analog voltage is positive or negative. If the analog input voltage is positive, the CONTROL LOGIC will pull the polarity control line high, which in turn will cause the voltage reference on the linear chip to deliver a positive reference voltage to the NON-LINEAR D/A CONVERTER. Conversely, if the analog input voltage is negative, a negative reference voltage will be applied to the NON-LINEAR D/A. The successive approximation will turn ON the second bit to the NON-LINEAR D/A CONVERTER and a decision is made to either leave that bit ON, or turn it OFF. The logic will then turn ON the third bit and make a decision to leave that bit ON or turn it OFF. In this way, the analog input voltage can be converted into the standard 8-bit μ-law or A-law code in 8 clock cycles.

At the end of the encode cycle the 8-bit code is loaded into the OUTPUT PCM BUFFER. The word is read out serially (MSB first) on PCM OUT by the Output Clock (F_{bo}) and the Output Sync (F_O).

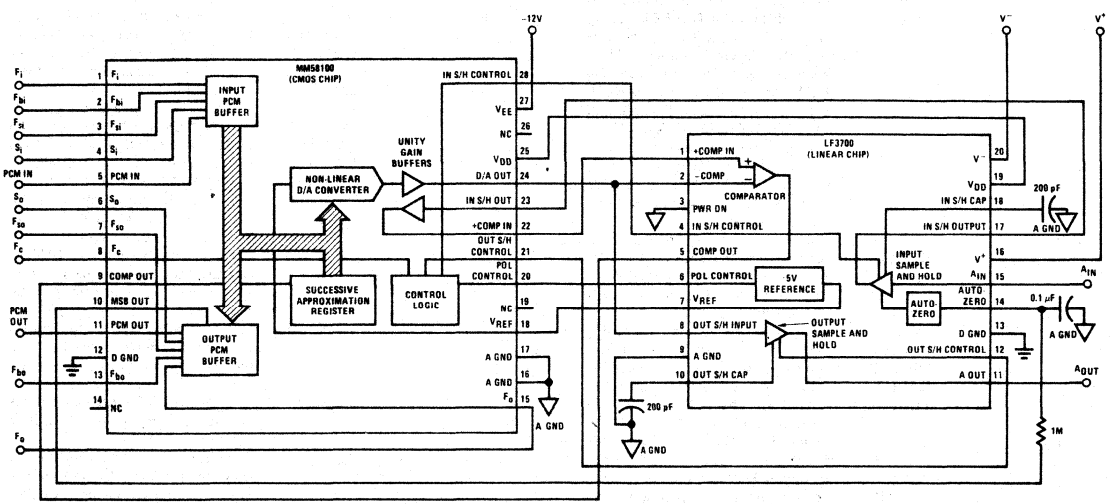
The incoming PCM word is read in serially (MSB first) on the PCM IN line by the Input Clock (F_{bi}) and the Input Sync (F_i). When the input word has been read in and F_i goes low, the system will immediately switch over to the decode mode. The current status of the successive approximation is temporarily stored while the decode word is delivered to the NON-LINEAR D/A CONVERTER. During decode, the ladder is shifted the required 1/2 LSB to minimize distortion. The CONTROL LOGIC will then raise the Output S/H Control line so that the Output Sample and Hold will acquire this new output voltage. After 4 clock cycles the circuit will return to the encode mode. The analog output of the system will therefore be a staircase type output with the associated sinx/x frequency distortion, *(Figure 3)*.

The system incorporates an AUTO-ZERO circuit to ensure a low DC offset for the encoding process, and very low idle channel noise. The encoded MSB (the sign bit) is latched on the MSB OUT pin. This signal then is fed to a simple external low pass RC filter (with a time constant of about 100 ms to 1 sec) and then to the AUTO-ZERO pin on the LF3700. The DC voltage on this pin will adjust the offset of the input sample and hold to correct for any offset voltage in the encoding path. This will also correct for up to ±20 mV DC offset voltage present in the analog input signal. This scheme simply forces equal numbers of positive and negative voltages over the long term.

There are 4 pins available in the TP3001 system for the insertion and extraction of signaling bits. The operation of these pins is covered in the timing diagrams.

System Block Diagrams

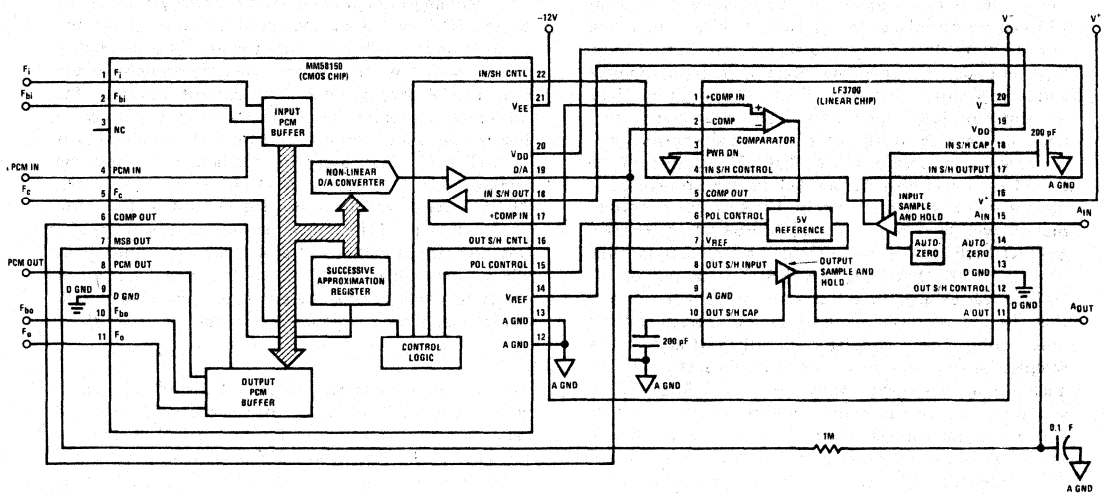
TP3001 System



Note. Pin 3 of the LF3700 should be connected to analog ground. Pin 3 of the LF3701 is a power down control; logic high (5V) is the power down standby mode for the TP3000 systems.

System Block Diagrams (Continued)

TP3002 System



Note. Pin 3 of the LF3700 should be connected to analog ground. Pin 3 of the LF3701 is a power down control; logic high (5V) is the power down standby mode for the TP3000 systems.

Ordering Information

SYSTEM	ORDER LINEAR PART: D20A	AND CMOS PART: D24A
TP3001 (μ-law)	LF3700D	MM58100D
TP3002 (A-law)	LF3700D	MM58150D

Description of Pin Functions

CMOS PIN FUNCTIONS:

MM58100 PIN NO.	MM58150 PIN NO.	NAME	FUNCTION
1	1	F_i (INPUT SYNC)	When this line goes high, the data on the PCM IN line is shifted into the INPUT PCM BUFFER by F_{bi} (INPUT CLOCK). This line must be high for 8 clock pulses of F_{bi}. When F_i goes low, the incoming PCM word is loaded into the NON-LINEAR D/A CONVERTER and the OUTPUT SAMPLE AND HOLD is placed in the acquire mode. During decode, the D/A converter is shifted 1/2 LSB. After the decode is complete, the successive approximation will resume.
2	2	F_{bi} (INPUT PCM CLOCK)	The leading edges of this clock will serially shift the data on the PCM IN line into the INPUT PCM BUFFER when the F_i (INPUT SYNC) line is high.
3	–	F_{si} (MM58100 INPUT SIGNALING ENABLE)	When this line is high, the falling edge of F_i (INPUT SYNC) will transfer the LSB on the incoming PCM word to S_i (INPUT SIGNALING BIT). The PCM word is then decoded as a 7-bit code.
4	–	S_i (MM58100 INPUT SIGNALING BIT)	When F_{si} (INPUT SIGNALING ENABLE) is high, the LSB of the incoming PCM word is transferred to this line and latched by the falling edge of F_i (INPUT SYNC). An external pull-up resistor of 10k to the digital positive supply is required.

CMOS PIN FUNCTIONS: (Continued)

MM58100 PIN NO.	MM58150 PIN NO.	NAME	FUNCTION
5	4	PCM IN	The incoming PCM word is received on this line.
6	–	S_o (MM58100 OUTPUT SIGNALING BIT)	When the F_{so} (OUTPUT SIGNALING ENABLE) line is high the LSB of the PCM word in the OUTPUT BUFFER is replaced by the logic state on this line.
7	–	F_{so} (MM58100 OUTPUT SIGNALING ENABLE)	When this line is high and F_o (OUTPUT SYNC) is low, the logic level on S_o (OUTPUT SIGNALING BIT) is transferred to the LSB of the OUTPUT PCM BUFFER.
8	5	F_c (MASTER CLOCK)	This is the principal clock of the CODEC system. All CODEC functions with the exception of F_i (INPUT SYNC) and F_{bi} (INPUT CLOCK) are synchronized to F_c. This clock frequency should be 128 kHz.
9	6	COMP OUT	This is the output of the analog comparator which is used in the successive approximation conversion.
10	7	MSB OUT	The encoded MSB appears on this line for use in the AUTO ZERO function.
11	8	PCM OUT	The result of the digital encoding is available on this line. A 1k external resistor to the digital positive supply is required.
12	9	D GND (DIGITAL (GND)	All digital signals should be referenced to this line.

Description of Pin Functions (Continued)

CMOS PIN FUNCTIONS: (Continued)

MM58100 PIN NO.	MM58150 PIN NO.	NAME	FUNCTION
13	10	F_{bo} (OUTPUT PCM CLOCK)	The falling edges of this clock will serially shift the PCM word in the PCM OUTPUT BUFFER to the PCM OUT line.
14	–	No Connection	
15	11	F_o (OUTPUT SYNC)	When this line goes high, the output PCM word can be shifted out by F_{bo} (OUTPUT CLOCK). This line must be high for 8 clock pulses of F_{bo}. When F_o goes high, the following sequence is initiated: the INPUT SAMPLE AND HOLD first acquires the ANALOG IN voltage and a successive approximation conversion is made on that voltage using the NON-LINEAR D/A CONVERTER and the COMPARATOR. The resulting 8-bit PCM word is then loaded into the OUTPUT PCM BUFFER.
16	12	A GND (ANALOG GROUND)	All analog signals should be referenced to this line.
17	13	A GND (ANALOG GROUND)	All analog signals should be referenced to this line.
18	14	V_{REF}	This is the $+V_{REF}$ or the $-V_{REF}$ for the NON-LINEAR D/A CONVERTER.
19	–	No Connection	
20	15	POL CNTL (POLARITY CONTROL)	This is the digital command for $+V_{REF}$ or $-V_{REF}$.
21	16	OUT S/H CNTL (OUTPUT SAMPLE AND HOLD CONTROL)	This is the digital command for the OUTPUT SAMPLE AND HOLD to acquire a new voltage.
22	17	+COMP IN (NON-INVERTING COMPARATOR INPUT)	This is the output of the buffer amplifier for the input sample and hold. This is connected to the +COMP IN pin on the linear chip.
23	18	IN S/H OUT (OUTPUT OF THE INPUT SAMPLE AND HOLD)	This is the input of the buffer amplifier for the input sample and hold. This is connected to the output of the input sample and hold on the linear chip.
24	19	D/A OUT	This is the output voltage of the NON-LINEAR D/A CONVERTER.
25	20	V_{DD}	This is the positive voltage supply for the digital chip which is provided by the analog chip.
26	–	No Connection	
27	21	V_{EE}	This is the negative supply voltage for the digital chip (−12V).
28	22	IN S/H CNTL (INPUT SAMPLE AND HOLD CONTROL)	This is the digital command for the INPUT SAMPLE AND HOLD to acquire a new voltage.

LINEAR PIN FUNCTIONS:

LF3700 PIN NO.	NAME	FUNCTION
1	+COMP IN (NON-INVERTING COMPARATOR INPUT)	This is tied to the +COMP IN pin on the CMOS chip.
2	–COMP IN (INVERTING COMPARATOR INPUT)	This is tied to the D/A OUT pin on the CMOS chip and the OUTPUT SAMPLE AND HOLD INPUT pin on the linear chip.
3	POWER DOWN	Connect to Analog Gnd – LF3700 (LF3701 see note System Block Diagram).
4	IN S/H CNTL (INPUT SAMPLE AND HOLD CONTROL)	This is tied to the IN S/H CNTL pin on the CMOS chip.
5	COMP OUT (COMPARATOR OUTPUT)	This is tied to the COMP OUT pin on the CMOS chip.
6	POL CNTL (POLARITY CONTROL)	This is tied to the POL CNTL pin on the CMOS chip.
7	V_{REF}	This is tied to V_{REF} on the CMOS chip.
8	OUT S/H INPUT (INPUT TO OUTPUT SAMPLE AND HOLD)	This is the analog input to the OUTPUT SAMPLE AND HOLD. This should be connected to the D/A OUT pin on the CMOS chip and the inverting comparator input pin on the linear chip.
9	A GND (ANALOG GROUND)	All analog signals should be referenced to this line.
10	OUT S/H CAP (OUTPUT SAMPLE AND HOLD CAPACITOR)	A low leakage, 200 pF capacitor should be connected from this line to ANALOG GROUND.
11	A OUT (ANALOG OUT)	This is the output of the OUTPUT SAMPLE AND HOLD.
12	OUT S/H CNTL (OUTPUT SAMPLE AND HOLD CONTROL)	This is tied to the OUT S/H CNTL pin on the CMOS chip.
13	D GND (DIGITAL GROUND)	All digital signals should be referenced to this line.
14	AUTO Z (AUTO ZERO)	This is connected to the MSB OUT line of the CMOS chip after an external low pass filter.
15	A IN (ANALOG IN)	This is the appropriately filtered analog input.
16	V^+	This is the positive supply voltage for the analog chip.
17	IN S/H OUTPUT (OUTPUT OF INPUT SAMPLE AND HOLD)	This is the analog output voltage of the INPUT SAMPLE AND HOLD. This is tied to the IN S/H OUT pin on the CMOS chip.
18	IN S/H CAP (INPUT SAMPLE AND HOLD CAPACITOR)	A low leakage, 200 pF capacitor should be connected from this line to analog ground.
19	V_{DD}	This is the positive supply voltage for the CMOS chip. This is tied to V_{DD} on the CMOS chip.
20	V^-	This is the negative supply for the linear chip.

Typical Performance Characteristics

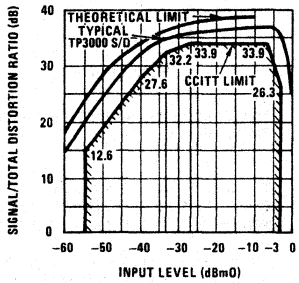


FIGURE 1. Typical Signal/ Total Distortion Ratio as a Function of Input Level with a White Noise Source

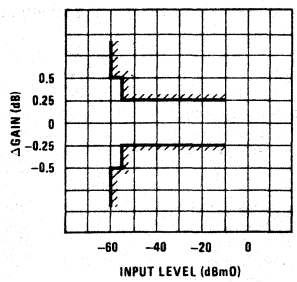


FIGURE 2. Maximum Gain Tracking Error (ΔGain) as a Function of Input Level with a White Noise Source

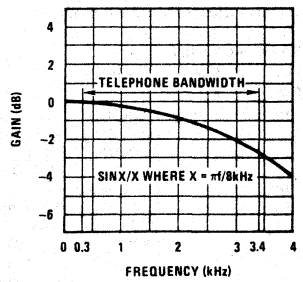
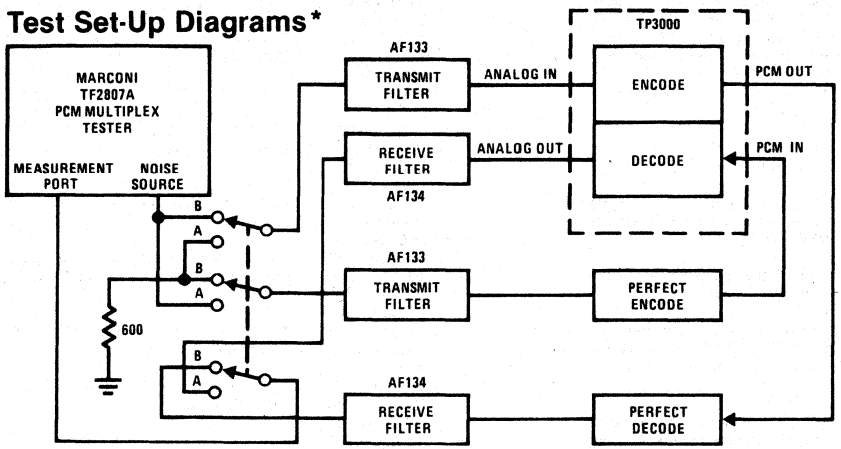


FIGURE 3. Output sinx/x Frequency Response

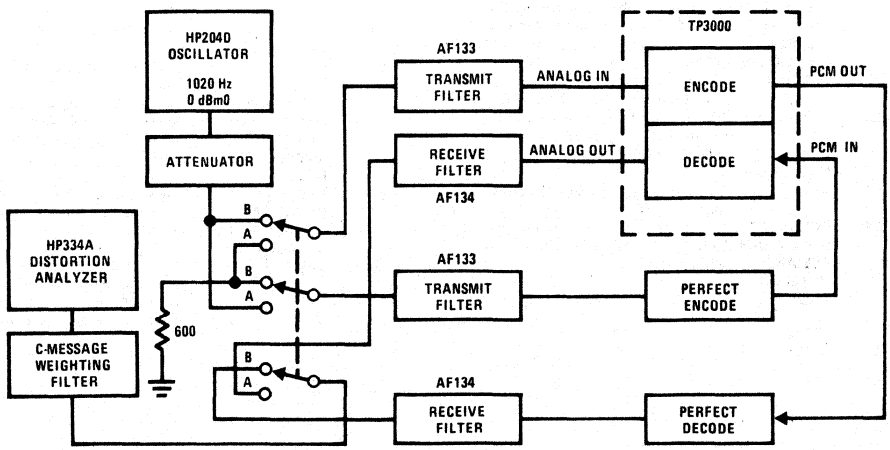
Test Set-Up Diagrams*



The Marconi TF2807A's noise output has a probability distribution of amplitude approximating a Gaussian distribution which is band limited to conform with the latest CCITT recommendations.

Switch position A — Perfect encode; decode TP3000
Switch position B — Encode TP3000; perfect decode

FIGURE 4. Test Set-Up for Signal-to-Distortion and Gain Tracking Using a Noise Source

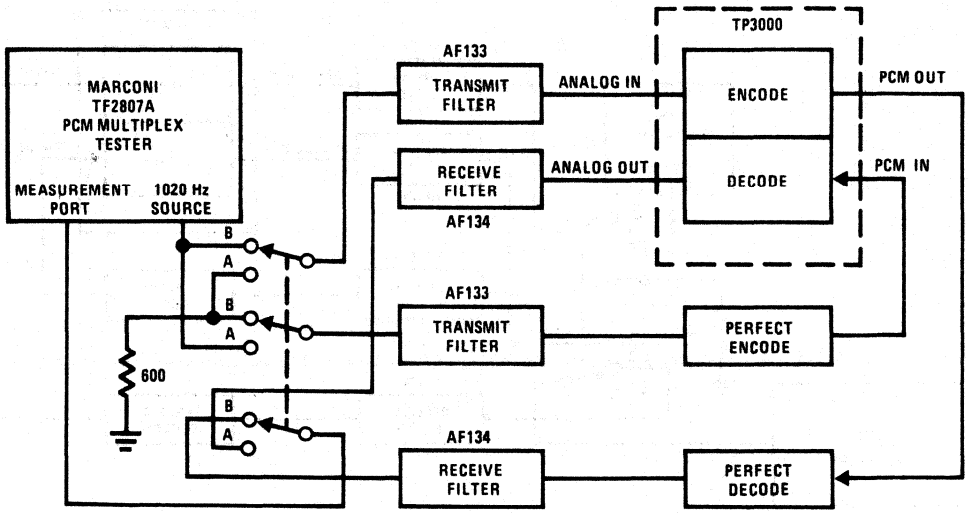


Switch position A — Perfect encode; decode TP3000
Switch position B — Encode TP3000; perfect decode

FIGURE 5. Test Set-Up for Signal-to-Distortion Using a 1020 Hz Signal

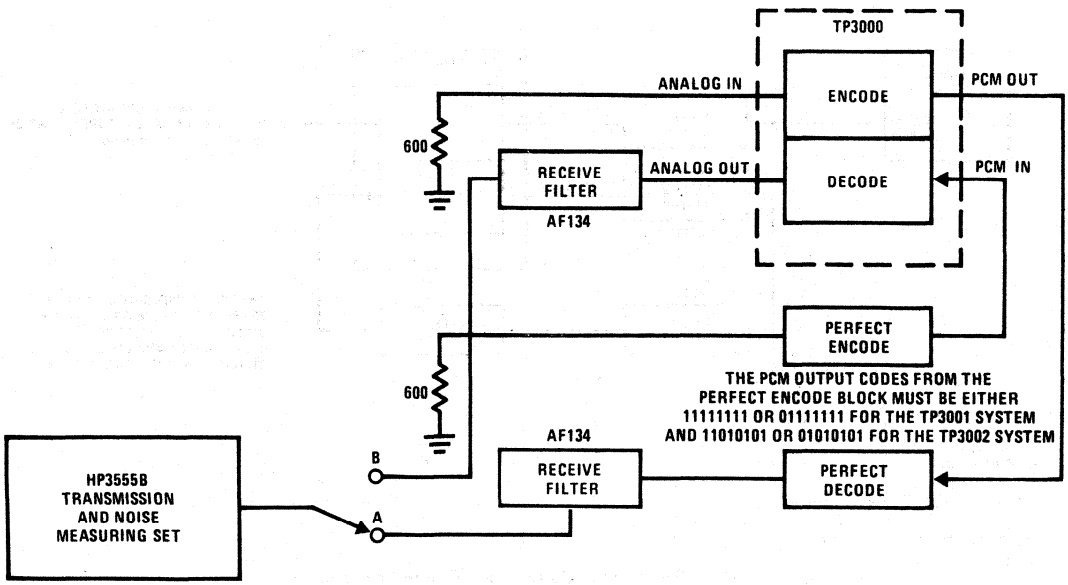
*Perfect encode or decode is μ-law when testing TP3001 and A-law when testing TP3002

Test Set-Up Diagrams* (Continued)



Switch position A - Perfect encode; decode TP3000
Switch position B – Encode TP3000; perfect decode

FIGURE 6. Test Set-Up for Gain Tracking Using 1020 Hz Signal

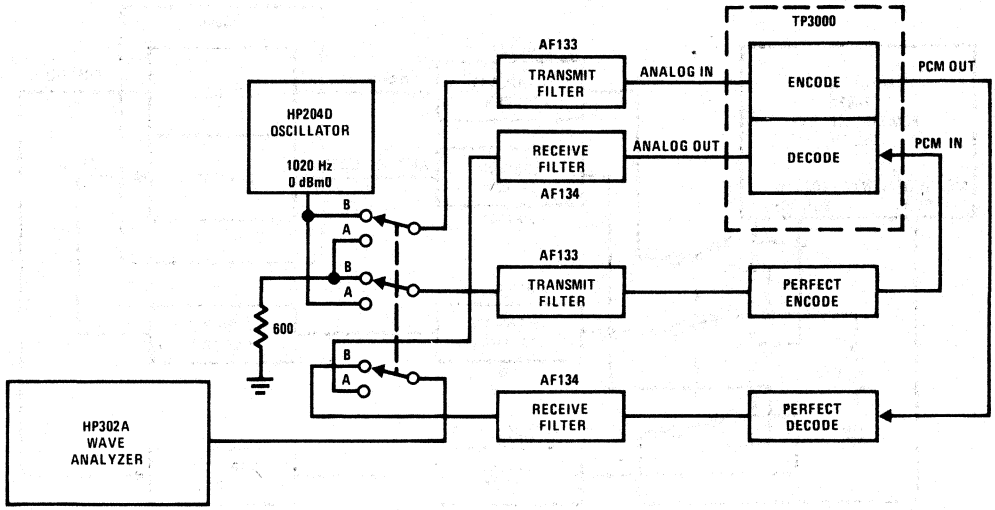


Determine the 0 dBm0 level on the HP3555B and then measure the idle channel noise with the HP3555B in the C-MSG-mode. The noise in dBrnc0 is 90 dBm0-A, where A is the idle channel noise measurement down from the 0 level (in dB).

FIGURE 7. Test Set-Up for Idle Channel Noise

*Perfect encode or decode is μ-law when testing TP3001 and A-law when testing TP3002

Test Set-Up Diagrams* (Continued)



The output at any frequency (except 1020 Hz) should be at least 40 dB down. The two frequencies of interest are the second and third harmonics (2040 Hz and 3060 Hz).

Switch position A -- Perfect encode; decode TP3000
Switch position B – Encode TP3000; perfect decode

FIGURE 8. Test Set-Up for Single Frequency Distortion

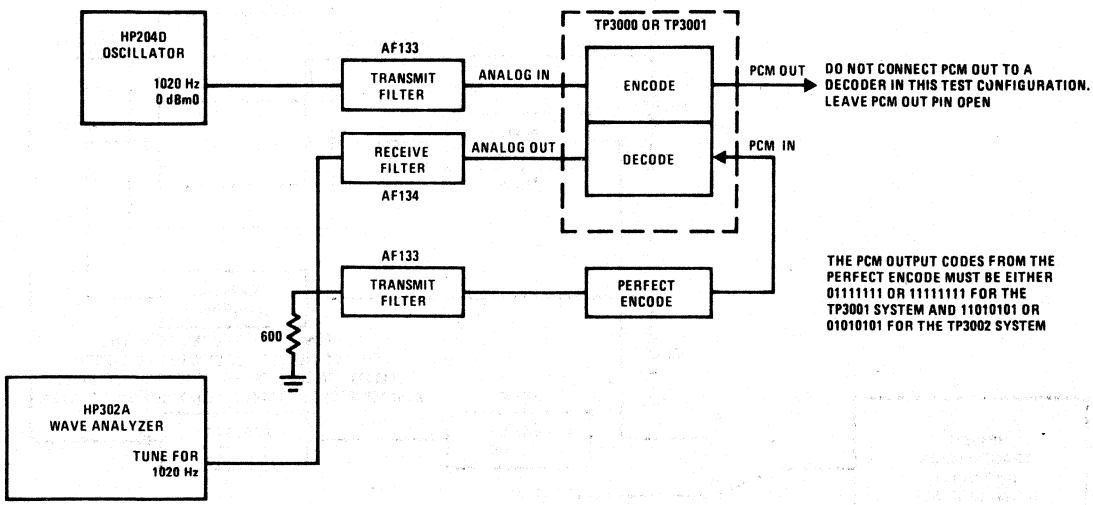


FIGURE 9. Test Set-Up for Go-to-Return Crosstalk

*Perfect encode or decode is μ-law when testing TP3001 and A-law when testing TP3002

Test Set-Up Diagrams* (Continued)

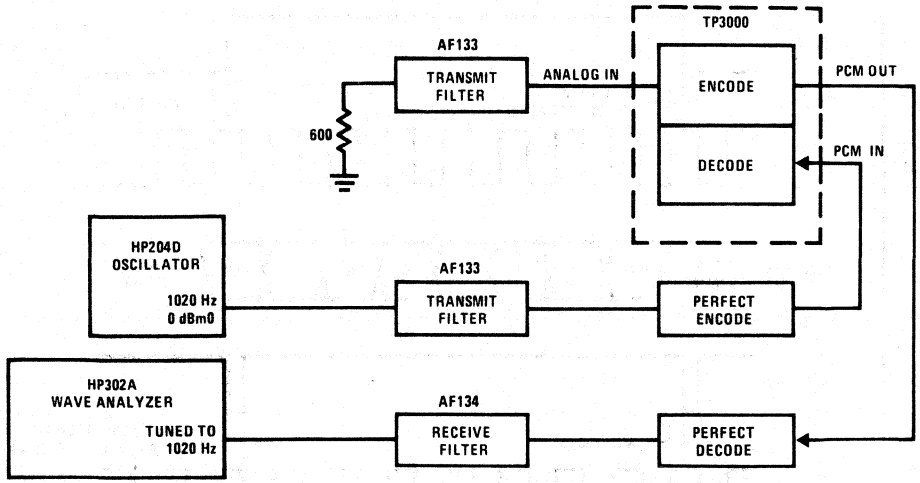
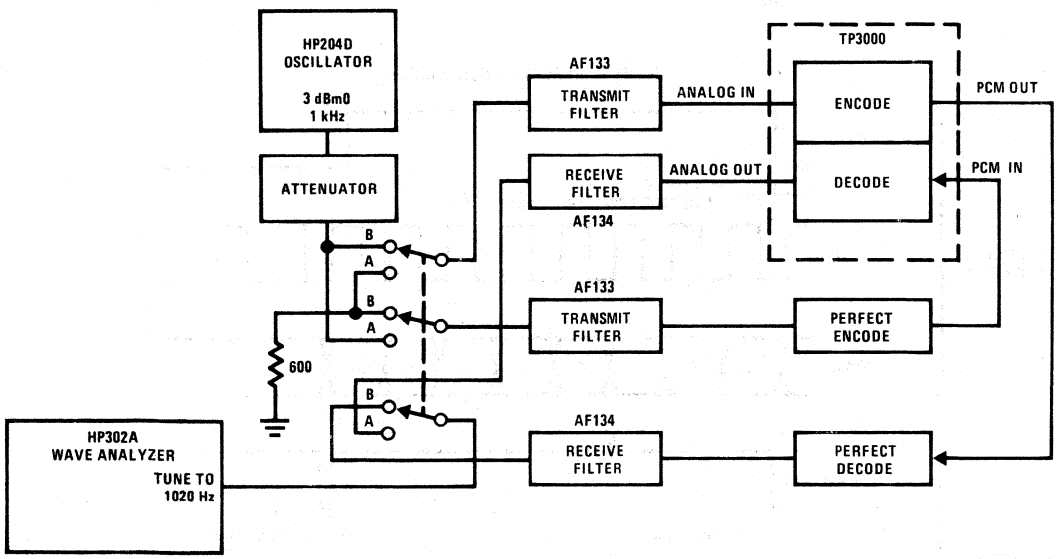


FIGURE 10. Test Set-Up for Return-to-Go Crosstalk



Switch position A — Perfect encode; decode TP3000
Switch position B — Encode TP3000; perfect decode

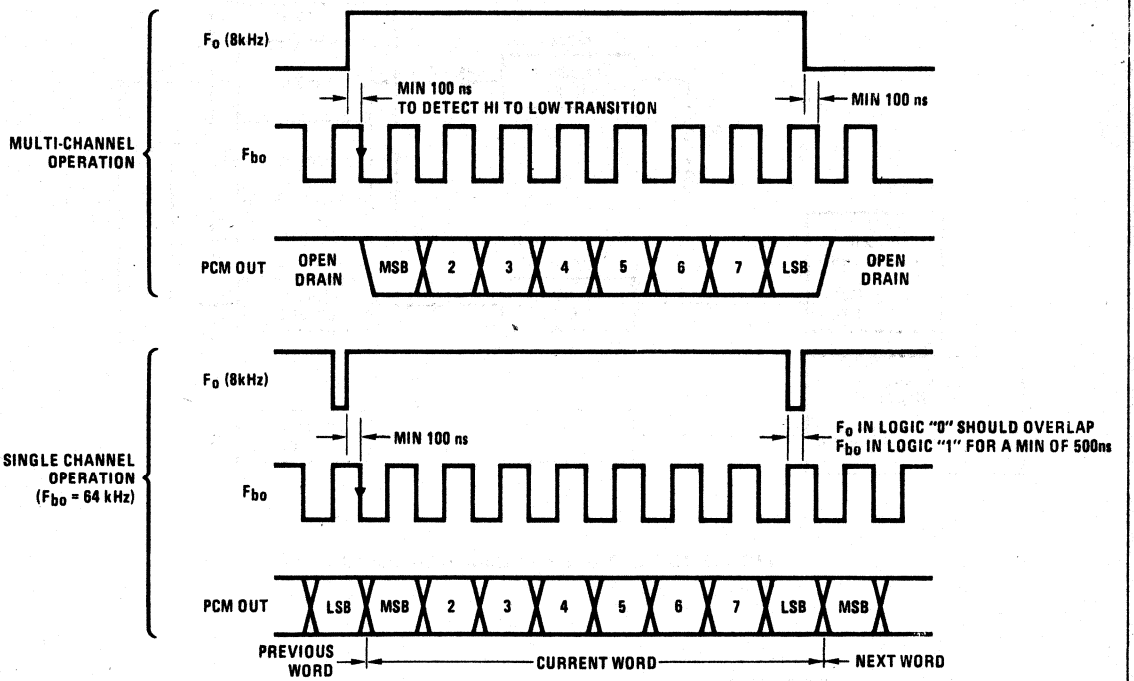
FIGURE 11. Test Set-Up for Interchannel Crosstalk

*Perfect encode or decode is μ-law when testing TP3001 and A-law when testing TP3002

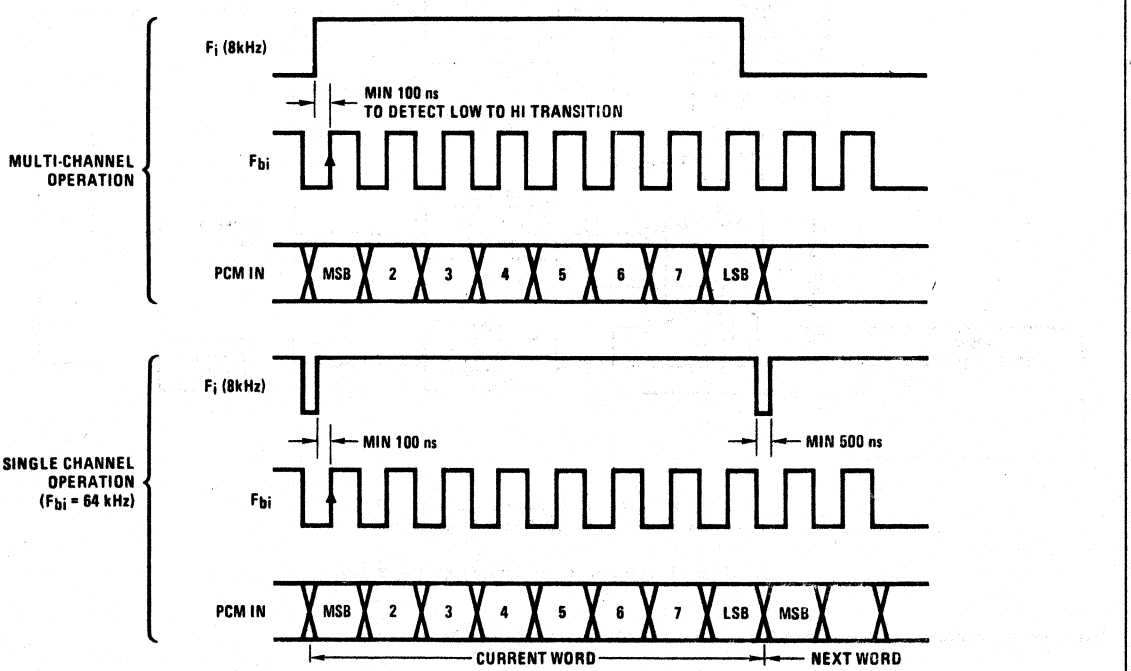
Timing Diagrams

SYSTEM TIMING

F_o, F_{bo} and PCM OUT Relationships



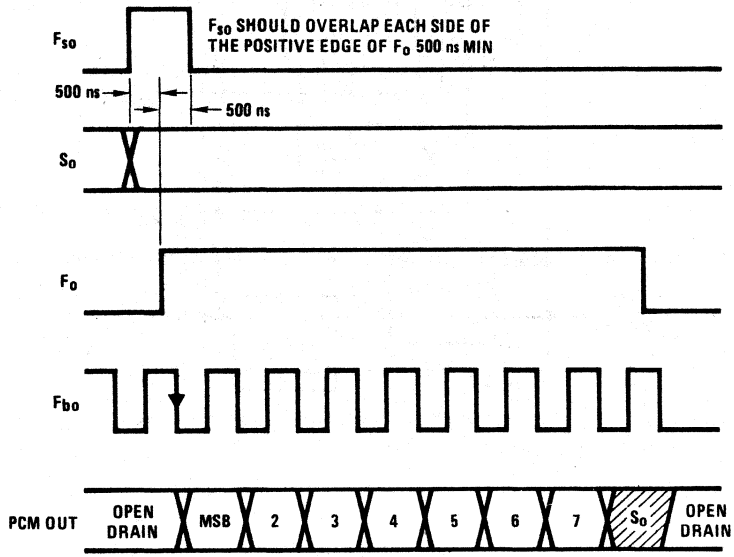
F_i, F_{bi} and PCM IN Relationships



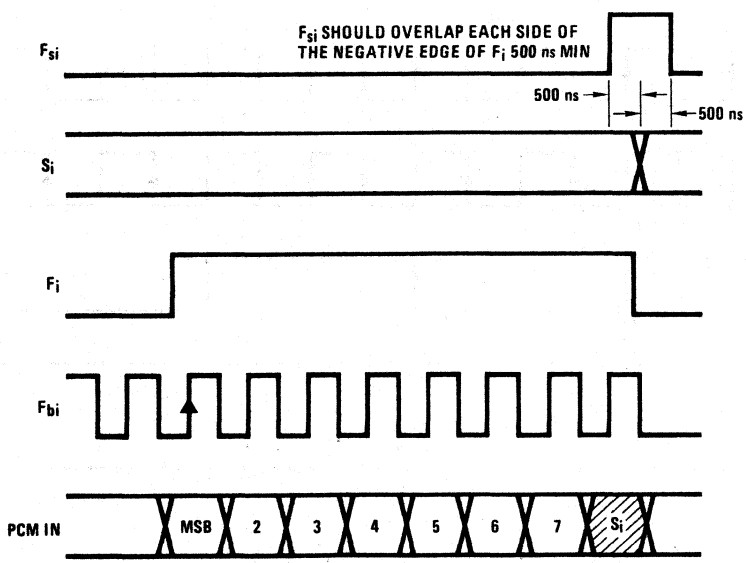
Timing Diagrams (Continued)

SIGNALING
(TP3001 Only)

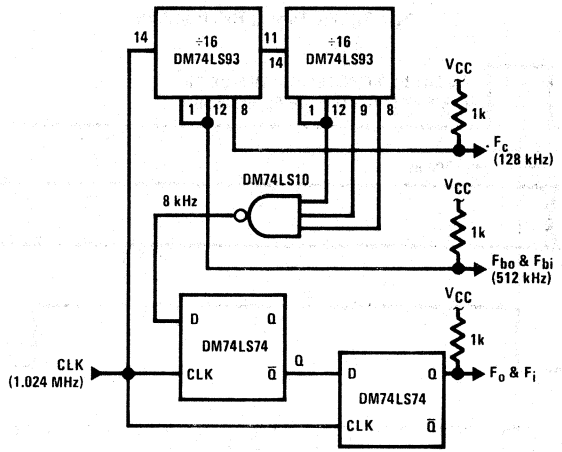
F_{so}, S_o, F_o Timing Relationships



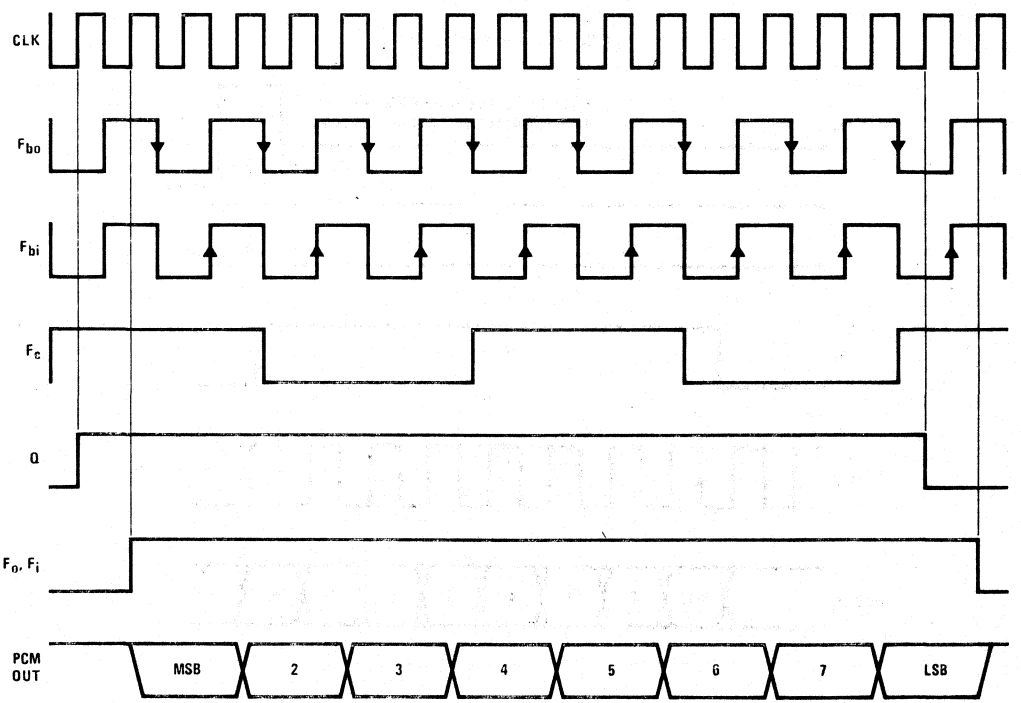
F_{si}, S_i, F_i Timing Relationships



Timing Generator



Timing Generator Outputs



Section 6

Analog-to-Digital Display (DVM)

6

Analog-to-Digital Display (DVM)

Section Contents

National Semiconductor

Analog-to-Digital Display (DVM)

ADD3501 3 1/2-Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3501 (MM74C935-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3501 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or -OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included on all 4 versions of this product.

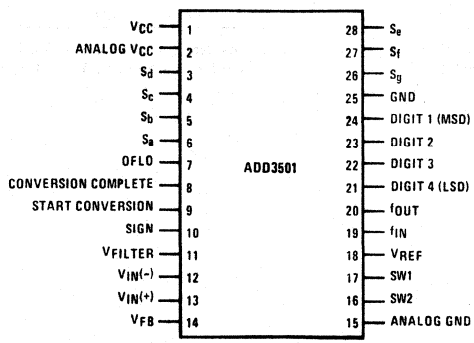
Features

- Operates from single 5V supply
- Converts 0V to ±1.999V
- Multiplexed 7-segment
- Drives segments directly
- No external precision component necessary
- Accuracy specified over temperature
- Medium speed — 200ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or -OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram



Order Number ADD3501CCN
See NS Package N28A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$
Package Dissipation at $T_A = 25°C$	800mW
derate at $\theta_{JA(MAX)} = 125°C$/Watt above $T_A = 25°C$	
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$

Electrical Characteristics $4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$, unless otherwise specified.

ADD3501

PARAMETER		CONDITIONS	MIN	TYP (2)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs except Digit Outputs)	$I_O = 1.1$ mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O = 0.7$ mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O = 50$ mA @ $T_J = 25°C$ $V_{CC} = 5V$ $I_O = 30$ mA @ $T_J = 100°C$	$V_{CC}-1.6$ $V_{CC}-1.6$	$V_{CC}-1.3$ $V_{CC}-1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs except Segment Outputs)	$I_O = 500\mu A$ (Digit Outputs) $I_O = 360\mu A$ (Conv. Complete, +/−, Oflo Outputs)	$V_{CC}-0.4$			V
I_{SOURCE}	Output Source Current (Digit Outputs)	$V_{OUT} = 1.0V$	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN} = 1.5V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN} = 0V$	−1.0			μA
I_{CC}	Supply Current	Segments and Digits Open		0.5	10	mA
	Oscillator Frequency			0.6/RC		kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/64,512$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/256$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32f_{MUX})$		sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

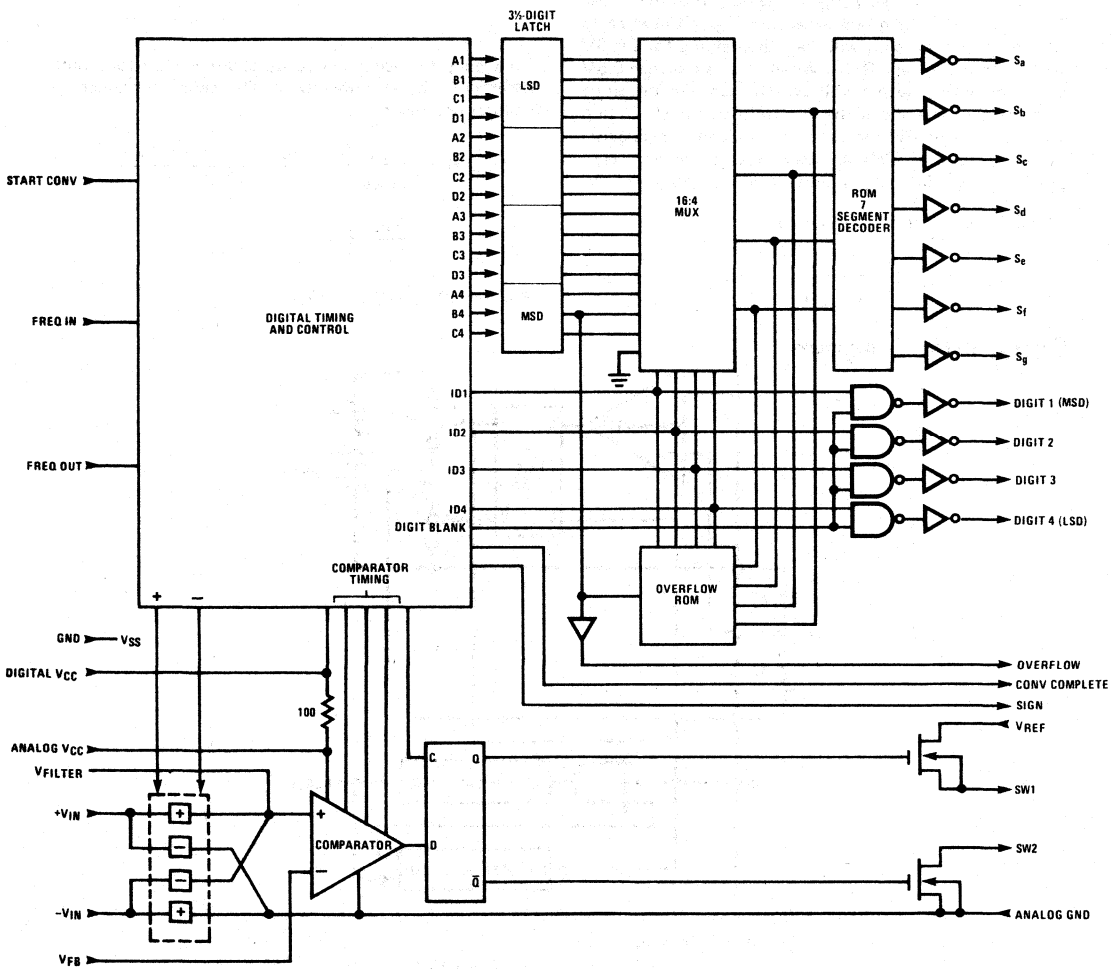
Note 2: All typicals given for $T_A = 25°C$.

Electrical Characteristics ADD3501

t_C = 5 conversions/second, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

Non-Linearity	V_{IN} = 0 - 2V Full Scale V_{IN} = 0 - 200mV Full Scale	-0.05	±0.025	+0.05	% of full scale
Quantization Error		-1		+0	counts
Offset Error, V_{IN} = 0V		-0.5	+1.5	+3	mV
Rollover Error		-0		+0	counts
Analog Input Current (V_{IN}+, V_{IN}-)	T_A = 25°C	-5	±0.5	+5	nA

Block Diagram



ADD3501 3½-Digit DVM Block Diagram

Theory of Operation

A schematic for the analog loop is shown in figure 1. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time V_{FB} will start discharging toward 0V with a time constant R_1C_1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\left(\frac{T_{ON}}{T_{ON}+T_{OFF}}\right) = V_{REF}(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}(\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}(\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{duty cycle}) \times (\text{clock})$$

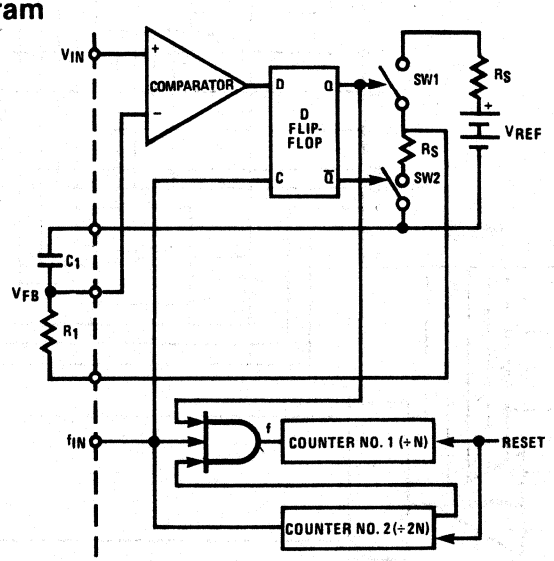
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(\text{clock})/N} = \frac{(\text{duty cycle}) \times (\text{clock})}{(\text{clock})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3501, N = 2000.

Schematic Diagram



$V_{IN} = V_{FB} = V_{REF} \times (\text{duty cycle})$

$f = (\text{duty cycle}) \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{(\text{duty cycle}) \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

Figure 1. Analog Loop Schematic
Pulse Modulation A/D Converter

General Information

The timing diagram, shown in figure 2, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 64,512 x $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 64 x $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way.

Internally the ADD3501 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in figure 3, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 x $1/f_{IN}$ and the minimum time is 256 x $1/f_{IN}$.

Timing Waveforms

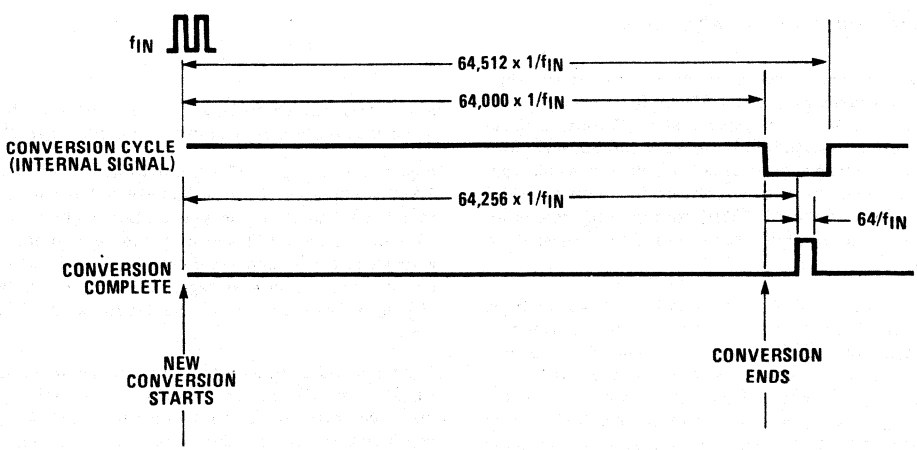


Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

Timing Waveforms (Continued)

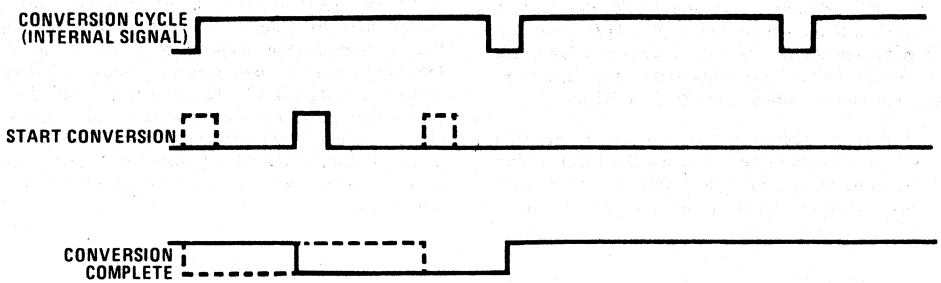


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3501 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3501 to minimize these problems but poor printed circuit layout can negate these features.

Figures 4, 5, and 6 show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators both function well and are shown in figures 4, 5, and 6. Adding more filtering than is shown will in general increase the jitter rather than decrease it. The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0V to 1.999V operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or – (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in figure 6.

Figures 5 and 6 show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0nA of leakage current will cause 0.1mV error ($1.0 \times 10^{-9}A \times 100k\Omega = 0.1mV$). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.

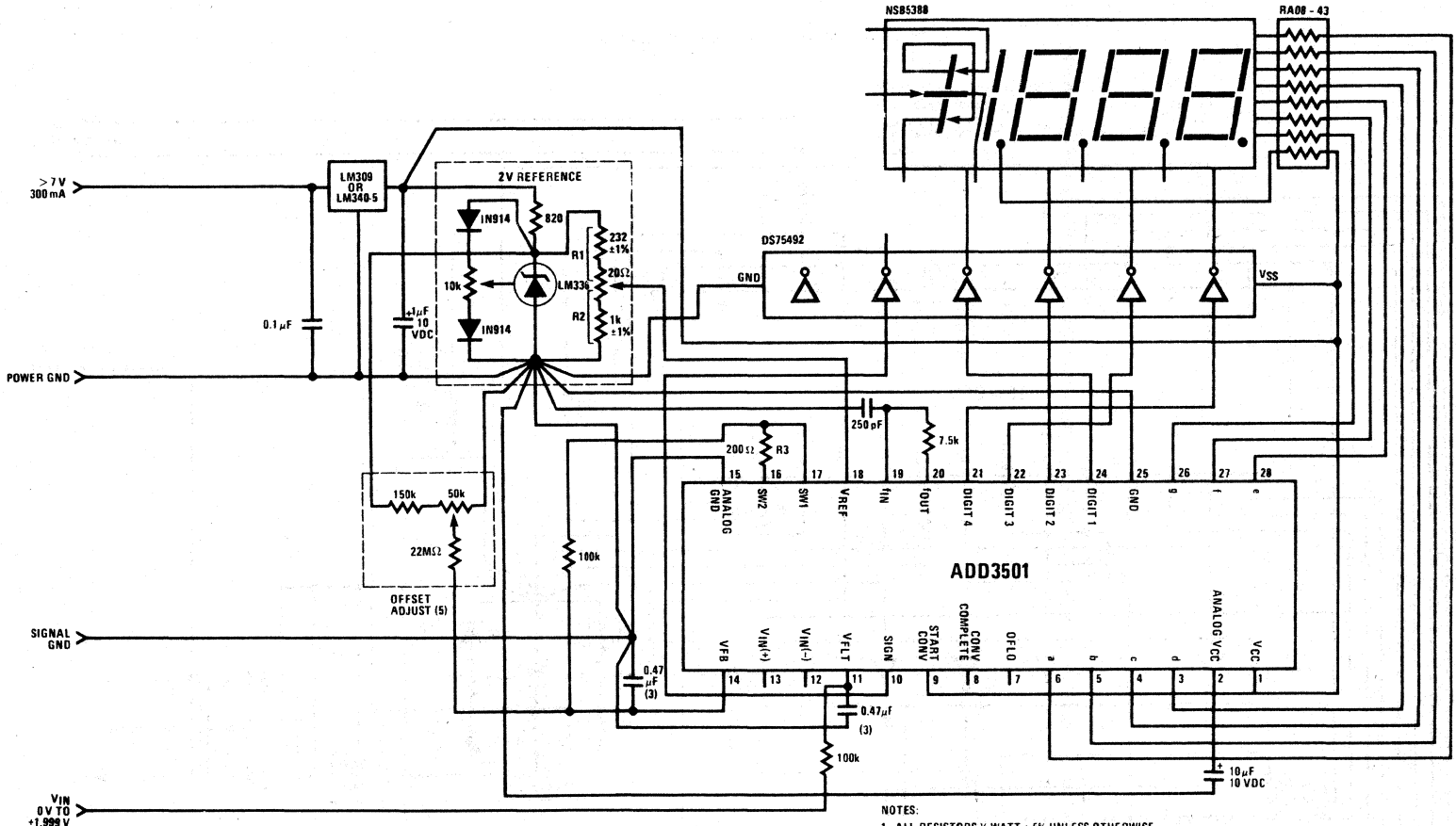


Figure 4. 3½-Digit DPM, +1.999 Volts Full Scale

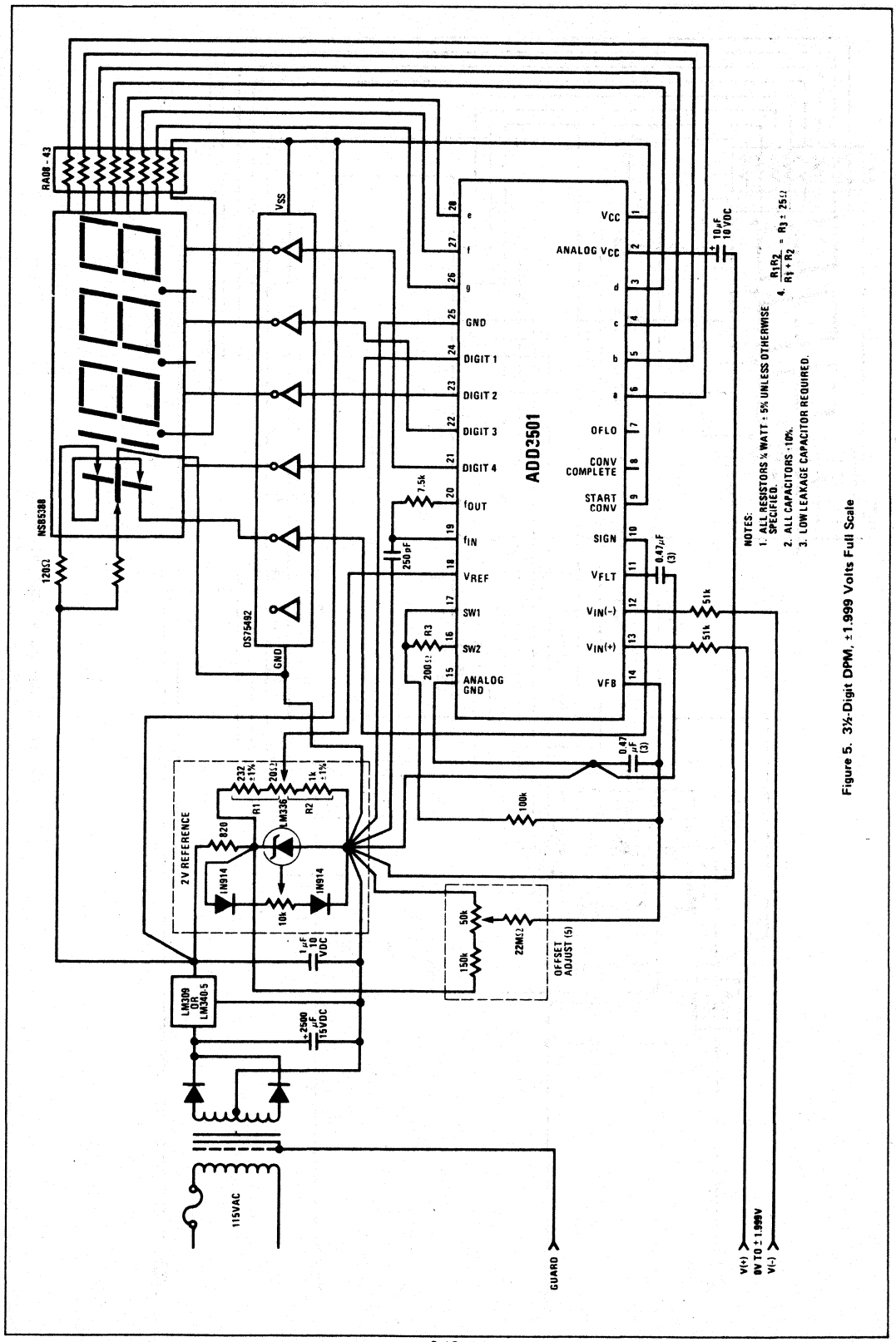
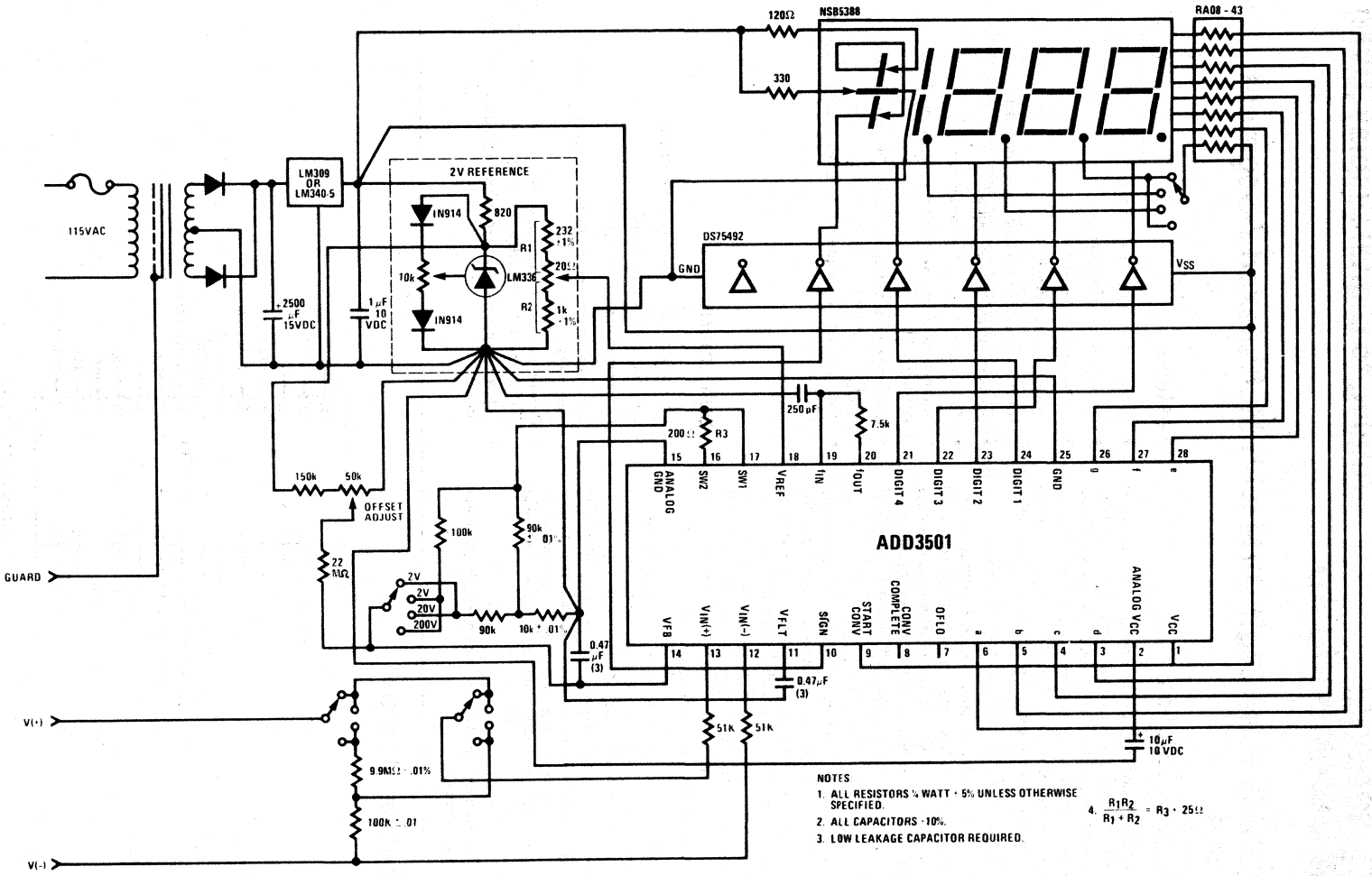


Figure 5. 3½-Digit DPM, ±1.999 Volts Full Scale



NOTES

1. ALL RESISTORS ¼ WATT ±5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$

Figure 6. 3½-Digit DVM, Four Decade, ±0.2 V, ±2 V, ±20 V and ±200 V Full Scale

National Semiconductor

Analog-to-Digital Display (DVM)

ADD3701 3 3/4-Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3701 (MM74C936-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5 V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3701 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or -OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included.

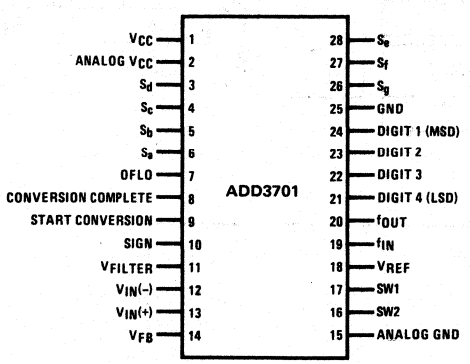
Features

- Operates from single 5 V supply
- Converts 0 to ±3999 counts
- Multiplexed 7-segment
- Drives segments directly
- No external precision components necessary
- Accuracy specified over temperature
- Medium speed — 400 ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or -OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers
- Indicators and displays requiring readout up to 3999 counts

Connection Diagram



Order Number ADD3701CCN
See NS Package N28A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin except Start Conversion	$-0.3V$ to $V_{CC} + 0.3V$
Voltage at Start Conversion	$-0.3V$ to $+15.0V$
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$
Package Dissipation at $T_A = 25°C$	800mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$

Electrical Characteristics ADD3701

$4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$, unless otherwise specified.

Parameter		Conditions	Min	Typ[2]	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs Except Digit Outputs)	$I_O = 1.1$ mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O = 0.7$ mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O = 50$ mA @ $T_J = 25°C$ $V_{CC}=5V$ $I_O = 30$ mA @ $T_J = 100°C$	$V_{CC} - 1.6$ $V_{CC} - 1.6$	$V_{CC} - 1.3$ $V_{CC} - 1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs Except Segment Outputs)	$I_O = 500\mu A$ (Digit Outputs) $I_O = 360\mu A$ (Conv. Complete, +/–, OFLO Outputs)	$V_{CC} - 0.4$			V
I_{SOURCE}	Output Source Current (Digit Outputs)	$V_{OUT} = 1.0V$	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN} = 15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN} = 0V$	-1.0			μA
I_{CC}	Supply Current	Segments and Digits Open		0.5	10	mA
	Oscillator Frequency			0.6/RC		kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/129,024$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/512$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32\,f_{MUX})$		seconds
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals given for $T_A = 25°$ C.

Note 3: Full scale = 4000 counts; therefore 0.025% of full scale = 1 count and 0.05% of full scale = 2 counts.

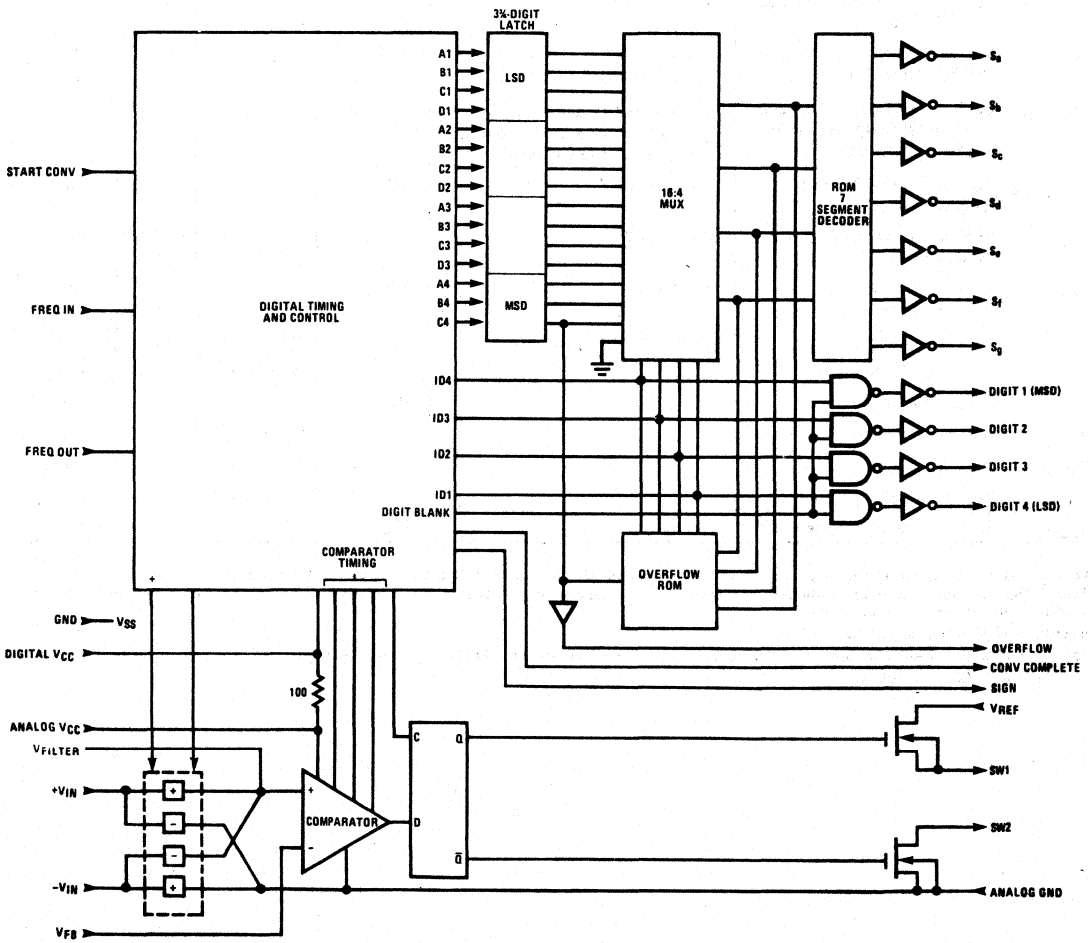
Note 4: For 2.000 Volts full scale, 1 mV = 2 counts.

Electrical Characteristics ADD3701

t_C = 2.5 conversions/second, 0°C ≤ T_A ≤ +70°C, unless otherwise specified.

Parameter	Conditions	Min	Typ[2]	Max	Units
Non-Linearity of Output Reading	V_{IN} = 0-2 V Full Scale V_{IN} = 0-200 mV Full Scale	-0.05	±0.025	+0.05	% full scale (Note 3)
Quantization Error		-1		+0	counts
Offset Error, V_{IN} = 0 V		-0.5	+1.5	+3	mV (Note 4)
Rollover Error		-0		+0	counts
Analog Input Current (V_{IN}+, V_{IN}-)	T_A = 25°C	-5	±1	+5	nA

Block Diagram



ADD3701 3¾-Digit DVM Block Diagram

Theory of Operation

A schematic for the analog loop is shown in figure 1. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0\,V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500 V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000 V) and V_{FB} will charge toward 2 V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500 V and the comparator output will switch to 0 V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0 V. At this time V_{FB} will start discharging toward 0 V with a time constant R_1C_1. When V_{FB} is less than 0.5 V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0 V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\,\frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF}\,(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}\,(\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}\,(\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{duty cycle}) \times (\text{clock})$$

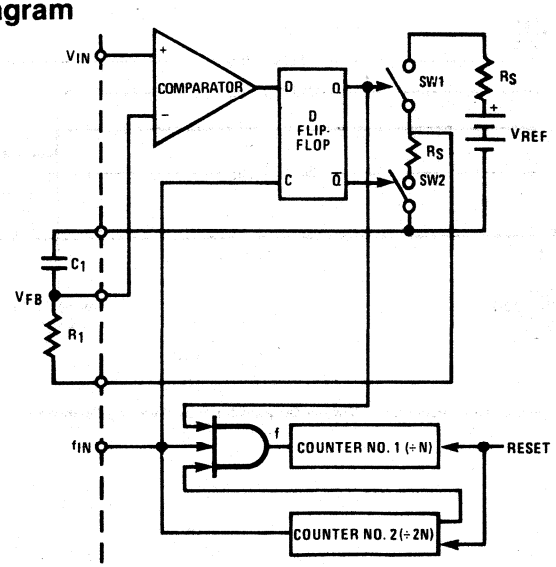
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(\text{clock})/N} = \frac{(\text{duty cycle}) \times (\text{clock})}{(\text{clock})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3701 N = 4000.

Schematic Diagram



$V_{IN} = V_{FB} = V_{REF} \times (\text{duty cycle})$

$f = (\text{duty cycle}) \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{(\text{duty cycle}) \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

Figure 1. Analog Loop Schematic Pulse Modulation A/D Converter

General Information

The timing diagram, shown in figure 2, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 129,024 x $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 128 x $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way.

Internally the ADD3701 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in figure 3, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 129,024 x $1/f_{IN}$ and the minimum time is 512 x $1/f_{IN}$.

Timing Waveforms

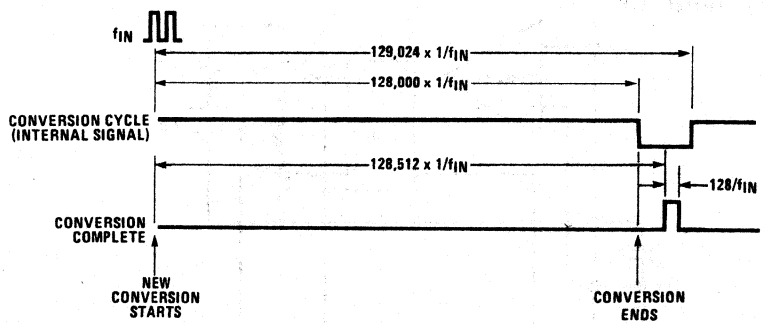


Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

Timing Waveforms (Continued)

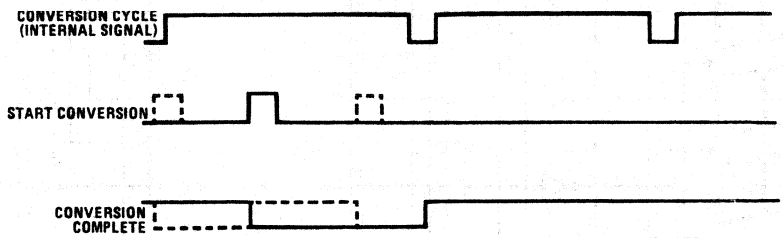


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3701 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3701 to minimize these problems but poor printed circuit layout can negate these features.

Figures 4, 5, and 6 show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators all function well and are shown in figures 4, 5, and 6. Adding more filtering than is shown will in general increase the jitter rather than decrease it.

The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0 to +3.999 counts operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or - (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in figure 5.

Figures 5 and 6 show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0 nA of leakage current will cause 0.1 mV error (1.0×10^{-9} A x 100 kΩ = 0.1 mV). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.

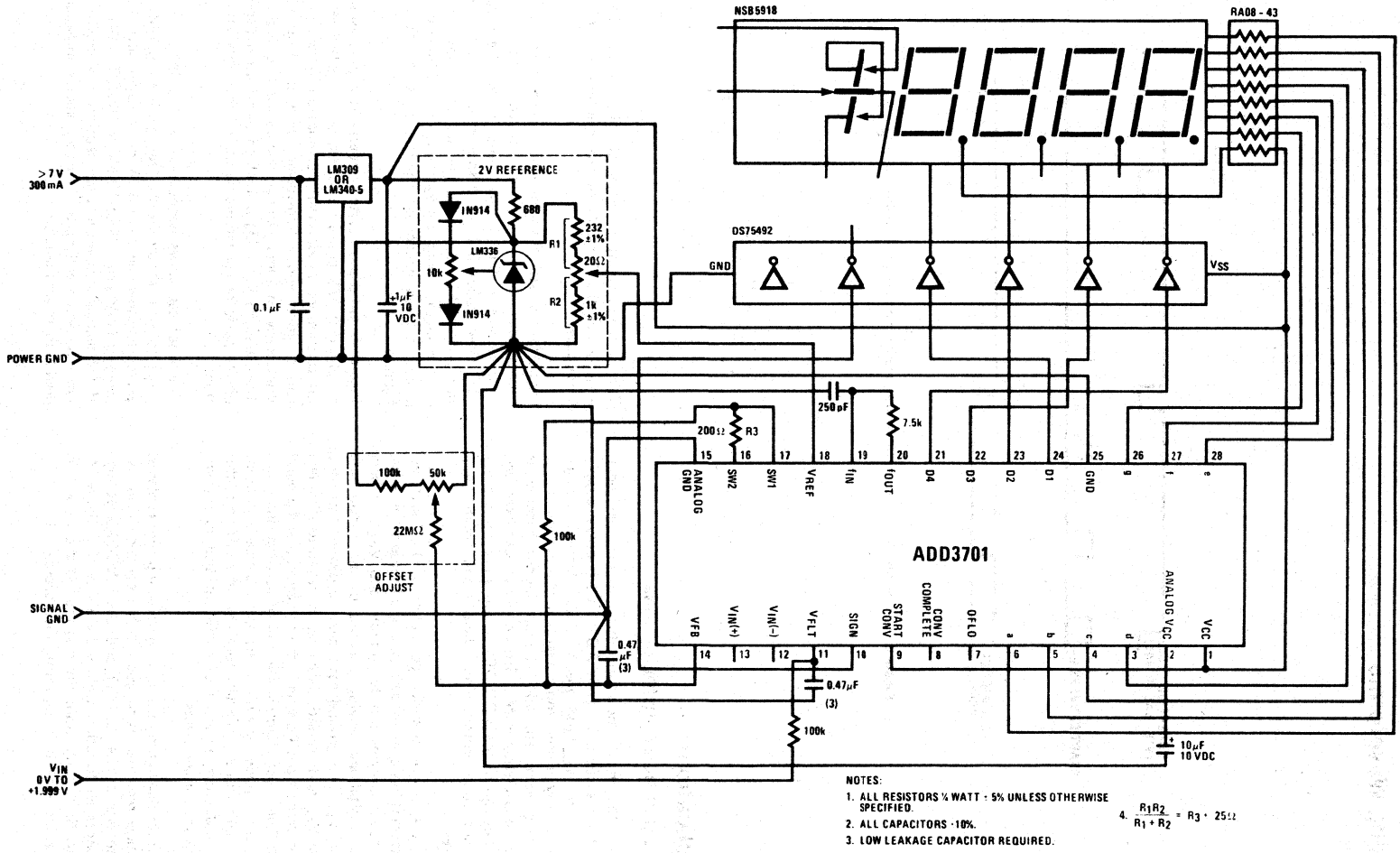
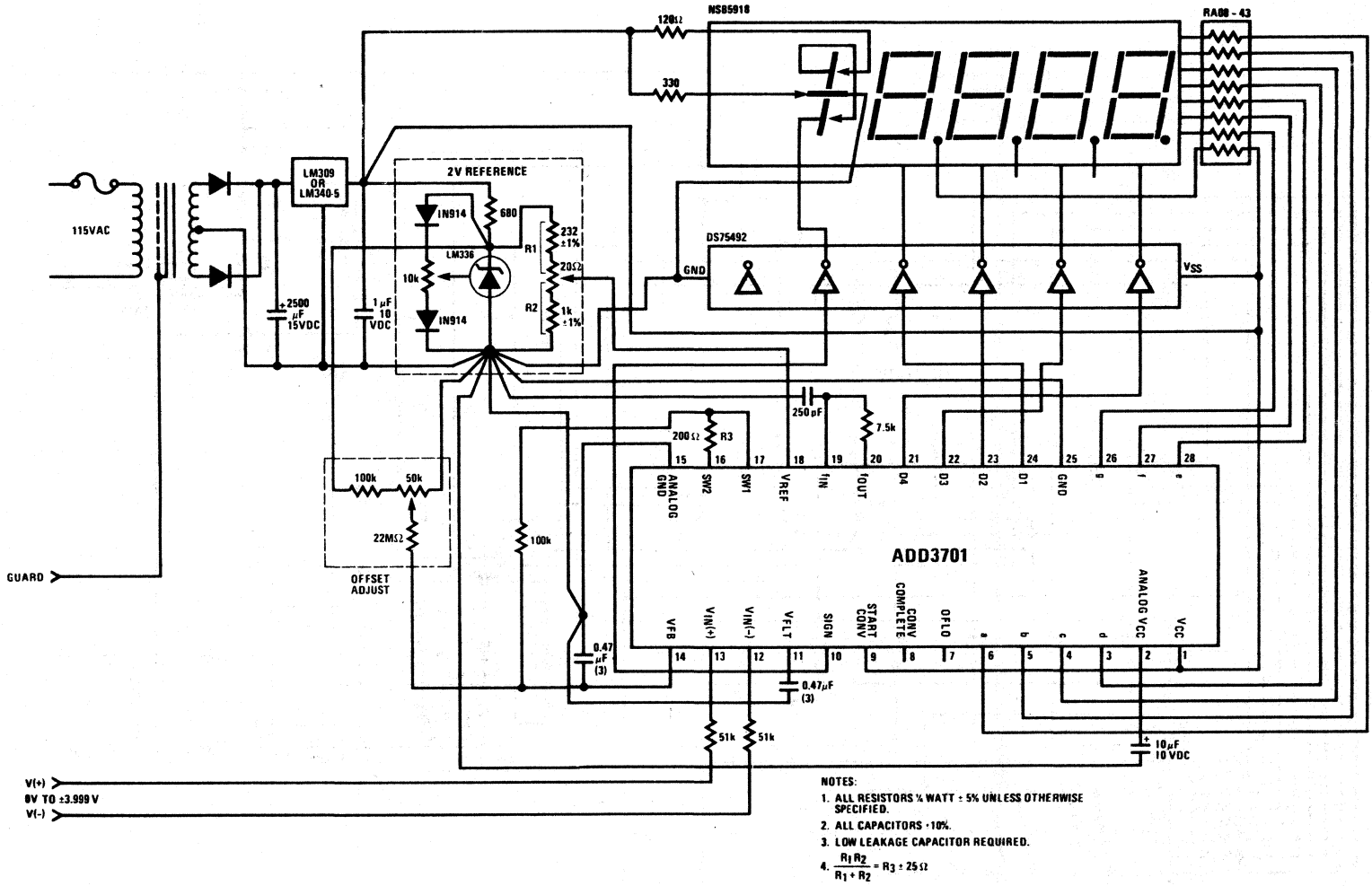


Figure 4. 3¾-Digit DPM, +3.999 Count Full Scale



NOTES:
1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$

Figure 5. 3¾-Digit DPM, ±3.999 Counts Full Scale

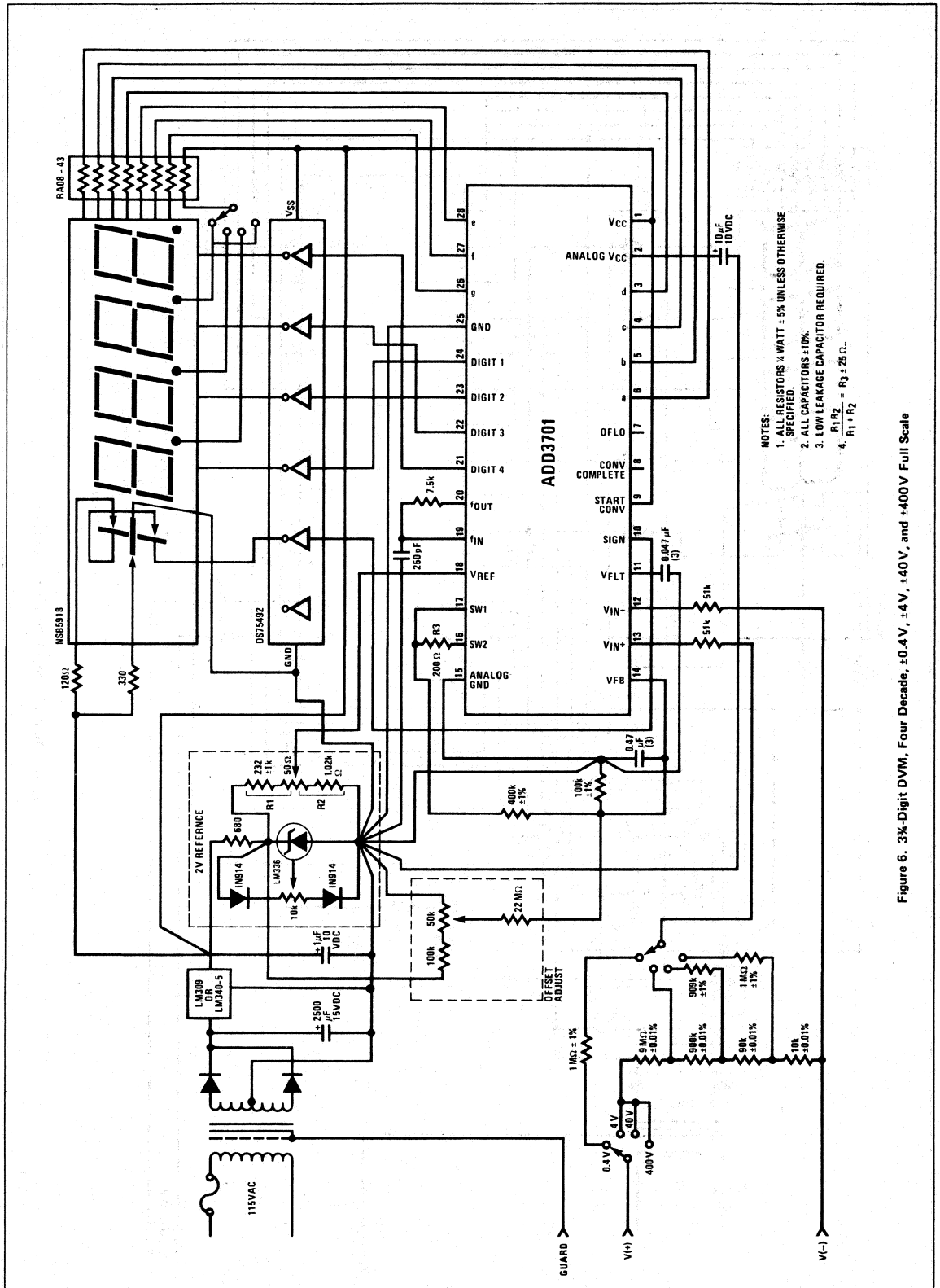


Figure 6. 3½-Digit DVM, Four Decade, ±0.4V, ±4V, ±40V, and ±400V Full Scale

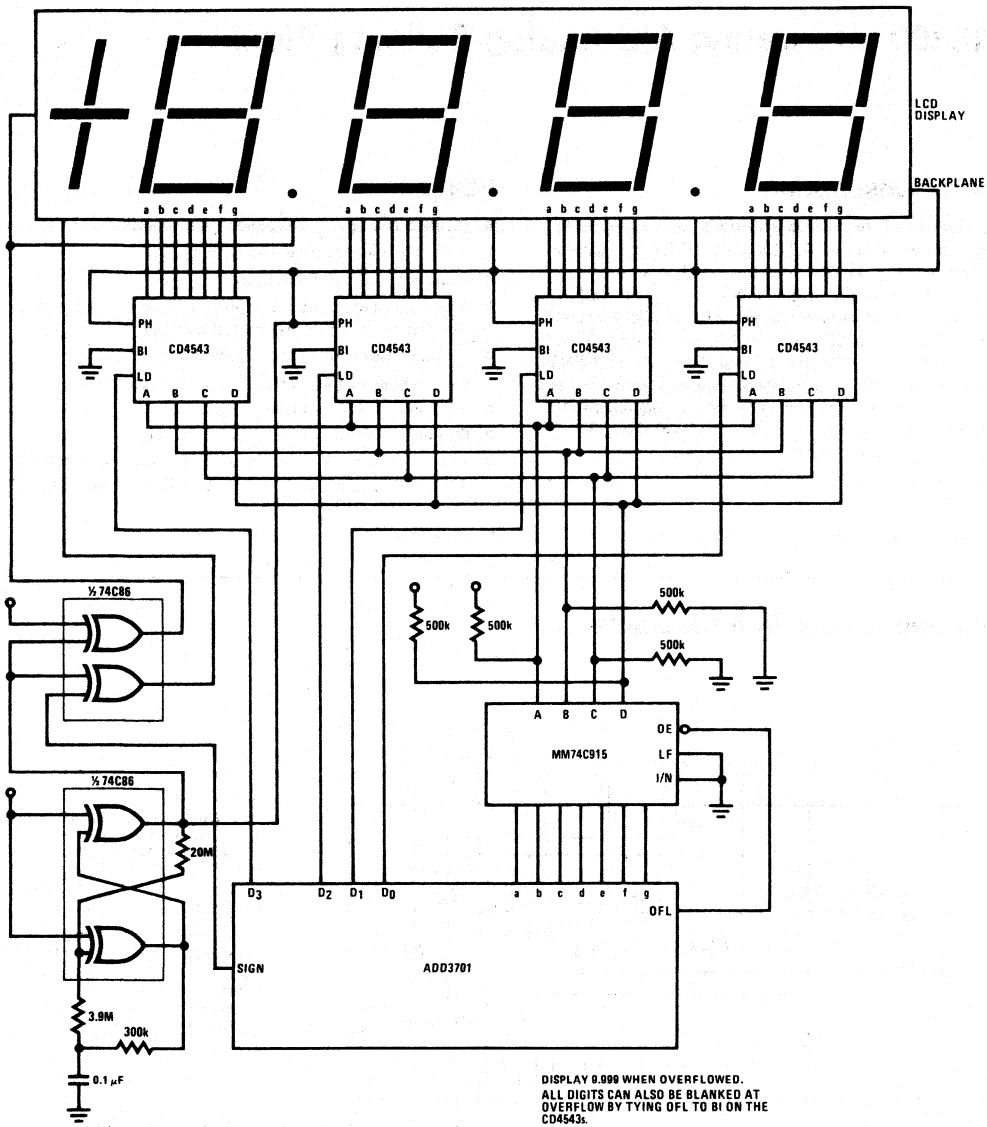
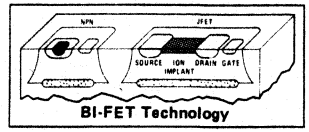


Figure 7. ADD3701 Driving Liquid Crystal Display

National Semiconductor

Analog-to-Digital Converters



LF13300 Integrating A/D Analog Building Block

General Description

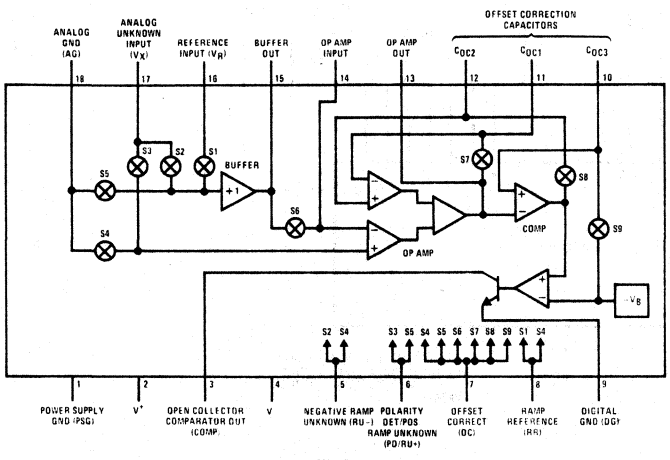
The LF13300 is the analog section of a precision integrating analog-to-digital (A/D) system. JFET and bipolar transistors (BI-FET) are combined on the same chip to provide a high input impedance unity gain buffer, comparator and integrator, along with 9 JFET analog switches. The LF13300 has sufficient resolution to construct up to a 4 1/2-digit Digital Panel Meter (DPM) or a 12-bit (plus sign) Data Acquisition System and is specifically designed for use with either the ADB4510 BCD digital building block or the ADB1200 (MM5863)* 12-bit binary building block.

*See ADB1200 (MM5863) data sheet for more information.

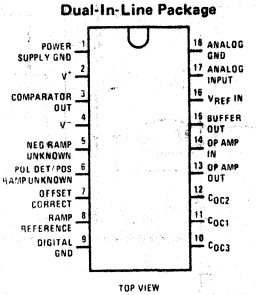
Features

- Rugged JFETs allow blow-out free handling
- High input impedance 10,000 MΩ typ
- Automatic offset correction
- Analog circuitry can be physically and electrically isolated from high noise digital circuits
- Analog input range of ±11V with ±15V supplies
- Wide power supply voltage range ±5V to ±18V
- TTL and CMOS compatible logic
- Can interface directly with microprocessors
- Versatile: can be used as a 12-bit plus sign binary A/D, 4 1/2-digit, 3 3/4-digit and 3 1/2-digit Digital Panel Meter (DPM)
- Low cost

Block and Connection Diagrams



Dual-In-Line Package



Order Number LF13300D
See NS Package D18A

Section 7

Data Acquisition Systems

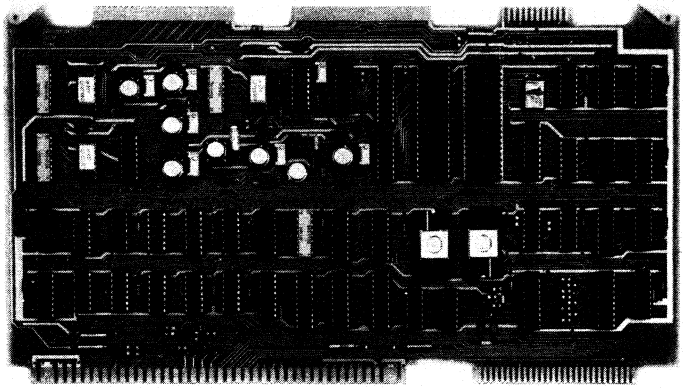
7

Section Contents

National Semiconductor

Data Acquisition Systems

BLC-8715
Intelligent Analog I/O Board



- **Intelligent Analog Input with Stand-Alone Measurement and Control Capability**
- **Low Cost Computing Power**
  - 8085 CPU
  - 1K static RAM
  - Up to 4K ROM/PROM
  - Memory-mapped 256 byte RAM communication/control "MAILBOX"
  - 4 interrupt levels
- **22 Channels Programmable Digital I/O**
- **RS232C Serial Interface**
- **Programmable 14-Bit Counter/Timer**
- **Analog Application Flexibility**
  - 16 single-ended/8 differential channels software configurable in any mix.
  - Bipolar capability from ±400 microvolts to ±5 volts.
  - All seven available gains from 1 to 100 software programmable.
  - 8-bit, 8-microsecond A to D conversion. Dynamic range expansion to >12 bits using auto-range techniques.
  - Scan modes software configurable.
  - 25kHz data throughput.
  - 4mHz bandwidth Bifet™ instrumentation amplifiers.
  - Analog measurement sequence after channel selection to end-of-conversion hardware controlled, freeing CPU for other tasks.
  - ±1 LSB overall analog accuracy, including quantizing and worst-cased for all error sources.
- **Firmware Monitor available with CPU programming, analog configuration, analog scanning, and calibration features**
- **Compatible with All Series/80 Boards and Card Cages**

Product Overview

The BLC-8715 is a self-contained low-cost stand-alone computer with flexible analog measurement and digital I/O capability. The BLC-8715 extends the Series/80 family of microcomputer products into a wider variety of instrumentation and industrial applications by providing dedicated distributed processing capability in a single board.

The analog capability of the BLC-8715 provides for multiple inputs. The analog input functions allow an input sampling rate of 25kHz, and subsequent processing and storage may be performed on-board. The BLC-8715 is equipped with sample and hold circuitry. Accuracy of conversion is assured by dedicated logic providing proper sampling and

holding intervals. Analog inputs may be sampled in any mix of random, sequential and repetitive modes, under on-board computer control. The board contains an 8-bit analog converter, 16 single-ended or 8 differential channels, programmable gain amplifier, and sample hold functions.

The BLC-8715 is also a complete computer including a CPU, serial communications interface, 22 parallel I/O, 1K-bytes private static random access memory, sockets to accept up to 4 K-bytes of read only memory, a 14 bit counter/timer, a system clock, and an additional 256 bytes of RAM accessible by the local CPU, or a MULTIBUS host CPU, mappable over the system 64 K-byte address space.

The BLC-8715 is configured as a MULTIBUS slave and may be interrrupt or status driven by a MULTIBUS host, communicating through its 256 byte dual access mailbox memory.

Functional Description

Central Processor

The CPU is an 8085A which has 100% software compatibility with the 8080A. The advanced features of the 8085A chip set are utilized to provide a system clock, vectored interrupts, serial I/O, memory and parallel I/O.

Memory

The BLC-8715 provides 1024 bytes of private RAM implemented with MM2114 modules. Private RAM is mapped from 2000_H to $23FF_H$.

Sockets and jumper options are provided to implement up to 2 K-bytes of EPROM with 2708s or 4 K-bytes with 2716s, or their ROM equivalents. ROM/PROM addressing is defined from 0000_H to limits set by the type and quantity of ROM/PROM used.

The BLC-8715 also provides 256 bytes of RAM accessible by either the BLC-8715 CPU or a MULTIBUS host for communication and control. This "mailbox" is addressed from BASE + 00_H to BASE + FF_H, where BASE is set by user selectable jumpers on 256 byte boundaries. Means are provided to permit the local CPU to determine the BASE address.

Parallel I/O

22 parallel I/O lines are provided by the I/O section of an 8155. Using standard 8080/8085 instructions, the 22 lines may be configured into a wide variety of unidirectional, bidirectional, and interrupt/ status driven modes.

Serial I/O

The unique serial SID and SOD pins of the 8085 are interfaced to the outside world via RS232 drivers. Using software techniques only, or in combination with the timer section of the 8155, baud rates up to 9600 may be implemented. Power from the BLC-8715 is made available to the 26 contact J1 card edge to support the BLC-530 TTY adapter.

Interval Timer

A 14-bit programmable timer is made available as part of an 8155. The timer out pulse is default jumpered to interrupt RST 7.5, which is edge latched by the CPU and may be acknowledged and reset by software.

Interrupt System

4 interrupt levels are supported by the BLC-8715.

Interrupt Level	Priority
TRAP	1 (highest)
RST 7.5	2
RST 6.5	3
RST 5.5	4

Trap is a non-maskable interrupt and is normally disabled by a jumper to GND but may be jumpered to pin 19 of P2 for power-fail shut down purposes or similar catastrophic events.

RST 7.5 is an edge sensitive, latched, maskable interrupt which is normally jumpered to the timer output.

RST 6.5 is a level sensitive, maskable interrupt which is normally jumpered to the ADC end-of-conversion (EOC) latch. The EOC latch is reset whenever the ADC output register is read by the CPU.

RST 5.5 is a level sensitive, maskable interrupt which is normally disabled, but may be connected to any of various sources.

The 8155 parallel port handshake lines are brought to the interrupt jumper matrix to utilize any of the available interrupt levels as desired.

MULTIBUS interrupts, INT0/ — INT7/, are brought to the interrupt matrix to utilize any of the available interrupt levels.

Analog Input

A flexible local CPU interface to the analog measurement control hardware is provided via 4

unique I/O instructions. These instructions provide the following functions:

I/O ADDRESS	I/O OPERATION	FUNCTION
07_H to $F7_H$	Read	• Starts measurement sequence • Selects input channel (High Nibble = Input Channel I.D.) • Causes a gain/ configuration register to output 3 bits to gain selector switch and 1 bit to configuration (single/differential) selector switch • Sampling interval & hold timing through end of conversion interrupt generation is initiated by this instruction.
06_H	Read	• Places ADC output into CPU accumulator • Resets measurement control logic • Resets EOC interrupt • Resets base address interrupt when used to retrieve base address on CPU initialization
06_H	Write	• Sets an interrupt which may be used to generate an interrupt to a MULTIBUS host. This is automatically cleared when host accesses BLC-8715
07_H to $F7_H$	Write	• Writes lower nibble of CPU accumulator to the 16 x 4 bit gain/ configuration register. High nibble of I/O address corresponds to each input channel I.D.

Analog input scan modes (sequential, random, repetitive) may be simply achieved in software by configuring the sequence of I/O reads. The BLC-8915 Firmware Monitor provides a convenient method of passing the desired scan parameters to the CPU via the 256 byte mailbox.

Firmware Monitor

The BLC-8915 Monitor provides the following functions:

- Serial I/O operator interface routine via CRT/Keyboard
- Initialization of all BLC-8715 hardware
- Direct user through calibration, test, and measurement scan
- Provide programming routines (modify and display memory, modify and display CPU registers, initiation of user program, insert, breakpoint, single step, and read and dump paper tape)

The monitor makes use of the memory mapped mailbox to provide a host/stand-alone software interface to transfer channel configuration, scan control, command, and data to or from the resident firmware. The address of the mailbox is from BASE + 00_F to BASE + FF_H, where BASE is user selectable jumper code relocating the mailbox anywhere in the 65K address range on the 256 byte boundaries.

BASE + 0 is dedicated as a command register. After a write operation to this location, by either a host or the local CPU, the analog measurement is started. The mailbox is defined in Table A for use by the BLC-8915 Monitor, and represents one of many possibilities for providing a flexible software information and control interface.

A. Dual Access Register

Host operation options are specified in the following table. For stand-alone operation, user BLC-8715 software could initialize the table as desired. The BLC-8915 Monitor provides default values of sequential scan, no skips, stop scan after one cycle, scan all channels with gain of 1, and single-ended channel configuration. Under monitor control, a user may initialize the table, then use the monitor "A" command to commence the scan.

Table A

Address	Name	Operation
Base + 0_H	Command	Write
Base + 1_H	Status	Read
Base + 2_H	Acknowledge	Read/Write
Base + 3_H	Scan Parameter	Write
Base + 4_H to Base + 15_H	User Defined	User Defined
Base + 16_H	Start Scan	Write
Base + 17_H	End Scan	Write
Base + 18_H to Base + 27_H	Configuration	Write
Base + 28_H to Base + 37_H	Data	Read
Base + 38_H to Base + FF_H	User Defined	User Defined

B. Command Register (Base + 0_H)

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	EOS INT.

If bit 0 is set, an interrupt to the Series/80 bus is generated after one scan cycle. After a write to this register, a scan sequence is started.

C. Status Register (Base + 1_H)

This register may be user defined to post status. It is not used by the BLC-8915 Monitor.

D. Acknowledge Register (Base + 2_H)

Useful as a host/slave software in continuous scan operation. The BLC-8715 writes FF_H after each scan. The BLC-8715 can then monitor this register until host has read the scan data and cleared this register before the BLC-8715 starts its next scan sequence.

E. Scan Parameter Register (Base + 3_H)

7	6	5	4	3	2	1	0
X	X	X	Single or Repetitive Scan	No. of Channels Skipped			

If skip scan is specified in the command register, the program looks up the number of channels to skip from this register, after previously looking up the starting channel address.

F. User Defined (Base + 4_H to Base + 15_H)

These may be used to expand scan control registers, HI/LO alarm limits for each channel, or additional status conditions.

G. Start Scan Register (Base + 16_H)

7	6	5	4	3	2	1	0
Relative Base Address of Start of Scan Channel (18_H to 27_H)							

H. End Scan Register (Base + 17_H)

7	6	5	4	3	2	1	0
Relative Base Address of End of Scan Channel (18_H to 27_H)							

I. Configuration Registers (Base + 18_H to Base + 27_H)

7	6	5	4	3	2	1	0
Channel No.				Single/ Differential	Gain		

0	0	1	X1
0	1	0	X2
0	1	1	X5
1	0	0	X10
1	0	1	X20
1	1	0	X50
1	1	1	X100

In a scan mode, channel selection is sequential from contents of Base + 18_H to Base + 27_H in ascending order. Random scan is achieved by writing the random sequence desired.

Differential channels consist of paired single-ended channel numbers N and N + 8, where N = 0 to 7. Only the address of the upper channel of a differential pair need be specified for differential selection.

J. Data Registers (Base + 28_H to Base + 37_H)

7	6	5	4	3	2	1	0
ADC OUTPUT							

The monitor simply writes the output corresponding to each channel specified by the Configuration Register to the corresponding Data Registers. The BLC-8715 provides a jumper to obtain either 2's complement or offset binary format.

Specifications

Microprocessor

CPU —	8085A
Instruction —	8, 16, or 24 Bits
Data —	8 Bits
Cycle Time —	2.00 microsecond for fastest instruction, i.e. 4 clock cycles
System Clock —	2.00mHz ± 0.1%

Memory

RAM —	1024 Bytes, private 256 Bytes, dual access
ROM —	Sockets for up to 4k Bytes
Parallel I/O —	22 programmable lines (three 8155 ports)
Serial I/O —	SID and SOD functions of 8085 CPU used for serial communications controlled by software through RIM and SIM instructions. RS-232 and TTL interfaces. TTY interface via BLC 530 adapter.
Interrupts —	Four-level interrupts routed to CPU. Each interrupt automatically refers to a unique address location.
Timer —	14-bit programmable timer 125.0kHz ± 0.1% clock input

Analog Input

Scan Mode —	On-board programmable (sequential, random, repeat, mixed)
Channels —	16 single-ended or 8 differential (software configurable in any mix)
Channel Resolution —	8-bit 2's complement or offset binary. Dynamic range of A/D converter expanded to greater than 12 bits with auto ranging capability via programmable gains.
Full Scale Range —	±(0.05, 0.10, 0.25, 0.5, 1.0, 2.5, 5.0) volts
Programmable Gain —	X1, X2, X5, X10, X20, X50, X100
Sample Time —	Default jumpered to 32 microseconds to insure 12-bit accuracy @ X 100 gain. Rejumperable to 2 microseconds, in steps.
Input Leakage —	< 10nA @ 25°C
Current —	< 60nA, 0-70°C
Input Resistance —	2 Kohms, power off > 100 Megohms, power-on
Input Capacitance —	< 100pF
Channel Crosstalk —	< 80dB @ 200Hz
Sample and Hold Feed Through —	< 80dB @ 200Hz
Common-Mode Rejection —	> 60dB @ 1 kohm source unbalance
Common-Mode Voltage —	±5 volts, max (signal + common mode)
Input Over Voltage Protection —	±30 volts, peak
Overall Accuracy —	6 months, 15°C to 35°C, ±(0.4% RDG + 1 LSB)
Accuracy Tempco —	0 to 15°C & 35°C to 50°C, ±(0.01% RDG + 0.01% Range)/°C
Monotonicity —	Guaranteed, 0-70°C
System Interface —	MULTIBUS™ compatible memory-mapped slave

Connectors

System Bus —	86 contact double-sided card edge connector on 0.156 inch centers
Auxiliary Bus —	60 contact double-sided card edge connector on 0.1 inch centers
Parallel I/O — and Analog Inputs	50 contact double-sided card edge connector on 0.1 inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O —	26 contact double-sided card edge connector on 0.1 inch centers Recommended mating connector: 3M 3462-0001 AMP 1-583715-1

Power	**VDC**	**Max Current**
	+5	2A
	−5	100mA with 2708 EPROM
	+12	250mA
	−12	250mA

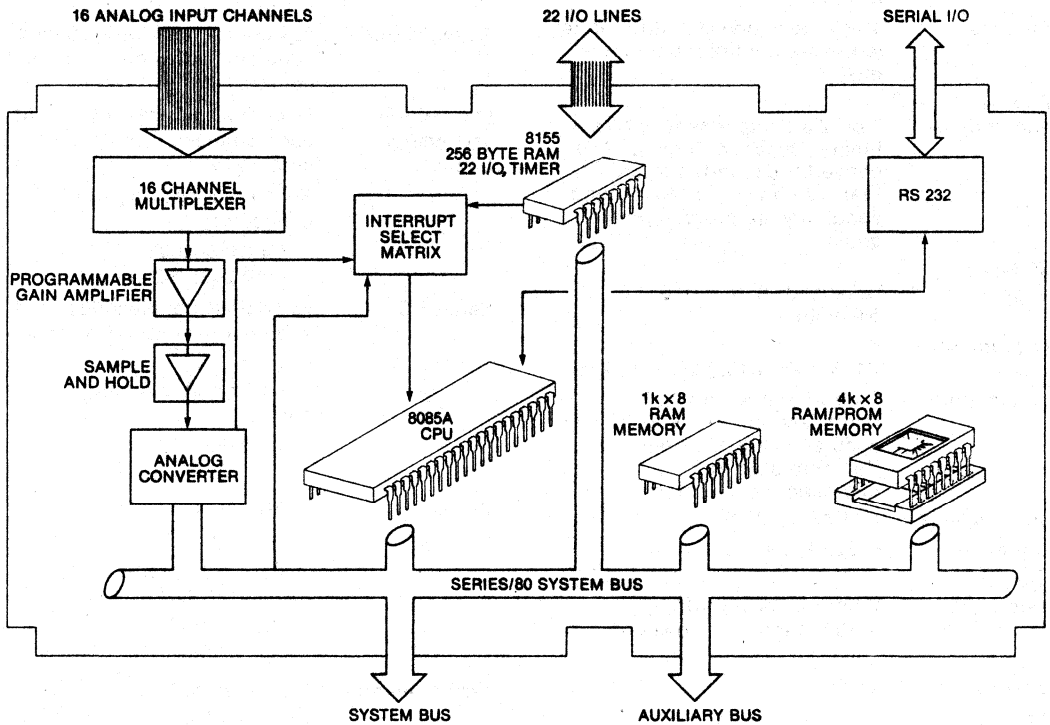
Environmental	Temperature 0-70° Humidity 0-90% RH, non-condensing
Physical	Height 6.75 in (17.15 cm) Width 12.00 in (30.48 cm) Depth 5 in (12.7 cm) Weight 14 oz (397 gm)

Ordering Information

BLC-8715	Series 80 Intelligent Analog Board includes CPU, 1KB static RAM, sockets for up to 4KB ROM, 22 parallel digital I/O, serial I/O interface, timer, and 16 single-ended or 8 differential channel analog processing capability.
BLC-8915	BLC-8715 Monitor provides CPU programming, analog configuration, analog scanning, analog measurement, and analog calibration functions.

Documentation

420305927-001	BLC-8715 Intelligent Analog Board Hardware Reference Manual

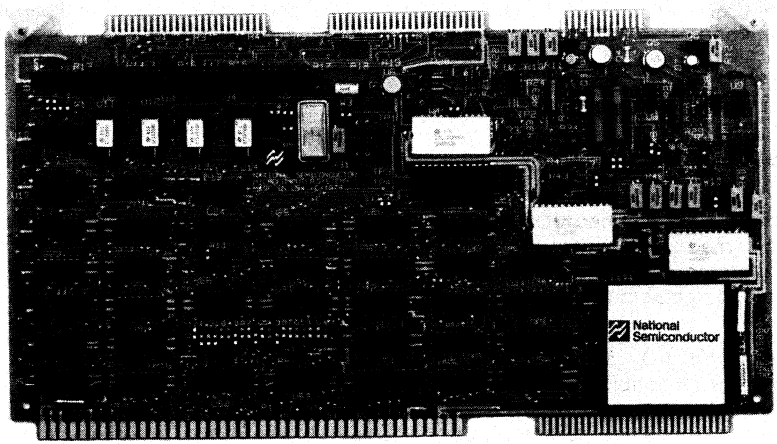


BLC-8715 Diagram

National Semiconductor

Data Acquisition Systems

BLC-8737
Analog Input/Output Board With Memory



- **Mailbox Bus Interface**
  - Latest data from all channels stored on-board
  - Gains need be set only once
  - Simple memory reference instructions to read data or set gains
- **Application Flexibility**
  - 16 single-ended/8 differential channels
  - Expandable to 32 single-ended/16 differential channels
  - 2 output channels
  - Provisions for 4-20ma inputs and outputs
  - Programmable gain amplifier
  - Sequential scan or CPU-driven selected channel conversions
  - Input protection up to 125VAC
- **12-Bit Resolution With ±0.05% Overall Input and Output Accuracy**
- **4-20ma True Current Sourcing Output Channels Permit Grounded Loads**
- **Single 5V Power Required**

Product Overview

The BLC-8737 analog I/O Board with memory extends the Series/80 family of microcomputer products into a wide variety of instrumentation and process-control applications, yet minimizes the data interfacing software because of the on-card memory. Multiple analog input and output capability is provided.

The BLC-8737 makes each input channel appear to be a RAM address. Data is read by a single memory-read instruction at normal memory speeds. Writing into that address once will set the gain on that channel until reset to a different gain by a subsequent write (gain) instruction.

Analog inputs are automatically sampled in sequential repetitive mode. However, a gain-set write instruction will re-start the scan at that channel. This mode, together with an interrupt output, allows random or equivalent single-channel operation when desired. The throughput rate is 8500 channels/second, and is adequate for most process/instrumentation systems with data bandwidth to 100/200/400 Hz on each of 32/16/8 channels.

The input circuitry contains 16 single-ended or 8 differential-channel multiplexers, input protection on each channel, a fast-settling differential (instrumentation) amplifier with software programmable gain, sample-and-hold amplifier, a 12-bit analog-to-digital converter, voltage reference, gain-program memory, and 32-channel data memory. The input may be expanded to 32 single-ended or 16 differential channels.

The output circuitry contains two 12-bit digital-to-analog converters with latched input registers, a precision voltage reference with offsetting circuitry, and two 4-20ma voltage-to-current converters with true current sourcing to permit grounded loads.

Input channels are memory mapped to any contiguous block of addresses which are jumper selected beginning with an even address. Output channels are memory mapped anywhere else within the same 2K block as the input channels. RAM and ROM inhibit signals are provided, should the I/O card address overlap installed memory.

Functional Description

Standard Series/80 instructions control analog input and output. Memory mapped I/O and single memory-reference read and write instructions greatly simplify the programming task and reduce computer timing load compared with other analog I/O systems.

With memory mapped I/O, a segment of 32 contiguous addresses (16 double-byte locations) is predefined for input channels, and set by movable jumpers on the board. These addresses may be on any given 32-byte boundary within the 64K bytes of available address space. These addresses overlay system memory address functions with memory inhibit logic to prevent address contention for memory-mapped I/O addresses. Output channels share the same six most significant address bits with input addresses, however, they may be jumper selected to any other block of 16 locations within the same 2K space occupied by the input channels.

Analog Input

The card normally operates in a sequential scan mode with a 118 microsecond period devoted to each channel. This allows settling time for the multiplexer, instrumentation amplifier, and S/H amplifier A to D conversion time and data load time for on-card RAM. The BLC-8737 is always in operation, loading RAM with latest data for each channel and updating RAM on each succeeding scan. The data is read with a memory-read instruction (LHLD). Input data appears as 12 bits, right justified in a 16-bit data format. Bipolar data includes extended sign.

If channel data must be known to be more current than 2 milliseconds, the random access feature may be employed. To use this feature it is only necessary to re-write the gain instruction for the desired channel. A gain-set instruction will reset the channel address counter to the addressed channel, and will initiate a data acquisition/conversion cycle. At completion of conversion, an interrupt will signal when current data may be read as outlined above. The interrupt may be set to any, or none, of the eight bus interrupt lines.

The selected analog input is applied to the A/D converter through a software controlled programmable-gain amplifier which provides gains of 1,2,5, or 10, and a sample-and-hold amplifier. A set of movable jumpers allows additional gain multiples of 1, 4 or 10 applied to the above gains. With the ADC jumper selected for +10.24 or ±10.24 full-scale input voltage, the variable gain amplifier permits sampling of analog input voltages as shown in Table I.

Table I. Programmable-Gain Full-Scale Values

Gain Selected		Unipolar	Bipolar Selection
Software	Jumper		
1	1	+10.24	±10.24
2		+ 5.12	+ 5.12
5		+ 2.048	+ 2.048
10		+ 1.024	+ 1.024
1	4	+ 2.56	± 2.56
2		+ 1.28	± 1.28
5		+ 0.512	± 0.512
10		+ 0.256	± 0.256
1	10	+ 1.024	± 1.024
2		+ 0.512	± 0.512
5		+ 0.2048	± 0.2048
10		+ 0.1024	± 0.1024

The only analog input control parameter is the gain setting for each channel. After system initialization, gain must be set for every channel. Part of a post-initialization or system start-up program will be a series of gain-set memory-write instructions, one to each channel address. A two-bit gain word may be written into either byte of the addresses assigned to the input channels. The gain select words are described in Table II.

Table II Gain-Set Data Word

Gain	Data Word
1	(MSB) X X X X X X 1 1
2	X X X X X X 1 0
5	X X X X X X 0 1
10	X X X X X X 0 0

Analog Output

Two independent analog outputs may be unipolar or bipolar, and provide outputs via 12-bit DACs, according to jumper selections as follows:

0 to +5V
0 to +10V
±2.5V
±5V
±10V
4 to 20mA (source)

The current mode is operational for loop supplies of +12 to +40V. Both output channels are set to minimum scale at system initialization.

Output data is 12-bits, right justified in a 16-bit data field. The address space occupied by the output channels is in the same 2K byte area selected for input channels. Address lines ADR4/ to ADR9/ may be jumper selected anywhere in the 2K byte sector except at those addresses occupied by the input channels. The remaining address bits select the output channel and byte as shown in Table III.

Table III. Output Channel Addressing

Base + Address Bit 3/	2/	1/	0/	Channel
X	X	0	0	Ch1, Low Byte
X	X	0	1	Ch1, High Byte
X	X	1	0	Ch2, Low Byte
X	X	1	1	Ch2, High Byte

DC to DC Converter

The board contains a DC/DC converter to convert the +5V logic supply to the ±15V required by analog circuitry.

Diagnostic Test

A diagnostic test program is included with BLC-8737 to allow testing and calibration of the analog circuits. Calibration is recommended when a full-scale range jumper is reset (input or output).

Channel Expansion

Sockets are provided to double the number of channels by inserting two multiplexers (LF13508).

Specifications

Analog Input

Data Channels — 16 single-ended or 8 differential
Expandable to — 32 single-ended or 16 differential
Scan Mode — Sequential
Throughput Rate — 8500 conversions/second
Maximum Data Bandwidth — 200 Hz/ch (16 installed channels)
Full-scale Range —

0-10.24V		±10.24		0-20ma
0-5.12V	0-0.512V	±5.12	±0.512V	with user
0-2.56V	0-0.256V	±2.56V	±0.256V	installed
0-2.048V	0-0.2048V	±2.048V	±0.2048	250 ohm
0-1.024V	0-0.1024V	±1.024V	±0.1024V	resistors

Common Mode Voltage — +10.24V (signal plus common mode)
Overvoltage Protection — 125VAC
Programmable Gain
Software 1, 2, 5, 10
Jumper 1, 4, 10
Input Leakage Current — ⩽ 10nA @ 25°C (16 installed channels)
⩽ 60nA @ 0-55°C (16 installed channels)
Input Resistance — 3K ohms (power OFF)
⩾ 100M ohms (power ON)
Input Capacitance — ⩽ 100pF for ON channel (16 installed channels)
⩽ 10pF for OFF channel
Sample & Hold Feedthrough — ⩽ −80dB @ 200Hz
Crosstalk OFF to ON channel — ⩽ −80dB @ 200 Hz
Common-Mode Rejection ⩾ 60dB @ 200Hz (any gain)
ADC Resolution — 12 bits
Quantizing Error — ±½ LSB
Linearity Error — ⩽ ±½ LSB @ 55°V
⩽ ±1 LSB 0-55°C
Overall Accuracy — ⩽ ±0.05% FSR ± ½ LSB @25°C (Gain = 1)
⩽ ±0.07% FSR ± ½ LSB @25°C (Gain = 2, 5, 10)
Includes 3 sigma noise, linearity, offset and scale errors
No Missing Codes — 0-55°C

Analog Output

Data Channels — 2
Full-Scale Range — 0-5V and 0-10V @ 5mA
±2.5V, ±5V, and ±10V @ ±5mA
4-20mA sourced (load may be grounded)
Current-Mode Supply Voltage — 12-40V (positive)
Max. Current-Mode Load Resistance (+24V supply) — 800 ohms
DAC Resolution — 12 bits
Linearity Error — (Voltage Mode) ⩽ ±½ LSB @ 25°C
⩽ ±1LSB 0-55°C

Overall Accuracy (Voltage or current mode)	⩽ ±0.05% FSR @25°C (includes linearity, noise, zero and scale errors)
Settling Time —	
Voltage Mode	⩽ 4μs to ±0.05% of FSR
Current Mode	⩽ 1ms to 0.05%
Monotonic	0–55°C

Interface

System Bus Interface —	Data, address and control bus signals are TRI-STATE® or open-collector TTL compatible. Fully BLC/SBC compatible.

Interface

System Bus Interface —	Data, address and control bus signals are TRI-STATE® or open-collector TTL compatible. Fully BLC/SBC compatible.

Connectors	
System Bus —	86-contact double-sided card-cage edge connector on 0.156" centers.
Analog —	One 50-contact double-sided card-edge connector on 0.1 inch centers for input channels 1–16.
	One 50-contact double-sided card-edge connector on 0.1 inch centers for input channels 17–32.
	One 26-contact double-sided card-edge connector on 0.1 inch centers for output channels.
Recommended Mating Connector (Analog)	50 contact double sided connector on 0.1 inch centers 3M 3415-001 AMP 2-86792-3 26 contact double-sided connector on 0.1 inch centers 3M 3462-0001 AMP 1-583715-1

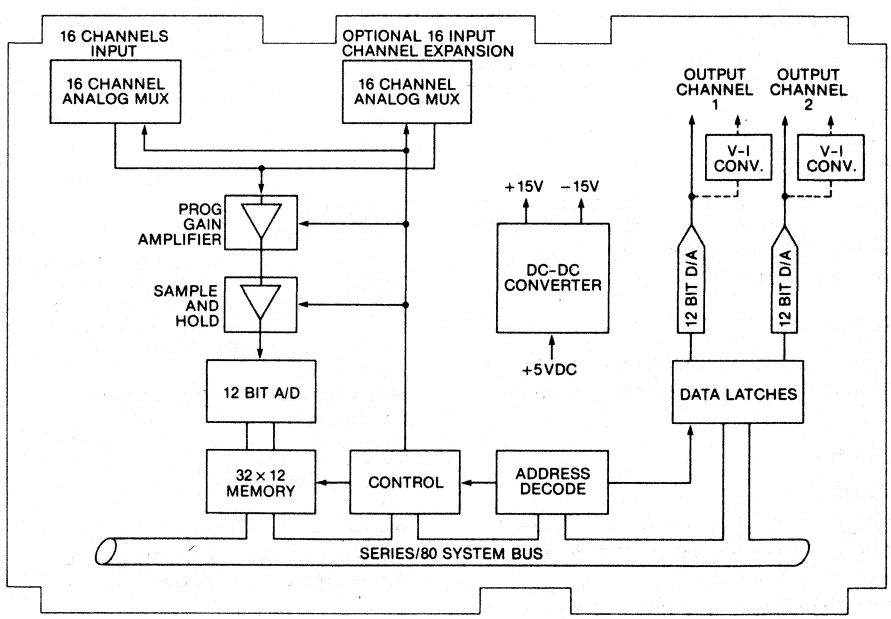
Power —	+5V ±5% @ 3A
Environmental —	
Temperature	0–55°C
Humidity	0–90% non-condensing
Physical —	
Height	6.75" (11.15 cm)
Width	12.00" (30.48 cm)
Depth	0.50" (1.27 cm)
Weight	18 oz. (510.3 g)

Order Information

BLC-8737-1 Analog I/O Board with Memory	Includes 16 single-ended or 8 differential analog input channels, manual, and diagnostic test program in paper tape media.
BLC-8737-2 Analog I/O Board with Memory	Includes 16 single-ended or 8 differential analog input channels, 2 analog voltage output channels, manual, and diagnostic test program in paper tape media.
BLC-8737-3 Analog I/O Board with Memory	Includes 16 single-ended or 8 differential analog input channels, 2 analog voltage or current output channels, manual, and diagnostic test program in paper tape media.

Documentation

420305890-001	BLC-8737 Analog I/O Board with Memory Hardware Reference Manual



BLC-8737 DIAGRAM

Section 8

Digital-to-Analog Converters

8

Section Contents

National Semiconductor

AD7520/AD7530 10-Bit, AD7521/AD7531 12-Bit Binary Multiplying D/A Converters

General Description

The AD7520 and the AD7521 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (typically 0.0002%/°C linearity error temperature coefficient). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference.

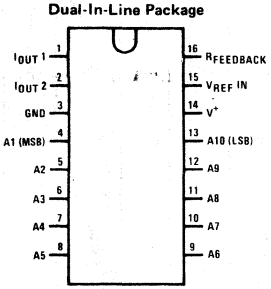
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity. The AD7520L, AD7520K, and AD7520J are direct replacements for the 10-bit resolution AD7520 and AD7530 family, and equivalent to AD7533 family. The AD7521K, AD7521J and AD7521L are direct replacements for the 12-bit resolution AD7521 and AD7531 family. For more information, see DAC1020 data sheet.

Features

- Linearity specified with zero and full-scale adjust only
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @ 15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq +25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—600 ns typ
- Low feedthrough error—1/2 LSB @ 100 kHz typ

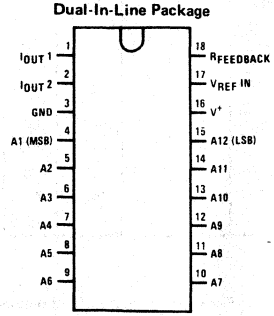
Connection Diagrams

AD7520/AD7530
Dual-In-Line Package



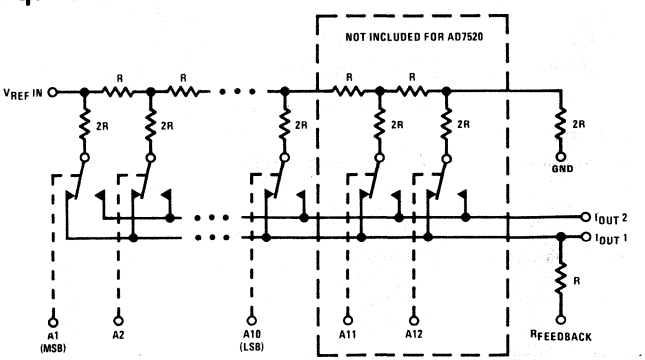
TOP VIEW

AD7521/AD7531
Dual-In-Line Package



TOP VIEW

Equivalent Circuit



Switches shown in digital high state

Ordering Information*

10-BIT D/A CONVERTERS

TEMPERATURE RANGE		0°C to 70°C		−40°C to +85°C		−55°C to +125°C
ACCURACY	0.05%	AD7520LN	AD7530LN	AD7520LD	AD7530LD	AD7520UD
	0.10%	AD7520KN	AD7530KN	AD7520KD	AD7530KD	AD7520TD
	0.20%	AD7520JN	AD7530JN	AD7520JD	AD7530JD	AD7520SD
PACKAGE OUTLINE		N16A		D16C		D16C

12-BIT D/A CONVERTERS

TEMPERATURE RANGE		0°C to 70°C		−40°C to +85°C		−55°C to +125°C
ACCURACY	0.05%	AD7521LN	AD7531LN	AD7521LD	AD7531LD	AD7521UD
	0.10%	AD7521KN	AD7531KN	AD7521KD	AD7531KD	AD7521TD
	0.20%	AD7521JN	AD7531JN	AD7521JD	AD7531JD	AD7521SD
PACKAGE OUTLINE		N18A		D18A		D18A

*Note: Devices ordered using these P/N's will be marked with AD7520 series and DAC102X series numbers.

Absolute Maximum Ratings

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Temperature Range

	MIN	MAX	UNITS
AD7520LN, AD7520KN, AD7520JN	0	+70	°C
AD7521LN, AD7521KN, AD7521JN	0	+70	°C
AD7530LN, AD7530KN, AD7530JN	0	+70	°C
AD7531LN, AD7531KN, AD7531JN	0	+70	°C
AD7520LD, AD7520KD, AD7520JD	−40	+85	°C
AD7521LD, AD7521KD, AD7521JD	−40	+85	°C
AD7530LD, AD7530KD, AD7530JD	−40	+85	°C
AD7531LD, AD7531KD, AD7531JD	−40	+85	°C
AD7520UD, AD7520TD, AD7520SD	−55	+125	°C
AD7521UD, AD7521TD, AD7521SD	−55	+125	°C

Electrical Characteristics (V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	AD7520L, AD7520K, AD7520J			AD7521L, AD7521K, AD7521J			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		10			12			Bits
Linearity Error	$T_{MIN} \le T_A \le T_{MAX}$, $-10V \le V_{REF} \le +10V$, (Note 1) End Point Adjustment Only (See Linearity Error in Definition of Terms)							
10-bit Parts	AD7520L, AD7520U, AD7521L, AD7521U, AD7530L, AD7531L			0.05			0.05	% FSR
9-bit Parts	AD7520T, AD7520K, AD7521T, AD7521K, AD7530K, AD7531K			0.10			0.10	% FSR
8-bit Parts	AD7520S, AD7520J, AD7521S, AD7521J, AD7530J, AD7531J			0.20			0.20	% FSR
Linearity Error Tempco	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)		0.0002			0.0002		% FS/°C
Full-Scale Error	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)		0.3			0.3		% FS
Full-Scale Error Tempco	$T_{MIN} < T_A < T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current								
I_{OUT1}	All Digital Inputs Low, $T_{MIN} \le T_A \le T_{MAX}$			200			200	nA
I_{OUT2}	All Digital Inputs High, $T_{MIN} \le T_A \le T_{MAX}$			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \le V^+ \le 16V$ (*Figure 2* of DAC1020 data sheet)		0.005			0.005		% FS/V
V_{REF} Input Resistance		10	15	20	10	15	20	kΩ
Full-Scale Current Settling Time	R_L = 100Ω from 0 to 99.95% FS							
	All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low, V_{REF} = 20 Vp-p @ 100 kHz			10			10	mVp-p
	D Package (Note 4)		6	9		6	9	mVp-p
	N Package		2	5		2	5	mVp-p
Output Capacitance								
I_{OUT1}	All Digital Inputs Low		40			40		pF
	All Digital Inputs High		200			200		pF
I_{OUT2}	All Digital Inputs Low		200			200		pF
	All Digital Inputs High		40			40		pF
Digital Input	(Note 1)							
Low Threshold	$T_{MIN} < T_A < T_{MAX}$,			0.8			0.8	V
High Threshold	$T_{MIN} < T_A < T_{MAX}$	2.4			2.4			V
Digital Input Current	$T_{MIN} \le T_A \le T_{MAX}$							
	Digital Input High		1	100		1	100	μA
	Digital Input Low		−50	−200		−50	−200	μA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range		5		15	5		15	V

Note 1: V_{REF} = ±10V and V_{REF} = ±1V.

Note 2: Using internal feedback resistor.

Note 3: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. For every millivolt offset between I_{OUT1} or I_{OUT2}, 0.005% linearity error will be introduced.

Note 4: To achieve this low feedthrough in D package, the user must ground the metal lid.

National Semiconductor

DAC0800 8-Bit Digital-to-Analog Converter

General Description

The DAC08 is a monolithic 8-bit high-speed current-output digital-to-analog converter (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC08 also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC08 will accept TTL levels with the logic threshold pin, V_{LC}, pin 1 grounded. Simple adjustments of the V_{LC} potential allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800L, DAC0802L, DAC0800LC, DAC0801LC and DAC0802LC are a direct replacement for the DAC08, DAC08A, DAC08C, DAC08E and DAC08H, respectively.

Features

- Fast settling output current — 100 ns
- Full scale error — ±1 LSB
- Nonlinearity over temperature — ±0.1%
- Full scale current drift — ±10 ppm/°C
- High output compliance — −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33 mW at ±5V
- Low cost

Typical Applications

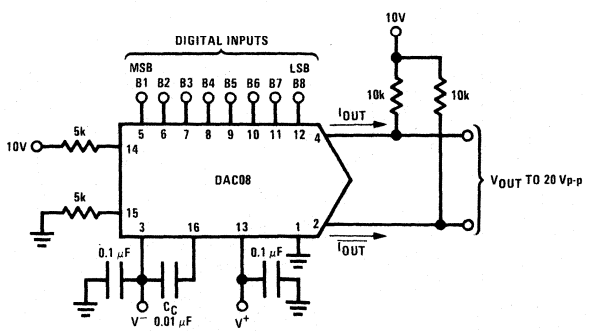
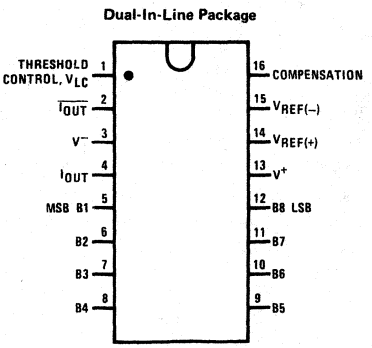


FIGURE 1. ±20 Vp-p Output Digital-to-Analog Converter

Connection Diagram



TOP VIEW

Ordering Information

NON LINEARITY	TEMPERATURE RANGE	ORDER NUMBERS*					
		D PACKAGE (D16C)		J PACKAGE (J16A)		N PACKAGE (N16A)	
±0.1% FS	−55°C ≤ T_A ≤ +125°C	DAC0802LD	LMDAC08AD				
±0.1% FS	0°C ≤ T_A ≤ + 70°C			DAC0802LCJ	LMDAC08HJ	DAC0802LCN	LMDAC08HN
±0.19% FS	−55°C ≤ T_A ≤ + 125°C	DAC0800LD	LMDAC08D				
±0.19% FS	0°C ≤ T_A ≤ +70°C			DAC0800LCJ	LMDAC08EJ	DAC0800LCN	LMDAC08EN
±0.39% FS	0°C ≤ T_A ≤ +70°C			DAC0801LCJ	LMDAC08CJ	DAC0801LCN	LMDAC08CN

*Note. Devices may be ordered by using either order number.

Absolute Maximum Ratings

Supply Voltage	±18V or 36V
Power Dissipation (Note 1)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs	*Figure 24*
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

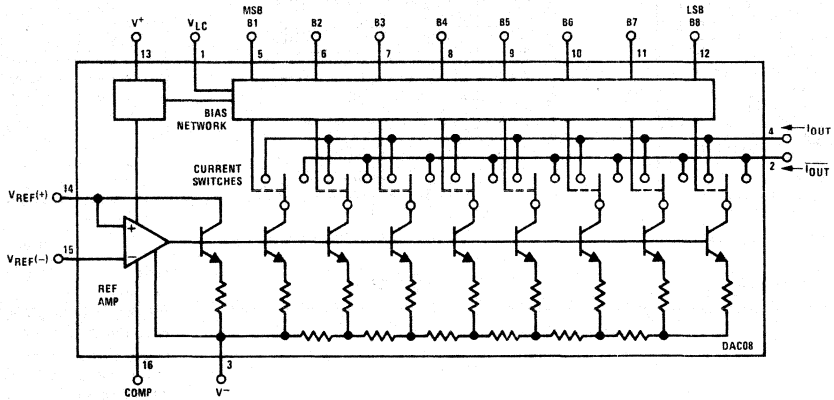
	MIN	MAX	UNITS
Temperature (T_A)			
DAC0802LA, LMDAC08A	−55	+125	°C
DAC0800L, LMDAC08	−55	+125	°C
DAC0800LC, LMDAC08E,	0	+70	°C
DAC0801LC, LMDAC08C,	0	+70	°C
DAC0802LC, LMDAC08H	0	+70	°C

Electrical Characteristics (V_S = ±15V, I_{REF} = 2 mA, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

	PARAMETER	CONDITIONS	DAC0802L/ DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19			±0.39	%FS
t_s	Settling Time	To ±1/2 LSB, All Bits Switched "ON" or "OFF", T_A = 25°C		100	135					100	150	ns
		DAC0800L					100	135				ns
		DAC0800LC					100	150				ns
t_{PLH}, t_{PHL}	Propagation Delay	T_A = 25°C										
	Each Bit			35	60		35	60		35	60	ns
	All Bits Switched			35	60		35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change < 1/2 LSB, R_{OUT} > 20 MΩ Typ	−10		18	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF} = 10.000V, R14 = 5.000 kΩ R15 = 5.000 kΩ, T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1	±8.0		±2	±16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	V^- = −5V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V^- = −8V to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels											
V_{IL}	Logic "0"	V_{LC} = 0V			0.8			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			2.0			V
	Logic Input Current	V_{LC} = 0V										
I_{IL}	Logic "0"	−10V ≤ V_{IN} ≤ +0.8V		−2.0	−10		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	2V ≤ V_{IN} ≤ +18V		0.002	10		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	V^- = −15V	−10		18	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S = ±15V	−10		13.5	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	*(Figure 24)*		8.0			8.0			8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	4.5V ≤ V^+ ≤ 18V		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$		−4.5V ≤ V^- < 18V		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
		I_{REF} = 1 mA										
	Power Supply Current	V_S = ±5V, I_{REF} = 1 mA										
I_+				2.3	3.8		2.3	3.8		2.3	3.8	mA
I_-				−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	mA
		V_S = 5V, −15V, I_{REF} = 2 mA										
I_+				2.4	3.8		2.4	3.8		2.4	3.8	mA
I_-				−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	mA
		V_S = ±15V, I_{REF} = 2 mA										
I_+				2.5	3.8		2.5	3.8		2.5	3.8	mA
I_-				−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Dissipation	±5V, I_{REF} = 1 mA		33	48		33	48		33	48	mW
		5V, −15V, I_{REF} = 2 mA		108	136		108	136		108	136	mW
		±15V, I_{REF} = 2 mA		135	174		135	174		135	174	mW

Note 1: The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 100°C. For operating at elevated temperatures, devices in the dual-in-line J or D package must be derated based on a thermal resistance of 100°C/W, junction to ambient, 175°C/W for the molded dual-in-line N package.

Block Diagram



Equivalent Circuit

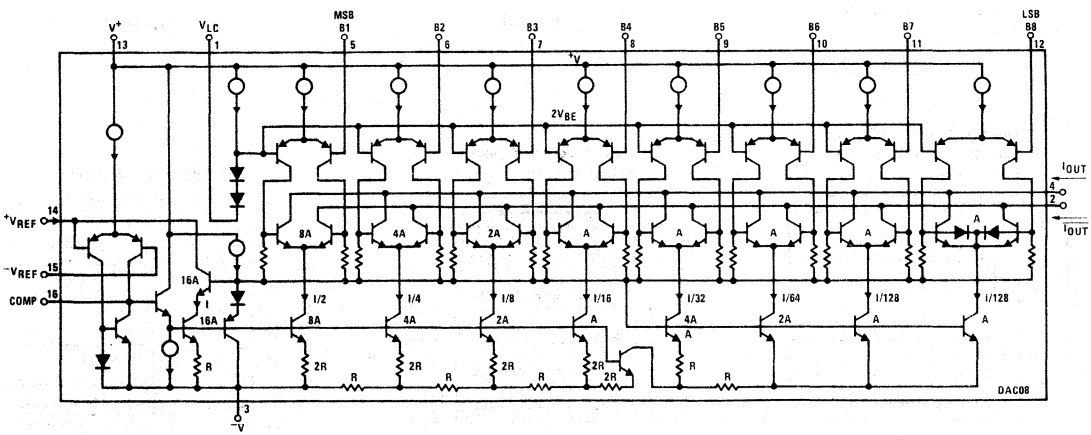


FIGURE 2

Typical Performance Characteristics

Full Scale Current vs Reference Current

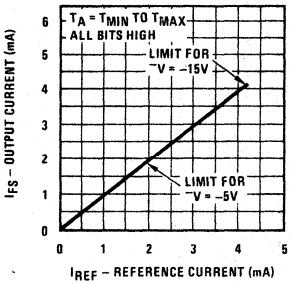


FIGURE 3

LSB Propagation Delay vs I_{FS}

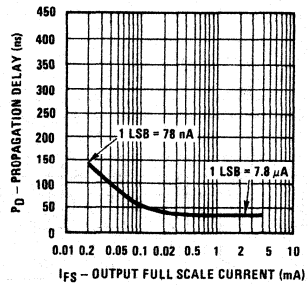
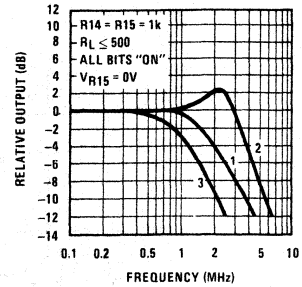


FIGURE 4

Reference Input Frequency Response



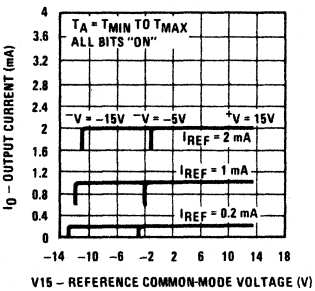
Curve 1: C_C = 15 pF, V_{IN} = 2 Vp-p centered at 1V.

Curve 2: C_C = 15 pF, V_{IN} = 50 mVp-p centered at 200 mV.

Curve 3: C_C = 0 pF, V_{IN} = 100 mVp-p at 0V and applied through 50 Ω connected to pin 14. 2V applied to R14.

FIGURE 5

Reference Amp Common-Mode Range



Note. Positive common-mode range is always (V+) − 1.5V.

FIGURE 6

Logic Input Current vs Input Voltage

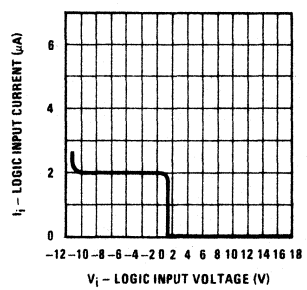


FIGURE 7

$V_{TH} - V_{LC}$ vs Temperature

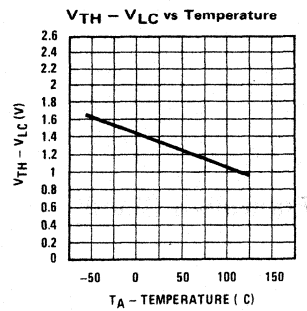


FIGURE 8

Output Current vs Output Voltage (Output Voltage Compliance)

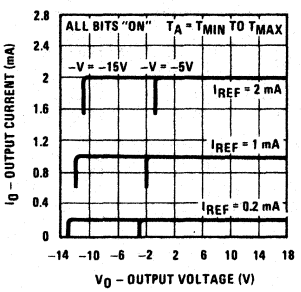


FIGURE 9

Output Voltage Compliance vs Temperature

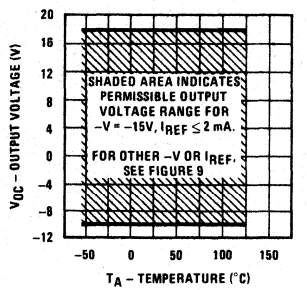
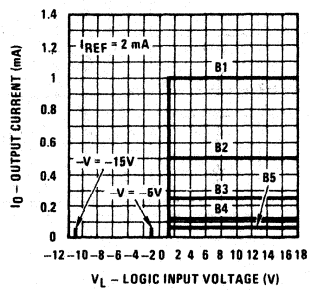


FIGURE 10

Bit Transfer Characteristics



Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

FIGURE 11

Typical Performance Characteristics (Continued)

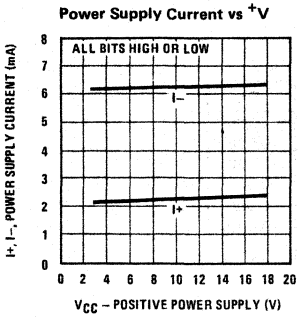


FIGURE 12

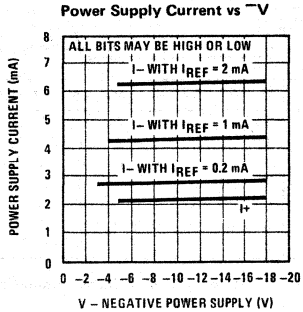


FIGURE 13

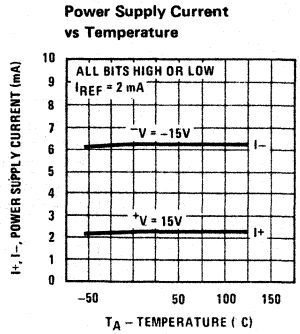
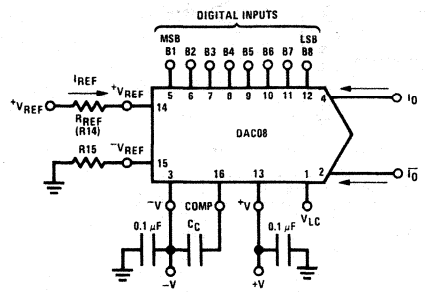


FIGURE 14

Typical Applications (Continued)



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:

$V_{REF} = 10.000V$
$R_{REF} = 5.000k$
$R15 \approx R_{REF}$
$C_C = 0.01\ \mu F$
$V_{LC} = 0V$ (Ground)

FIGURE 15. Basic Positive Reference Operation

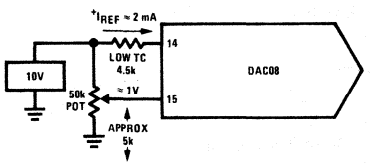
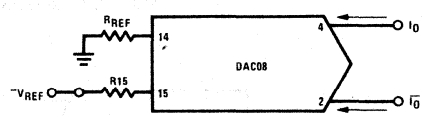


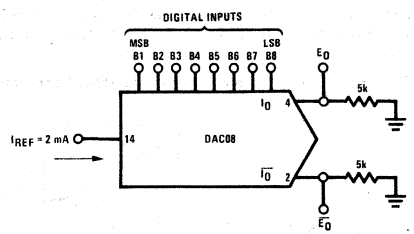
FIGURE 16. Recommended Full Scale Adjustment Circuit



$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note. R_{REF} sets I_{FS}; R15 is for bias current cancellation

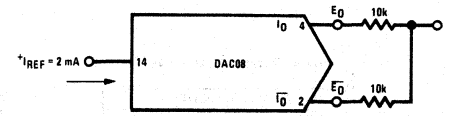
FIGURE 17. Basic Negative Reference Operation



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale−LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

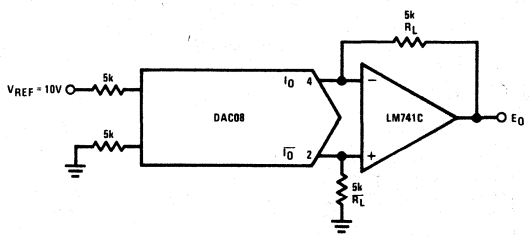
FIGURE 18. Basic Unipolar Negative Operation

Typical Applications (Continued)



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

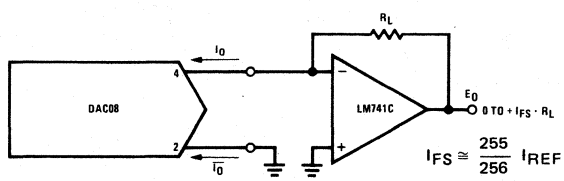
FIGURE 19. Basic Bipolar Output Operation



If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

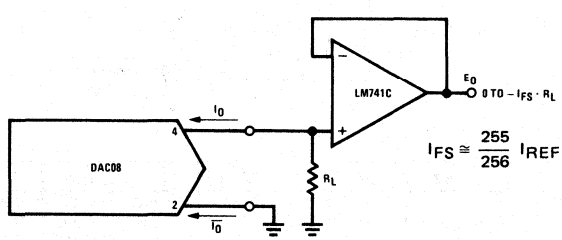
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.920

FIGURE 20. Symmetrical Offset Binary Operation



For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

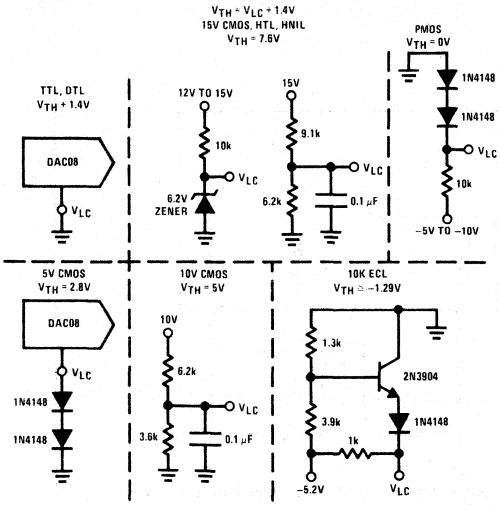
FIGURE 21. Positive Low Impedance Output Operation



For complementary output (operation as a negative logic DAC) connect non-inverting input of op amp to $\overline{I_O}$ (pin 2); connect I_O (pin 4) to ground.

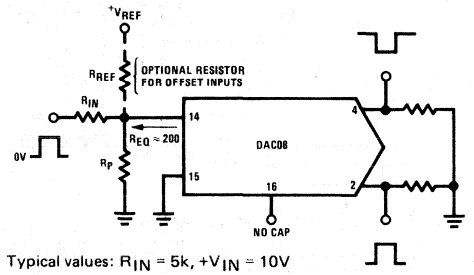
FIGURE 22. Negative Low Impedance Output Operation

Typical Applications (Continued)



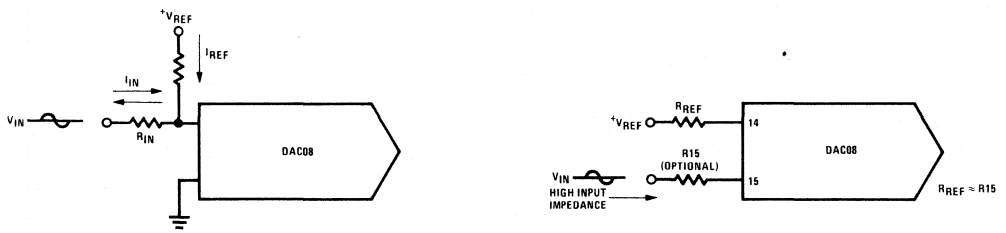
Note. Do not exceed negative logic input range of DAC.

FIGURE 23. Interfacing with Various Logic Families



Typical values: $R_{IN} = 5k$, $+V_{IN} = 10V$

FIGURE 24. Pulsed Reference Operation



(a) $I_{REF} \geq$ peak negative swing of I_{IN}

(b) $+V_{REF}$ must be above peak positive swing of V_{IN}

FIGURE 25. Accommodating Bipolar References

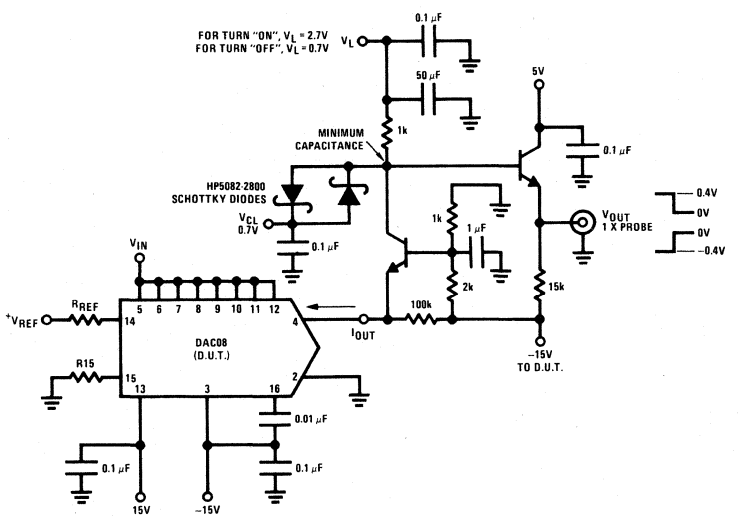
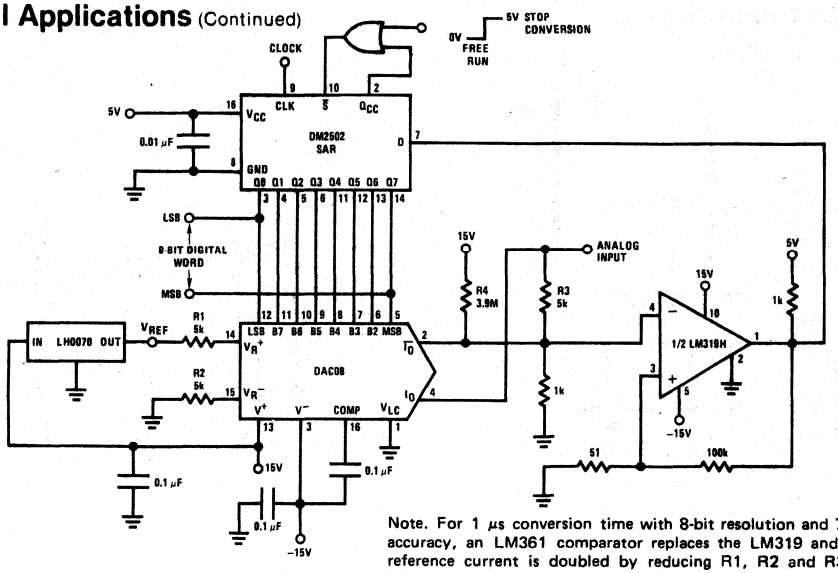


FIGURE 26. Settling Time Measurement

Typical Applications (Continued)



Note. For 1 μs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

FIGURE 27. A Complete 2 μs Conversion Time, 8-Bit A/D Converter

National Semiconductor

DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

General Description

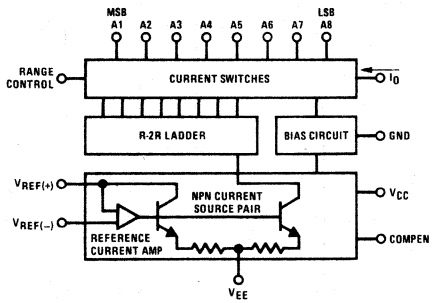
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

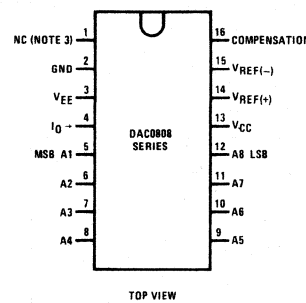
Features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Typical Application

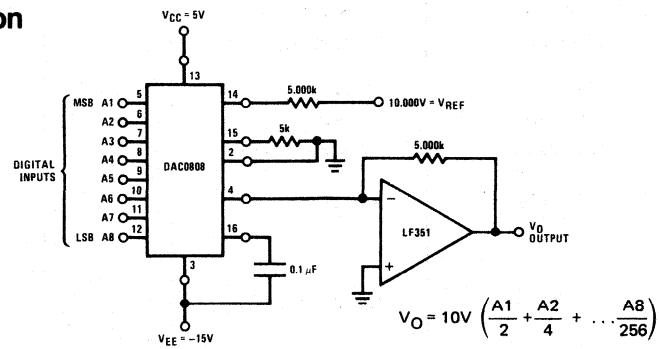


FIGURE 1. ±10V Output Digital to Analog Converter

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS*					
		D PACKAGE (D16C)		J PACKAGE (J16A)		N PACKAGE (N16A)	
8-bit	$-55°C \leq T_A \leq +125°C$	DAC0808LD	LM1508D-8				
8-bit	$0°C \leq T_A \leq +75°C$			DAC0808LCJ	LM1408J-8	DAC0808LCN	LM1408N-8
7-bit	$0°C \leq T_A \leq +75°C$			DAC0807LCJ	LM1408J-7	DAC0807LCN	LM1408N-7
6-bit	$0°C \leq T_A \leq +75°C$			DAC0806LCJ	LM1408J-6	DAC0806LCN	LM1408N-6

*Note. Devices may be ordered by using either order number.

Absolute Maximum Ratings

Power Supply Voltage	
V_{CC}	+18 V_{DC}
V_{EE}	−18 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Package Limitation)	
Cavity Package	1000 mW
Derate above T_A = 25°C	6.7 mW/°C
Operating Temperature Range	
DAC0808L	−55°C ≤ T_A ≤ +125°C
DAC0808LC Series	0 ≤ T_A ≤ +75°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808L: T_A = −55°C to +125°C, DAC0808LC, DAC0807LC, DAC0806LC, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

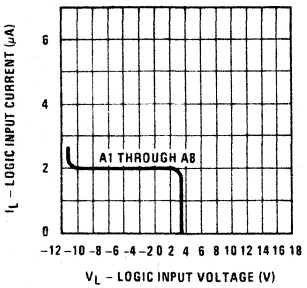
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808L (LM1508-8), DAC0808LC (LM1408-8)				±0.19	%
	DAC0807LC (LM1408-7), (Note 1)				±0.39	%
	DAC0806LC (LM1408-6), (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	T_A = 25°C (Note 2), *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, *(Figure 3)*	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance Pin 1 Grounded,	E_r ≤ 0.19%, T_A = 25°C			−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}
SRI_{REF}	Reference Current Slew Rate	*(Figure 6)*		8		mA/μs
	Output Current Power Supply Sensitivity	−5V ≤ V_{EE} ≤ −16.5V		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

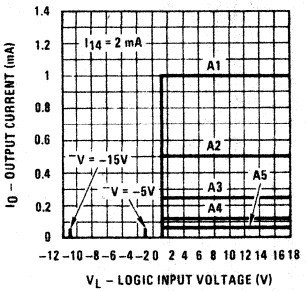
Typical Performance Characteristics

V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

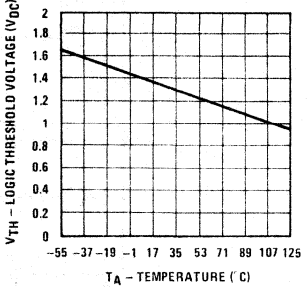
Logic Input Current vs Input Voltage



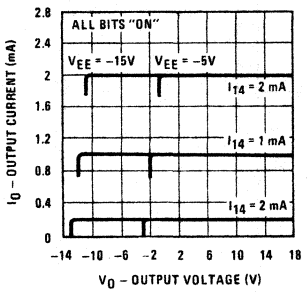
Bit Transfer Characteristics



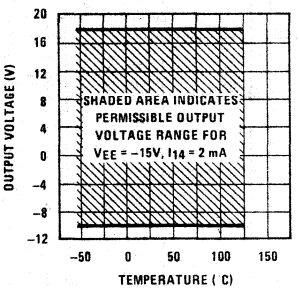
Logic Threshold Voltage vs Temperature



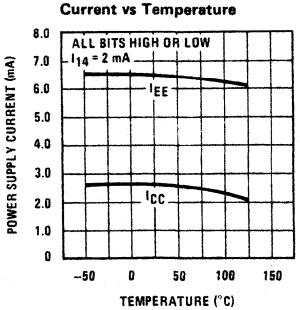
Output Current vs Output Voltage (Output Voltage Compliance)



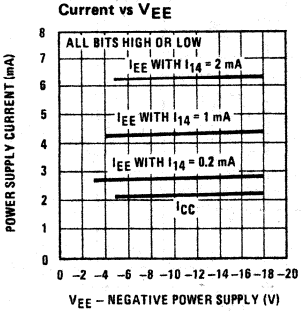
Output Voltage Compliance vs Temperature



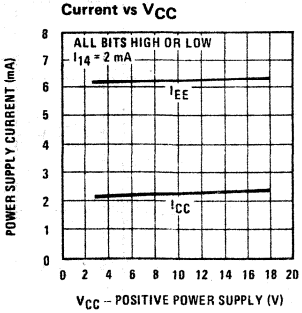
Typical Power Supply Current vs Temperature



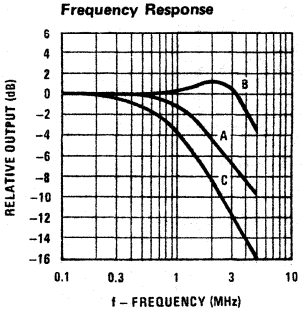
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

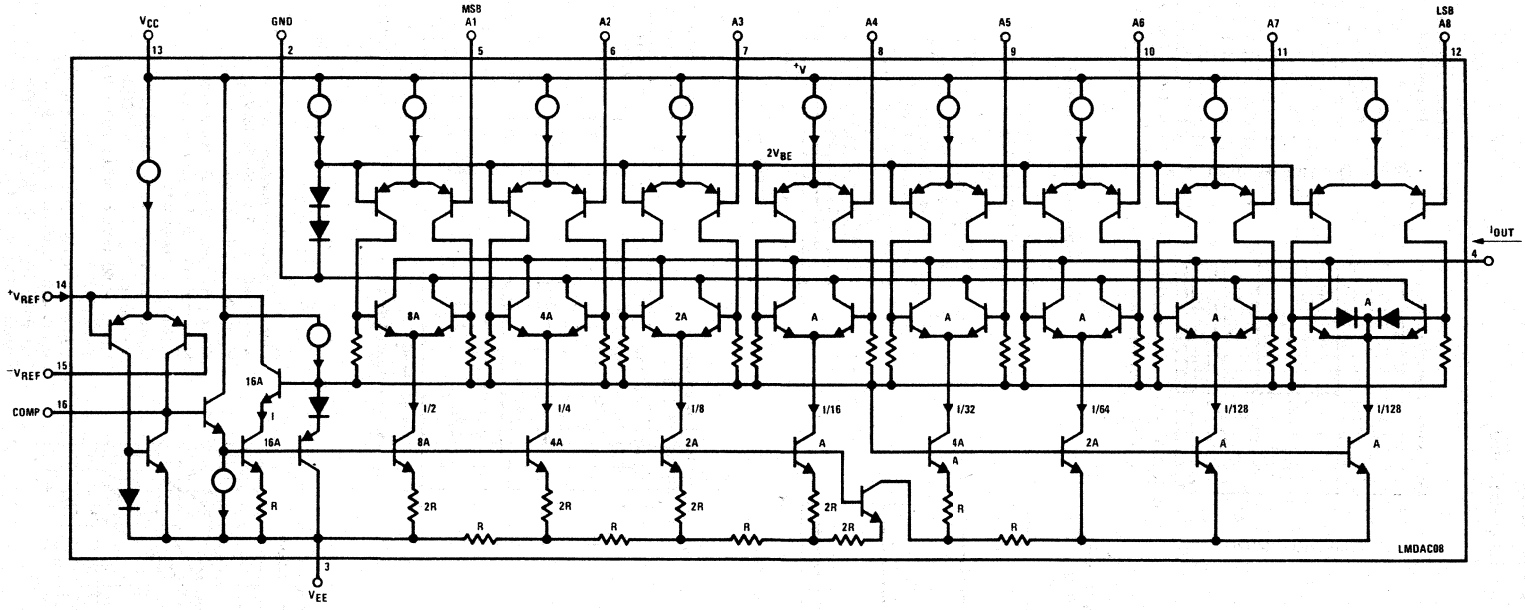
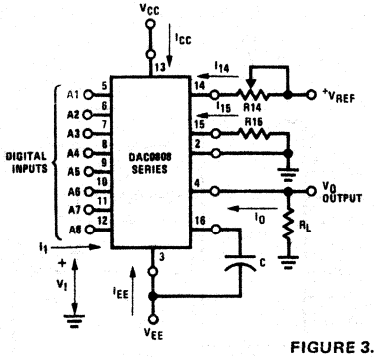


FIGURE 2. Equivalent Circuit of the DAC0808 Series

Test Circuits



V_I and I_I apply to inputs A1–A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level

A_N = "0" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit

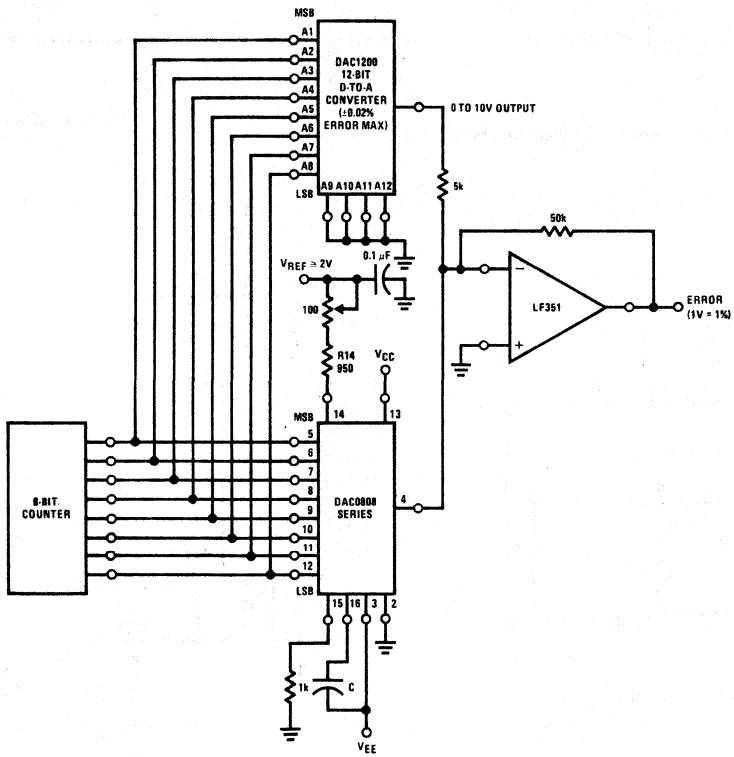


FIGURE 4. Relative Accuracy Test Circuit

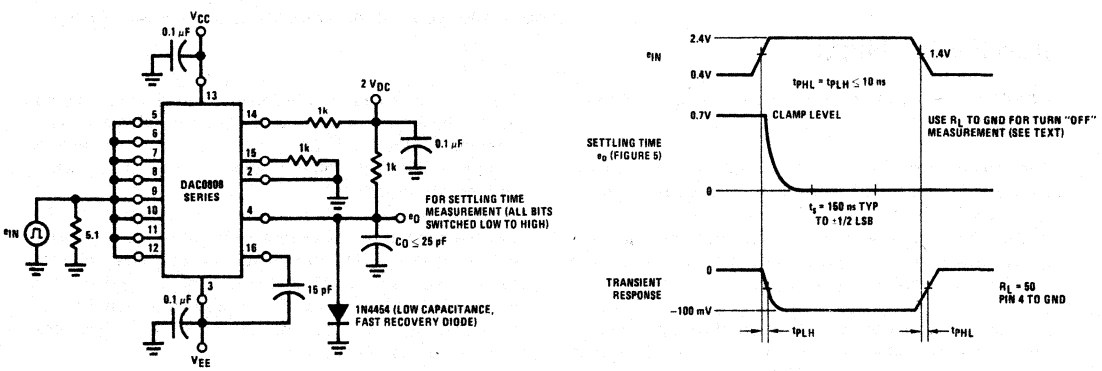


FIGURE 5. Transient Response and Settling Time

Test Circuits (Continued)

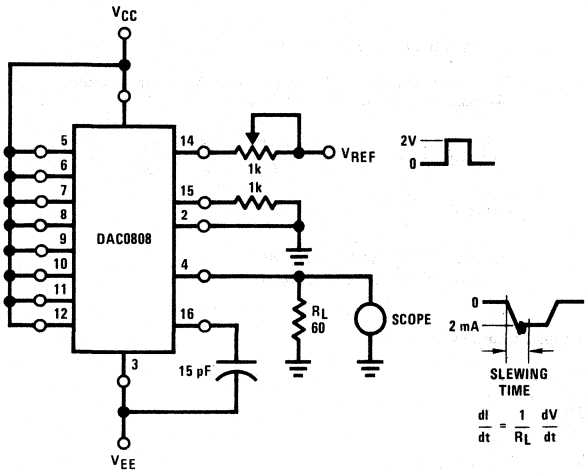


FIGURE 6. Reference Current Slew Rate Measurement

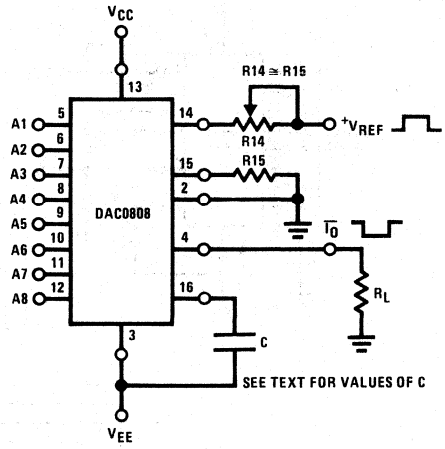


FIGURE 7. Positive V_{REF}

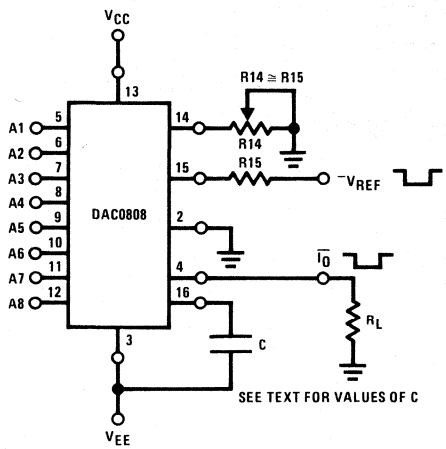


FIGURE 8. Negative V_{REF}

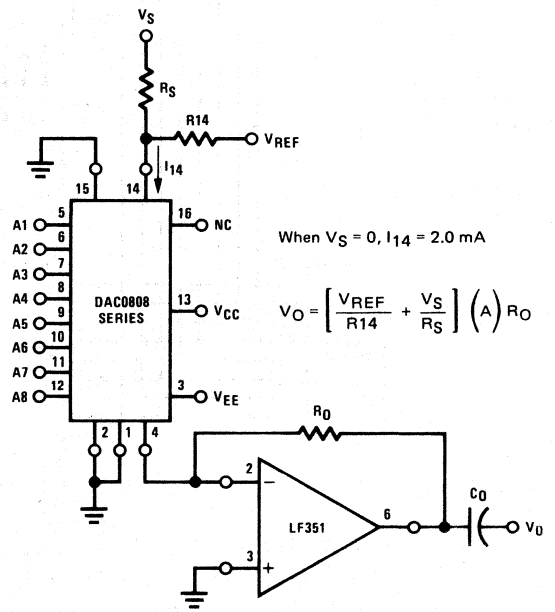


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

Application Hints (Continued)

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to 0.5V when V_{EE} = −5V due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −7V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536, or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 100 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactoy test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

National Semiconductor

Digital-to-Analog Converters
PRELIMINARY

DAC0830, DAC0831, DAC0832 MICRO-DAC™: 8-Bit μP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z-80, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DAC's (MICRO-DAC'sTM). For applications demanding higher resolution, the DAC1000 series (10-bits) and the DAC1208 and DAC1230 (12-bits) are available alternatives.

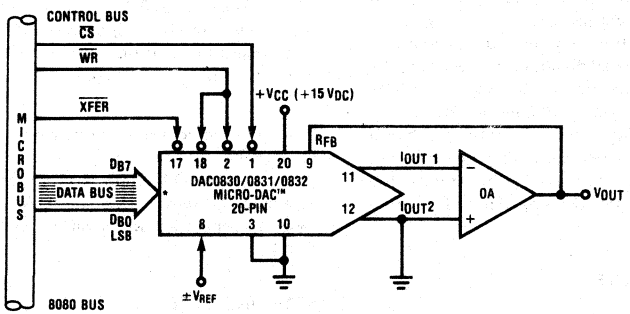
Features

- Linearity specified with full scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow-through digital data inputs
- Loads one 8-bit word
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference-full 4-quadrant multiplication
- Operates "STAND ALONE" (without μP) if desired

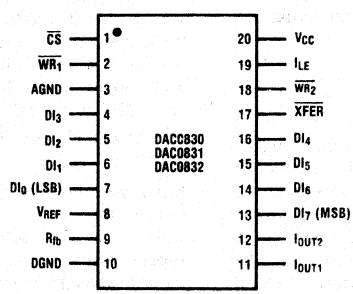
Key Specifications

■ Current settling time	1 μs
■ Resolution	8-bits
■ Linearity (guaranteed over temp.)	8, 9, or 10 bits
■ Gain Tempco	0.0002% FS/°C
■ Low power dissipation	20 mW
■ Single power supply	5 to 15 V_{DC}

Typical Application



Pin Configuration Top View



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at any digital input	V_{CC} to GND
Voltage at V_{REF} input	±25V
Storage temperature range	−65 °C to +150 °C
Package dissipation at T_A = 25 °C (Note 3)	500 mW
DC voltage applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead temperature (soldering, 10 seconds)	300 °C

Operating Ratings

Temperature Range	
Part numbers with 'LCN' suffix	0 °C to 70 °C
Part numbers with 'LCD' suffix	−40 °C to +85 °C
Part numbers with 'LD' Suffix	−55 °C to +125 °C
Voltage at any digital input	V_{CC} TO GND

General Electrical Characteristics T_A = 25°C, V_{REF} = 10.000 V_{DC} unless otherwise noted

Parameter	Conditions	See Note	V_{CC} = 12V_{DC} ± 5% to 15V_{DC} ± 5%			V_{CC} = 5V_{DC} ± 5%			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Resolution			8	8	8	8	8	8	bits
Linearity Error	Zero and full scale adjusted	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \leq V_{REF} \leq +10V$	5							
	DAC0830				0.05			0.05	% of FSR
	DAC0831				0.1			0.1	% of FSR
	DAC0832				0.2			0.2	% of FSR
Differential Nonlinearity	Zero and full scale adjusted	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \leq V_{REF} \leq +10V$	5							
	DAC0830				0.1			0.1	% of FSR
	DAC0831				0.2			0.2	% of FSR
	DAC0832				0.4			0.4	% of FSR
Monotonicity	$T_{MIN} < T_A < T_{MAX}$	4,6							
	$-10V \leq V_{REF} \leq +10V$	5	8	8	8	8	8	8	bits
Gain Error	Using internal R_{fb}								
	$-10V \leq V_{REF} \leq +10V$	5	−1.0	±0.2	1.0	−1.0	±0.2	1.0	% of FS
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$	6							
	Using internal R_{fb}	10		0.0002	0.0006		0.0002	0.0006	% of FS/°C
Power Supply Rejection	All digital inputs latched high								
	V_{CC} = 14.5V to 15.5V			0.0002					% FSR/V
	11.5V to 12.5V			0.0006					% FSR/V
	4.5V to 5.5V						0.0130		%FSR/V
Reference Input Resistance			10	15	20	10	15	20	kΩ
Output Feedthrough Error	V_{REF} = 20V_{P-P}, f = 100 kHz All data inputs latched low								
	D Package	9		3			3		mV_{P-P}
	N Package			3			3		mV_{P-P}
Output Capacitance I_{OUT1}	All data inputs			70			70		pF
I_{OUT2}	latched low			200			200		pF
I_{OUT1}	All data inputs			200			200		pF
I_{OUT2}	latched high			70			70		pF
Supply Current Drain	$T_{MIN} \leq T_A \leq T_{MAX}$	6		1.2	2.0		1.2	2.0	mA

General Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\,V_{DC}$ unless otherwise noted

Parameter		Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$			$V_{CC} = 5V_{DC} \pm 5\%$			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{OUT1}	$T_{MIN} \leq T_A \leq T_{MAX}$	6							
		All data inputs latched low	11			100			100	nA
	I_{OUT2}	All data inputs latched high				100			100	nA
Digital Input Voltages		$T_{MIN} \leq T_A \leq T_{MAX}$	6							
		Low Level								
		LD suffix				0.8			0.6	V_{DC}
		Parts with LCD or LCN suffix				0.8			0.8	V_{DC}
		High Level-All Parts		2.0			2.0			V_{DC}
Digital Input Currents		$T_{MIN} \leq T_A \leq T_{MAX}$	6							
		Digital inputs < 0.8V			−50	−200		−50	−200	μA_{DC}
		Digital inputs > 2.0V			0.1	+10		0.1	+10	μA_{DC}
Current Settling Time	t_S	$V_{IL} = 0V$, $V_{IH} = 5V$			1.0			1.0		μs
Write and XFER Pulse Width	t_W	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	8	320	60		320	250		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$	10	320	100		500	350		ns
Data Set Up Time	t_{DS}	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	10	320	60		320	250		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		320	100		500	350		ns
Data Hold Time	t_{DH}	$V_{IL} = 0V$, $V_{IH} = 5V$ $T_A = 25°C$	10	90	50		300	200		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		90	60		350	260		ns
Control Set Up Time	t_{CS}	$V_{IL} = 0V$, $V_{IL} = 5V$, $T_A = 25°C$	10	320	60		320	250		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		320	100		500	350		ns
Control Hold Time	t_{CH}	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	10	10			10			ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		10			10			ns

Note 1: "*Absolute Maximum Ratings*" are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these "*Absolute Maximum*" limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} - V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\,V_{DC}$ and $V_{REF} = \pm 1\,V_{DC}$.

Note 6: $T_{MIN} = 0°C$ and $T_{MAX} = 70°C$ for "LCN" suffix parts.
$T_{MIN} = -40°C$ and $T_{MAX} = 85°C$ for "LCD" suffix parts.
$T_{MIN} = -55°C$ and $T_{MAX} = 125°C$ for "LD" suffix parts.

Note 7: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC0830 is "0.05% of FSR (MAX)." This guarantees that after performing a zero and full scale adjustment (See Sections 2.5 and 2.6), the plot of the 256 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

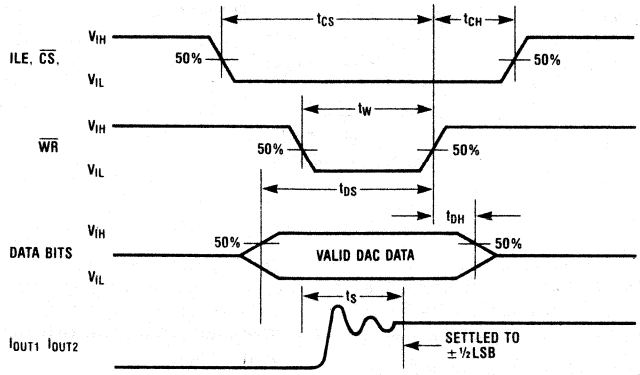
Note 8: This specification implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating, the feedthrough is typically 6 mV.

Note 10: Guaranteed by design but not tested.

Note 11: A 100 nA leakage current with $R_{fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(100 \times 10^{-9} \times 20 \times 10^3) \times 100/10$ which is 0.02% of FS.

Switching Waveforms:



Definition of Package Pinouts

Control Signals (All control signals level actuated)

$\overline{CS}$: Chip Select (active low). The $\overline{CS}$ in combination with ILE will enable $\overline{WR_1}$.

ILE: Input Latch Enable (active high). The ILE in combination with CS enables $\overline{WR_1}$.

$\overline{WR_1}$: Write 1. The active low $\overline{WR_1}$ is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR_1}$ is high. To update the input latch — $\overline{CS}$ and $\overline{WR_1}$ must be low while ILE is high.

$\overline{WR_2}$: Write 2 (active low). This signal, in combination with $\overline{XFER}$, causes the 8-bit data which is available in the input latch to transfer to the DAC register.

$\overline{XFER}$: Transfer control signal (active low).The $\overline{XFER}$ will enable $\overline{WR_2}$.

Other Pin Functions

DI_0-DI_7: Digital Inputs. DI_0 is the least significant bit (LSB) and DI_7 is the most significant bit (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} =$ constant (I full scale for a fixed reference voltage).

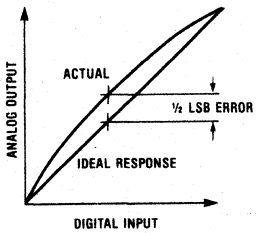
R_{fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of +10 to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

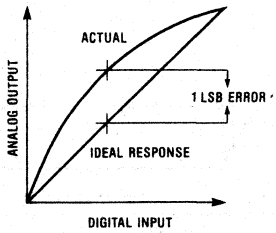
V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from +5 to +15V_{DC}. Operation is optimum for +15V_{DC}.

AGND: Analog Ground. This is the ground for the analog circuitry. This pin must always be connected to the digital ground potential.

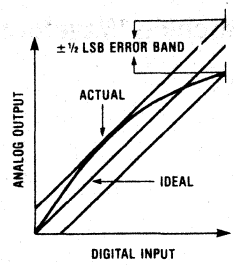
DGND: Digital Ground. This is the ground for the digital logic.



a) End point test after zero and fs adj.



b) Best straight line



c) Shifting fs adj. to pass best straight line test

Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC0830 has 2^8 or 256 steps and therefore has 8-bit resolution.

Linearity Error: Linearity Error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity "end point test" (a) and the "best straight line" test (b,c) used by other suppliers are illustrated above. The "end point test" greatly simplifies the adjustment procedure by eliminating the need for multiple iterations of checking the linearity and then adjusting full scale until the linearity is met. The "end point test" guarantees that linearity is met after a single full scale adjust. (One adjustment vs. multiple iterations of the adjustment.) The "end point test" uses a standard zero and F.S. adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within ± ½LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC0830 series, full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 39\,mV = 9.961V$. Full-scale error is adjustable to zero.

Differential Nonlinearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential nonlinearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. An 8-bit DAC which is monotonic to 8 bits simply means that increasing digital input codes will produce an increasing analog output.

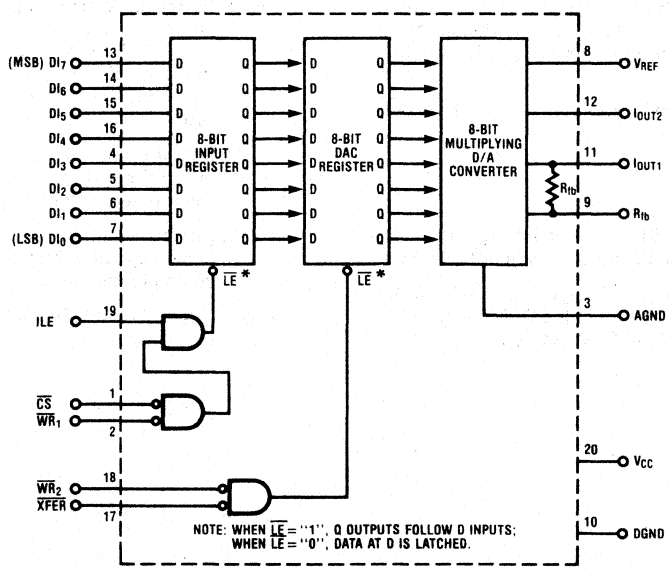
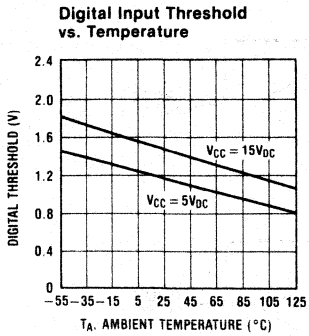
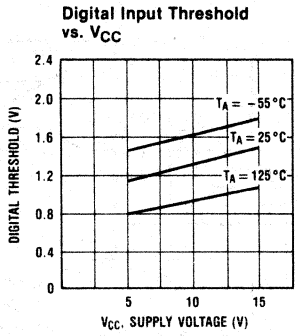
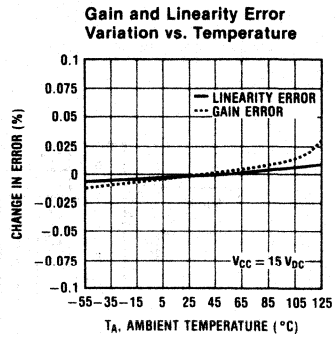
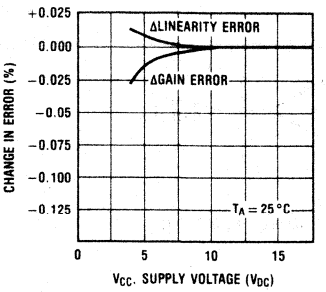


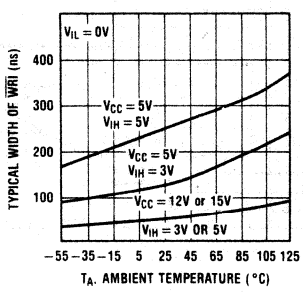
Figure 1. DAC0830 Functional Diagram

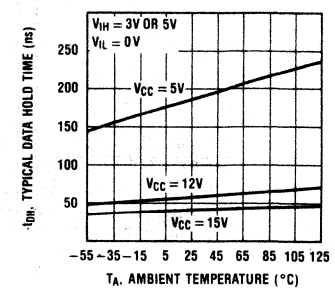












DAC0830 Series Application Hints

These DAC's are the industry's first microprocessor compatible, double-buffered 8-bit multiplying D to A converters. Double-buffering allows the utmost application flexibility from a digital control point of view. This 20-pin device is also pin for pin compatible (with one exception) with the DAC1230, a 12-bit MICRO-DAC™. In the event that a system's analog output resolution and accuracy must be upgraded, substituting the DAC1230 can eliminate hardware changes. Should this be necessary, only control software would have to be modified to output 12-bit DAC data in two bytes instead of a single 8-bit byte. The one pin function exception is that the ILE pin of the DAC0830 (See Section 1.1) is used as a BYTE1/$\overline{\text{BYTE2}}$ control for the DAC1230.

Analog signal control versatility is provided by a precision R-2R ladder network which allows full 4-quadrant multiplication of a wide range bipolar reference voltage by an applied digital word.

1.0 Digital Considerations

A most unique characteristic of these DAC's is that the 8-bit digital input byte is double-buffered. This means that the data must transfer through two independently controlled 8-bit latching registers before being applied to the R-2R ladder network to change the analog output. The addition of a second register allows two useful control features. First, any DAC in a system can simultaneously hold the current DAC data in one register (DAC register) and the next data word in the second register (input register) to allow fast updating of the DAC output on demand. Second, and probably more important, double-buffering allows any number of DAC's in a system to be updated to their new analog output levels simultaneously via a common strobe signal.

The timing requirements and logic level convention of the register control signals have been designed to minimize or eliminate external interfacing logic when applied to most popular microprocessors and development systems. It is easy to think of these converters as 8-bit "write only" memory locations that provide an analog output quantity. All inputs to these DAC's meet TTL voltage level specs and can also be driven directly with high voltage CMOS logic in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. If any of the digital inputs are inadvertantly left floating, the DAC interprets the pin as a logic "1".

1.1 Double-Buffered Operation

Updating the analog output of these DAC's in a double-buffered manner is basically a two step or double write operation. In a microprocessor system two unique system addresses must be decoded, one for the input latch controlled by the $\overline{\text{CS}}$ pin and a second for the DAC latch which is controlled by the $\overline{\text{XFER}}$ line. If more than one DAC is being driven, Figure 2, the $\overline{\text{CS}}$ line of each DAC would typically be decoded individually, but all of the converters could share a common $\overline{\text{XFER}}$ address to allow simultaneous updating of any number of DAC's. The timing for this operation is shown, Figure 3.

It is important to note that the analog outputs that will change after a simultaneous transfer are those from the DAC's whose input register had been modified prior to the $\overline{\text{XFER}}$ command.

The ILE pin is an active high chip select which can be decoded from the address bus as a qualifier for the normal $\overline{\text{CS}}$ signal generated during a write operation. This can

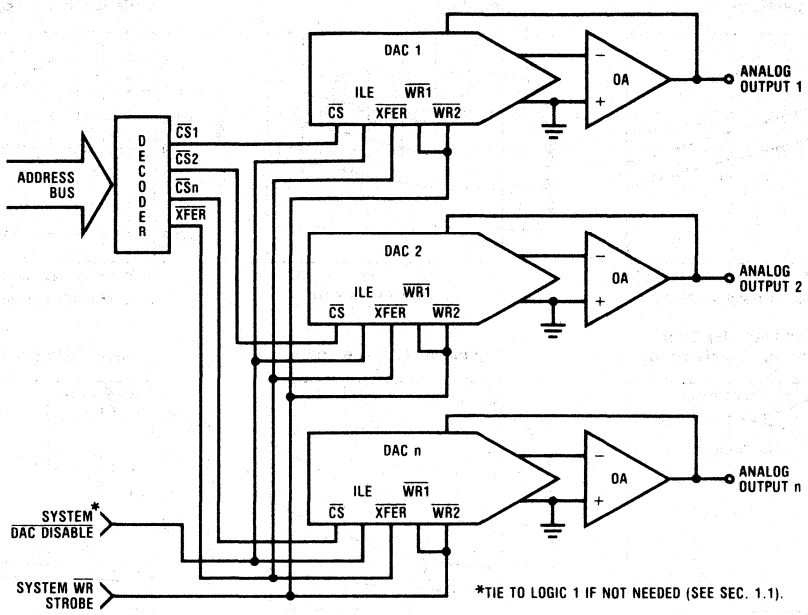


Figure 2. Controlling Multiple DAC's

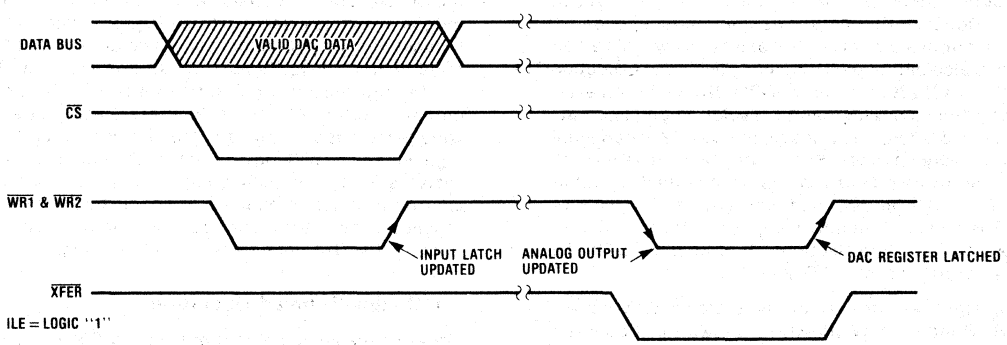


Figure 3.

be used to provide a higher degree of decoding unique control signals for a particular DAC, and thereby create a more efficient addressing scheme.

Another useful application of the ILE pin of each DAC in a multiple DAC system is to tie these inputs together and use this as a control line that can effectively "freeze" the outputs of all the DAC's at their present value. Pulling this line low latches the input register and prevents new data from being written to the DAC. This can be particularly useful in multiprocessing systems to allow a processor other than the one controlling the DAC's to take over control of the data bus and control lines. If this second system were to use the same addresses as those decoded for DAC control (but for a different purpose) the ILE function would prevent the DAC's from being erroneously altered.

In a "Stand-Alone" system the control signals are generated by discrete logic. In this case double-buffering can be controlled by simply taking $\overline{CS}$ and $\overline{XFER}$ to a logic "0", ILE to a logic "1" and pulling $\overline{WR_1}$ low to load data to the input latch. Pulling $\overline{WR_2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.

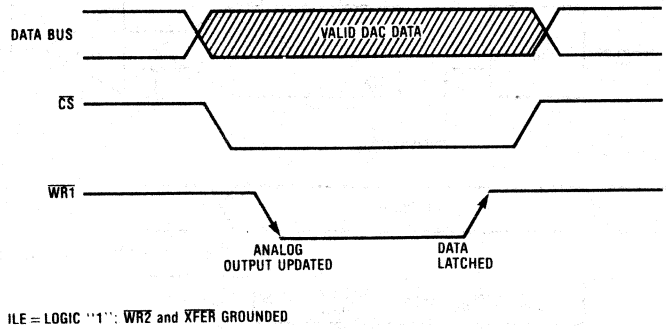


Figure 4.

1.2 Single-Buffered Operation

In a microprocessor controlled system where maximum data throughput to the DAC is of primary concern, or when only one DAC of several needs to be updated at a time, a single-buffered configuration can be used. One of the two internal registers allows the data to flow through and the other register will serve as the data latch.

Digital signal feedthrough (see Section 1.5) is minimized if the input register is used as the data latch. Timing for this mode is shown in figure 4.

Single-buffering in a "stand-alone" system is achieved by strobing $\overline{WR_1}$ low to update the DAC with $\overline{CS}$, $\overline{WR_2}$ and $\overline{XFER}$ grounded and ILE tied high.

1.3 Flow-Through Operation

Though primarily designed to provide microprocessor interface compatibility, the MICRO-DAC's can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary up-down counter, or in function generation circuits where a ROM is continuosly providing DAC data.

Simply grounding $\overline{CS}$, $\overline{WR_1}$, $\overline{WR_2}$, and $\overline{XFER}$ and tying ILE high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.4 Control Signal Timing

When interfacing these MICRO-DAC's to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 500 ns for all valid operating conditions of supply voltage and ambient temperature, but typically a pulse width of only 100 ns is adequate if $V_{CC} = 15V_{DC}$. A second consideration is that the guaranteed minimum data hold time of 90 ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulsewidth. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in Figure 5 for an exemplary system which provides a 250 ns $\overline{WR}$ strobe time with a data hold time of only 10 ns.

The proper data set-up time prior to the latching edge (LO to HI transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulsewidth is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

1.5 Digital Signal Feedthrough

When data is latched in the internal registers, but the digital inputs are changing state, a narrow spike of current may flow out of the current output terminals. This spike is caused by the rapid switching of internal logic gates that are responding to the input changes.

There are several recommendations to minimize this effect. When latching data in the DAC, always use the input register as the latch. Second, reducing the V_{CC} supply for the DAC from +15 volts to the +5V offers a factor of 5 improvement in the magnitude of the feedthrough, but at the expense of internal logic switching speed. Finally, increasing C_C (Figure 8) to a value consistent with the actual circuit bandwidth requirements can provide a substantial damping effect on any output spikes.

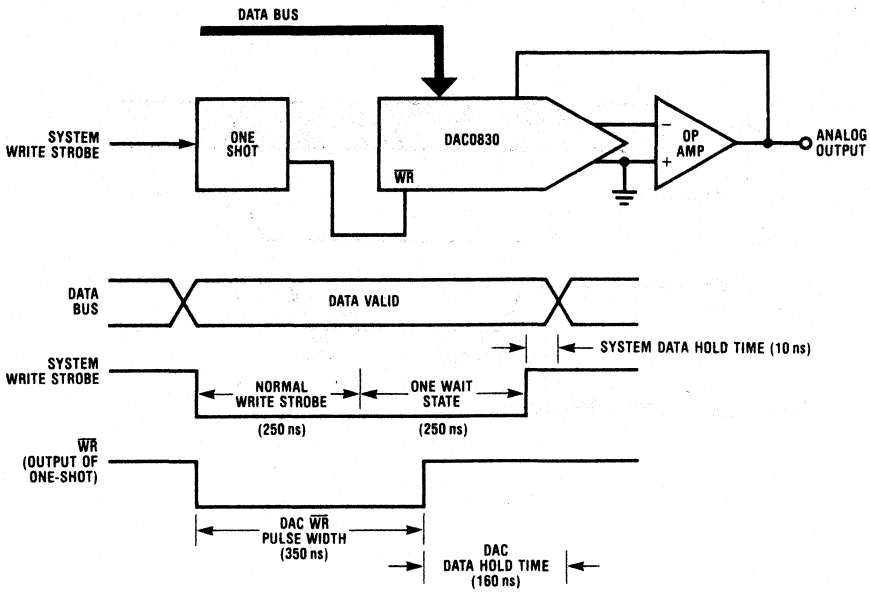


Figure 5. Accommodating a High Speed System

2.0 Analog Considerations

The fundamental purpose of any D to A converter is to provide an accurate analog output quantity which is representative of the applied digital word. In the case of the DAC0830, the output, I_{OUT1}, is a current directly proportional to the product of the applied reference voltage and the digital input word. For application versatility, a second output, I_{OUT2}, is provided as a current directly proportional to the complement of the digital input. Basically:

$$I_{OUT1} = \frac{V_{REF}}{15\,k\Omega} \times \frac{\text{Digital Input}}{256};$$

$$I_{OUT2} = \frac{V_{REF}}{15\,k\Omega} \times \frac{255 - \text{Digital Input}}{256}$$

where the digital input is the decimal (base 10) equivalent of the applied 8-bit binary word (0 to 255), V_{REF} is the voltage at pin 8 and 15kΩ is the nominal value of the internal resistance, R, of the R-2R ladder network (discussed in Section 2.1).

Several factors external to the DAC itself must be considered to maintain analog accuracy and are covered in subsequent sections.

2.1 The Current Switching R-2R Ladder

The analog circuitry, Figure 6, consists of a silicon-chromium (SiCr or Si-chrome) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there are no parasitic diode problems with the ladder (as there may be with diffused resistors) so the reference voltage, V_{REF}, can range −10V to +10V even if V_{CC} for the device is $5V_{DC}$.

The digital input code to the DAC simply controls the position of the SPDT current switches and steers the available ladder current to either I_{OUT1} or I_{OUT2} as determined by the logic input level ("1" or "0") respectively, as shown in Figure 6. The MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant muliplying feature of this DAC.

2.2 Basic Unipolar Output Voltage

To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential ($0V_{DC}$) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in Figure 7.

The inverting input of the op amp is a "virtual ground" created by the feedback from its output through the internal 15kΩ resistor, R_{fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage souce or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than or equal to the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15kΩ to ground to external circuitry.

Always use the internal R_{fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

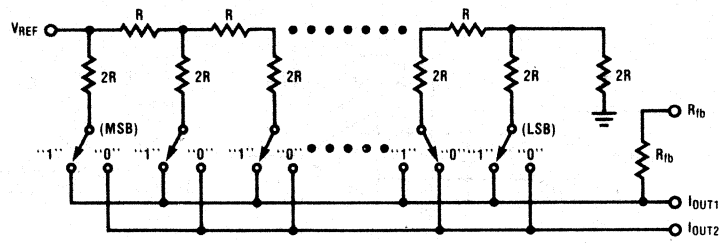


Figure 6.

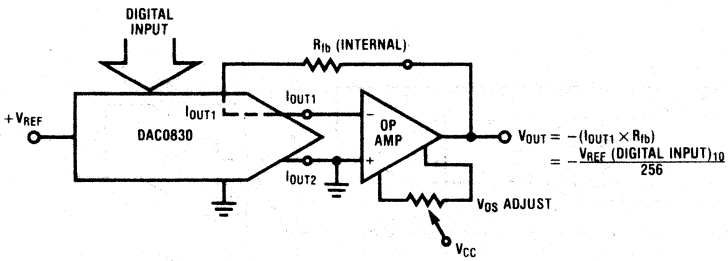


Figure 7.

2.3 Op Amp Considerations

The op amp used in Figure 7 should have offset voltage nulling capability (See Section 2.5).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET™* op amps are highly recommended for use with these DACs because of their very low input current.

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in Figure 8, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

Finally, the output voltage swing of the amplifier must be greater than V_{REF} to allow reaching the full scale output voltage. Depending on the loading on the output of the amplifier and the available op amp supply voltages (only ±12 volts in many development systems), a reference voltage less than 10 volts may be necessary to obtain the full analog output voltage range.

*BI-FET is a trademark of National Semiconductor Corporation.

2.4 Bipolar Output Voltage with a Fixed Reference

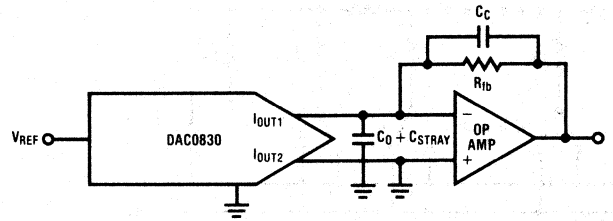
The addition of a second op amp to the previous circuitry can be used to generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word and allows two-quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication: $\pm V_{REF} \times \pm$Digital Code $= \mp V_{OUT}$. This circuit is shown in Figure 9.

This configuration features several improvements over existing circuits for bipolar outputs with other multiplying DAC's. Only the offset voltage of amplifier 1 has to be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp (although a constant output voltage error) has no effect on linearity. It should be nulled only if absolute output accuracy is required. Finally, the values of the resistors around the second amplifier do not have to match the internal DAC resistors, they need only to match and temperature track each other. A thin film 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. These resistors are matched to 0.1% and exhibit only 5 ppm/°C resistance tracking tempco. Two of the four available 10 kΩ resistors can be paralleled to form R in Figure 9 and the other two can be used independently as the resistances labeled 2R.

2.5 Zero Adjustment

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

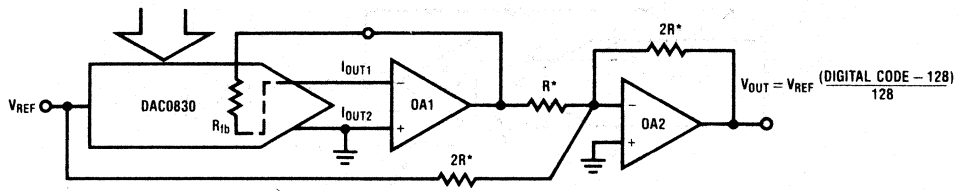
The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near $0V_{DC}$ as possible. This is accomplished for the typical DAC — op amp connection (Figure 7) by shorting out R_{fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all one's for I_{OUT2}). The short around R_{fb} is then removed and the converter is zero adjusted.



OP AMP	C_C	t_s (0 TO FULL SCALE)
LF356	22 pF	4 μs
LF351	22 pF	5 μs
LF357*	10 pF	2 μs

*3.6kΩ RESISTOR ADDED FROM (−) INPUT TO GROUND TO INSURE STABILITY

Figure 8.



$$1\ LSB = \frac{|V_{REF}|}{128}$$

INPUT CODE	IDEAL V_{OUT}	
MSB . . . LSB	$+V_{REF}$	$-V_{REF}$
1 1 1 1 1 1 1 1	$V_{REF} - 1$ LSB	$-\|V_{REF}\| + 1$ LSB
1 1 0 0 0 0 0 0	$V_{REF}/2$	$-\|V_{REF}\|/2$
1 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1	−1 LSB's	+1 LSB's
0 0 1 1 1 1 1 1	$-\frac{\|V_{REF}\|}{2} - 1$ LSB	$\frac{\|V_{REF}\|}{2} + 1$ LSB
0 0 0 0 0 0 0 0	$-\|V_{REF}\|$	$+\|V_{REF}\|$

*THESE RESISTORS ARE AVAILABLE FROM BECKMAN INSTRUMENTS, INC. AS THEIR PART NO. 694-3-R10K-D

Figure 9.

2.6 Full-Scale Adjustment

In the case where the matching of R_{fb} to the R value of the R-2R ladder (typically ±0.2%) is insufficient for full-scale accuracy in a particular application, the V_{REF} voltage can be adjusted or an external resistor and potentiometer can be added as shown in Figure 10 to provide a full-scale adjustment.

The temperature coefficients of the resistors used for this adjustment are an important concern. To prevent degradation of the gain error tempco by the external resistors, their temperature coefficients ideally would have to match that of the internal DAC resistors, which is a highly impractical constraint. For the values shown in Figure 10, if the resistor and the potentiometer each had a temperature coefficient of ±100 ppm/°C maximum, the overall gain error tempco would be degraded a maximum of 0.0025%/°C for an adjustment pot setting of less than 3% of R_{fb}.

2.7 Miscellaneous Application Hints

These converters are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to static discharge.

Conversion accuracy is only as good as the applied reference voltage so providing a stable source over time and temperature changes is an important factor to consider.

A "good" ground is most desirable. A single point ground distribution technique for analog signals and supply returns keeps other devices in a system from affecting the output of the DAC's.

During power-up supply voltage sequencing, the −15V (or −12V) supply of the op amp may appear first. This will typically cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is internally clamped to one diode drop below ground.

Careful circuit construction with minimization of lead lengths around the analog circuitry, is a primary concern. Good high frequency supply decoupling will aid in preventing inadvertant noise from appearing on the analog output.

Overall noise reduction and reference stability is of particular concern when using the higher accuracy versions, the DAC0830 and DAC0831, or their advantages are wasted.

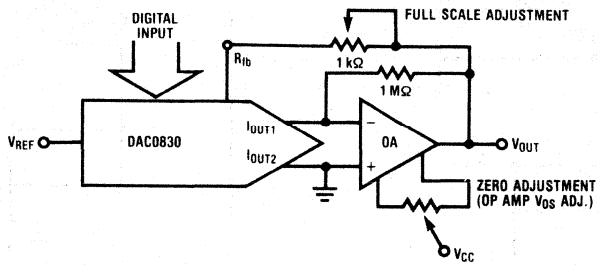
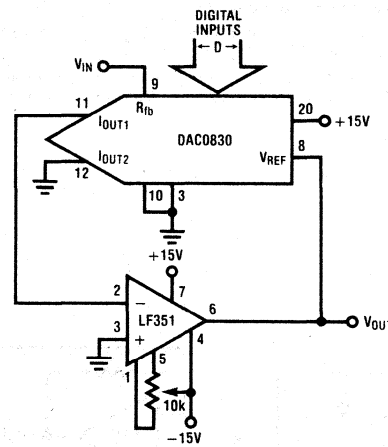


Figure 10. Adding Full-Scale Adjustment

3.0 General Application Ideas

The connections for the control pins of the digital input registers are purposely omitted. Any of the control formats discussed in Section 1 of the accompanying text will work with any of the circuits shown. The method used depends on the overall system provisions and requirements.

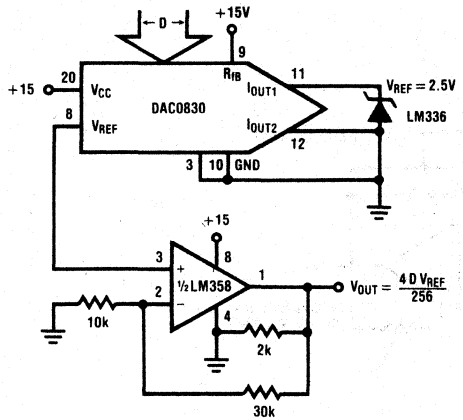
The digital input code is referred to as D and represents the decimal equivalent value of the 8-bit binary input, for example:



Binary Input Pin 13 MSB	Pin 7 LSB	D Decimal Equivalent
1 1 1 1 1 1 1 1		255
1 0 0 0 0 0 0 0		128
0 0 0 1 0 0 0 0		16
0 0 0 0 0 0 1 0		2
0 0 0 0 0 0 0 0		0

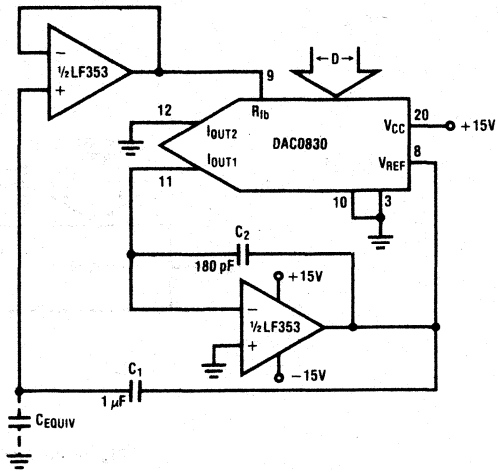
DAC Controlled Amplifier (Volume Control)

- $V_{OUT} = \frac{-V_{IN}\,(256)}{D}$
- When D = 0, the amplifier will go open loop and the output will saturate.
- Feedback impedance from the −input to the output varies from 15 kΩ to ∞ as the input code changes from full-scale to zero.



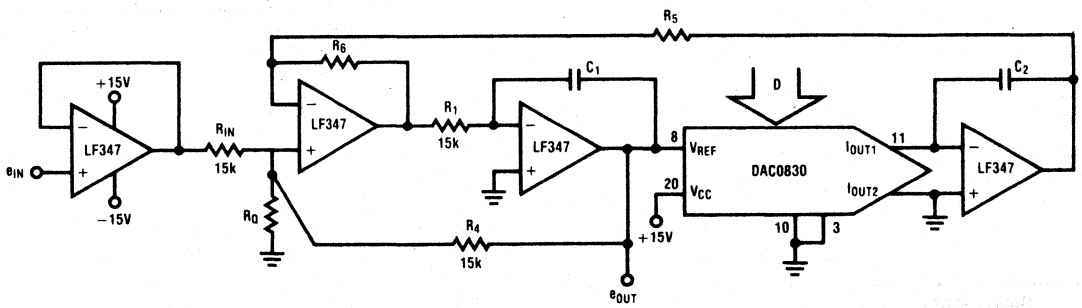
Single Supply DAC

- Uses DAC0830 in a voltage switching mode to eliminate negative supply requirement.
- V_{REF} as shown must be ⩽3V and ($V_{CC} - V_{REF}$) must be ⩾10V to preserve linearity.
- Zero code output voltage limited by the low level output saturation voltage of the op amp. The 2kΩ resistor helps reduce this voltage.



Capacitance Multiplier

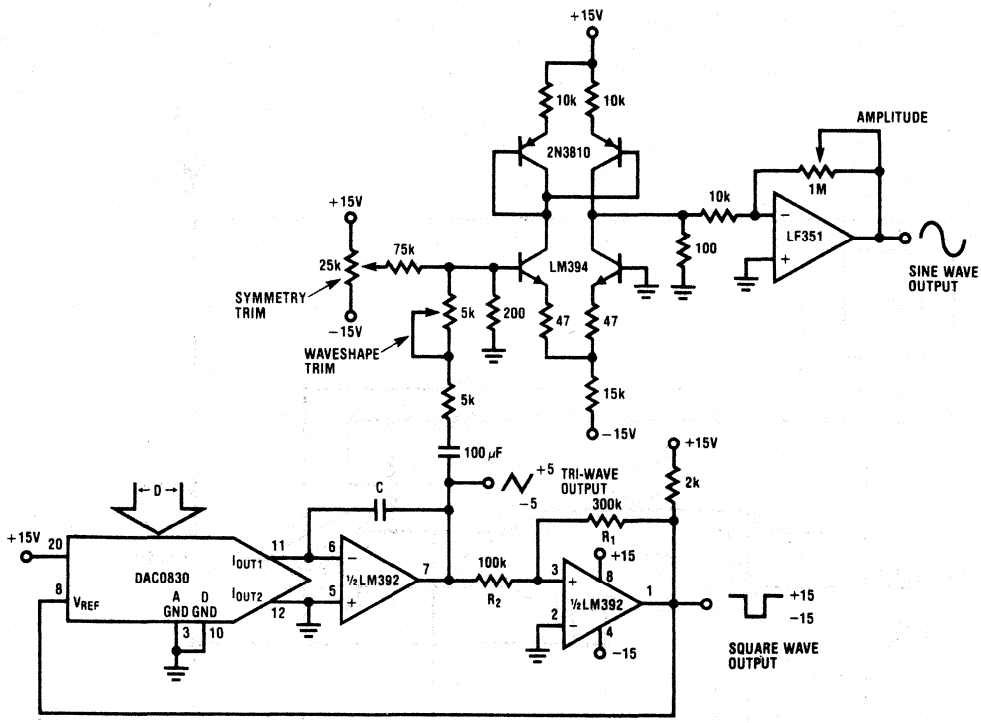
- $C_{EQUIV} = C_1 \left(1 + \frac{256}{D}\right)$
- Maximum voltage across the equivalent capacitance is limited to $\frac{V_{O\,MAX}\ (\text{op amp})}{1 + \frac{256}{D}}$
- C_2 is used to improve settling time of op amp.



Variable f_O, Variable Q_O, Constant BW Bandpass Filter

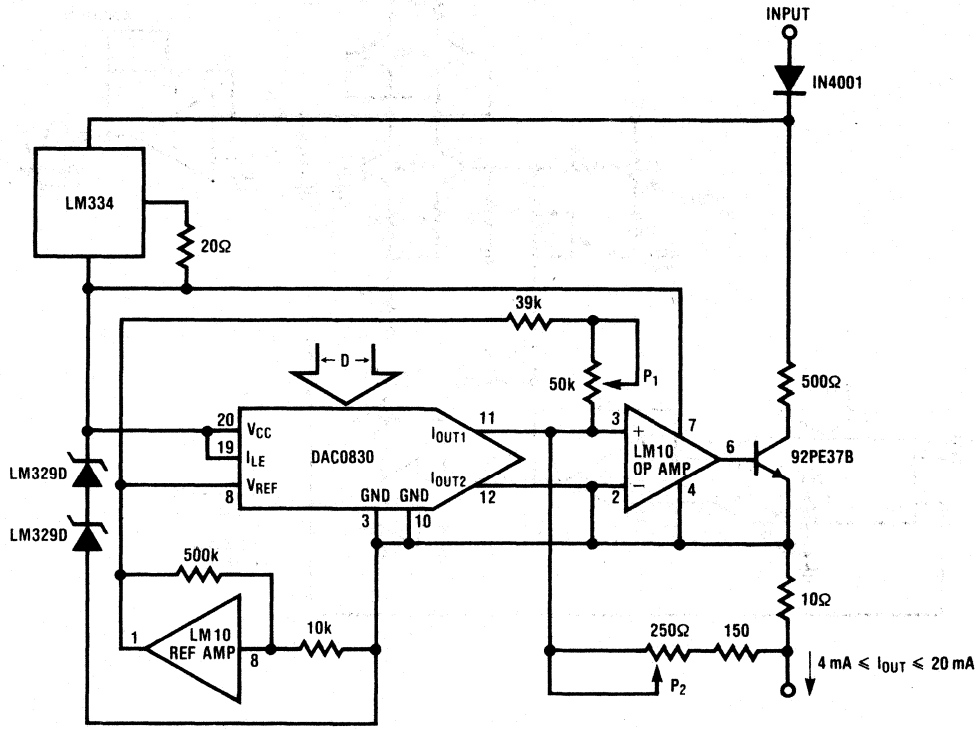
- $f_O = \frac{\sqrt{\frac{K\,D}{256}}}{2\pi R_1 C}$; $Q_O = \sqrt{\frac{K\,D}{256}} \frac{(2R_Q + R_1)}{R_Q(K+1)}$; $3\,\text{dbBW} = \frac{R_Q(K+1)}{2\pi R_1 C(2R_Q + R_1)}$

  where $C_1 = C_2 = C$; $K = \frac{R_6}{R_5}$ and $R_1 = R$ of DAC = 15k
- $H_O = 1$ for $R_{IN} = R_4 = R_1$
- Range of f_O and Q is ≈ 16 to 1 for circuit shown. The range can be extended to 255 to 1 by replacing R_1 with a second DAC0830 driven by the same digital input word.
- Maximum $f_O \times Q$ product should be ⩽ 200kHz.



DAC Controlled Function Generator

- DAC controls the frequency of sine, square, and triangle outputs.
- $f = \frac{D}{256(20k)C}$ for $V_{0MAX} = V_{0MIN}$ of square wave output and $R_1 = 3R_2$.
- 255 to 1 linear frequency range; oscillator stops with D = 0
- Trim symmetry and wave-shape for minimum sine wave distortion.



Two Terminal Floating 4 to 20 mA Current Loop Controller

- DAC0830 linearly controls the current flow from the input terminal to the output terminal to be 4 mA (for D = 0) to 20 mA (for D = 255).
- Circuit operates with a terminal voltage differential of 16V to 55V.
- P_2 adjusts the magnitude of the output current and P_1 adjusts the zero to full scale range of output current.
- Digital inputs can be supplied from a processor using opto isolators on each input or the DAC latches can flow-through (connect control lines to pins 3 and 10 of the DAC) and the input data can be set by SPST toggle switches to ground (pins 3 and 10).

Ordering Information

Temperature Range		0°C to +70°C	−40°C to +85°C	−55°C to +125°C
Linearity Error	0.05% FSR	DAC0830LCN	DAC0830LCD	DAC0830LD
	0.10% FSR	DAC0831LCN	DAC0831LCD	DAC0831LD
	0.20% FSR	DAC0832LCN	DAC0832LCD	DAC0832LD
Package Outline		N20A	D20A	D20A

National Semiconductor

DAC1000/1/2 and DAC1006/7/8 MICRO-DAC™: μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1000/1/2 and DAC1006/7/8 are advanced CMOS/Si-Cr 10-, 9- and 8-bit accurate multiplying DACs which are designed to interface directly with the 8080, 8048, 8085, Z-80 and other popular microprocessors. These DACs appear as a memory location or an I/O port to the μP and no interfacing logic is needed.

These devices, combined with an external amplifier and voltage reference, can be used as standard D/A converters; and they are very attractive for multiplying applications (such as digitally controlled gain blocks) since their linearity error is essentially independant of the voltage reference. They become equally attractive in audio signal processing equipment as audio gain controls or as programmable attenuators which marry high quality audio signal processing to digitally based systems under microprocessor control.

All of these DACs are double buffered. They can load all 10 bits or two 8-bit bytes and the data format can be either right justified or left justified. The analog section of these DACs is essentially the same as that of the DAC1020.

Part #	Accuracy (bits)	Pin	Description
DAC1000	10	24	Has all logic features
DAC1001	9		
DAC1002	8		
DAC1006	10	20	For left-justified data
DAC1007	9		
DAC1008	8		

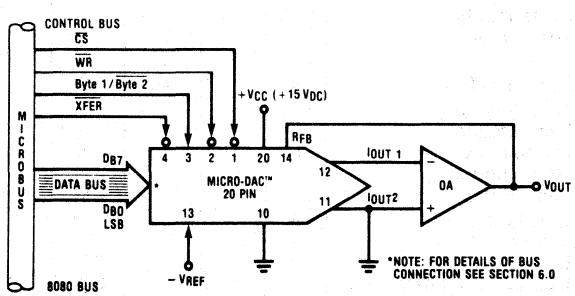
Features

- Uses easy to adjust END POINT specs, NOT BEST STRAIGHT LINE FIT
- Low power consumption
- Direct interface to all popular microprocessors.
- Integrated thin film on CMOS structure
- Double-buffered, single-buffered or flow through digital data inputs.
- Loads two 8-bit bytes or a single 10-bit word.
- Logic inputs which meet T^2L voltage level specs (1.4V logic threshold).
- Works with ±10V reference — full 4-quadrant multiplication.
- Operates STAND ALONE (without μP) if desired.
- Available in 0.3" standard 20-pin and 0.6" 24-pin package.
- Differential non-linearity selection available as special order.

Key Specifications

- Output Current Settling Time — 500ns
- Resolution — 10 bits
- Linearity — 10, 9, and 8 bits (guaranteed over temp.)
- Gain Tempco — −0.0003% of FS/°C
- Low Power Dissipation (including ladder) — 20mW
- Single Power Supply — 5 to 15 V_{DC}

Typical Application



DAC1006/1007/1008

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at any digital input	V_{CC} to GND
Voltage at V_{REF} input	±25V
Storage temperature range	−65°C to +150°C
Package dissipation at T_A = 25°C (Note 3)	500 mW
DC voltage applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead temperature (soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	
Part numbers with 'LCN' suffix	0°C to 70°C
Part numbers with 'LCD' suffix	−40°C to +85°C
Part numbers with 'LD' Suffix	−55°C to +125°C
Voltage at any digital input	V_{CC} to GND

General Electrical Characteristics T_A = 25°C, V_{REF} = 10.000 V_{DC} unless otherwise noted

Parameter	Conditions	See Note	V_{CC} = 12V_{DC} ± 5% to 15V_{DC} ± 5%			V_{CC} = 5V_{DC} ± 5%			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Resolution					10			10	bits
Linearity Error	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \leq V_{REF} \leq +10V$	5							
	DAC1000 and 1006				0.05			0.05	% of FSR
	DAC1001 and 1007				0.1			0.1	% of FSR
	DAC1002 and 1008				0.2			0.2	% of FSR
Differential Nonlinearity	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \leq V_{REF} \leq +10V$	5							
	DAC1000 and 1006				0.1			0.1	% of FSR
	DAC1001 and 1007				0.2			0.2	% of FSR
	DAC1002 and 1008				0.4			0.4	% of FSR
Monotonicity	$T_{MIN} < T_A < T_{MAX}$	4,6							
	$-10V \leq V_{REF} \leq +10V$	5							
	DAC1000 and 1006		10			10			bits
	DAC1001 and 1007		9			9			bits
	DAC1002 and 1008		8			8			bits
Gain Error	Using internal R_{fb}								
	$-10V \leq V_{REF} \leq +10V$	5	−1.0	±0.3	1.0	−1.0	±0.3	1.0	% of FS
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$	6							
	Using internal R_{fb}	10		−0.0003	−0.001		−0.0006	−0.002	% of FS/°C
Power Supply Rejection	All digital inputs latched high								
	V_{CC} = 14.5V to 15.5V			0.003	0.008				% FSR/V
	11.5V to 12.5V			0.004	0.010				% FSR/V
	4.75V to 5.25V						0.033	0.10	%FSR/V
Reference Input Resistance			10	15	20	10	15	20	kΩ
Output Feedthrough Error	V_{REF} = 20V_{P-P}, f = 100 kHz								
	All data inputs latched low								
	D Package	9		130			130		mV_{P-P}
	N Package			90			90		mV_{P-P}
Output Capacitance I_{OUT1}	All data inputs			60			60		pF
I_{OUT2}	latched low			250			250		pF
I_{OUT1}	All data inputs			250			250		pF
I_{OUT2}	latched high			60			60		pF
Supply Current Drain	$T_{MIN} \leq T_A \leq T_{MAX}$	6		0.5	2.0		0.5	2.0	mA
Output Leakage Current	$T_{MIN} \leq T_A \leq T_{MAX}$	6							
I_{OUT1}	All data inputs latched low	11			200			200	nA
I_{OUT2}	All data inputs latched high				200			200	nA
Digital Input Voltages	$T_{MIN} \leq T_A \leq T_{MAX}$	6							
	Low level								
	LD suffix				0.8			0.6	V_{DC}
	LCD or LCN suffix				0.8			0.8	V_{DC}
	High level (all parts)		2.0			2.0			V_{DC}

General Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\,V_{DC}$ unless otherwise noted

Parameter		Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$			$V_{CC} = 5V_{DC} \pm 5\%$			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Digital Input Currents		$T_{MIN} \leq T_A \leq T_{MAX}$	6							
		Digital inputs < 0.8V			−40	−150		−40	−150	μA_{DC}
		Digital inputs > 2.0V			1.0	+10		1.0	+10	μA_{DC}
Current Settling Time	t_S	$V_{IL} = 0V$, $V_{IH} = 5V$			500			500		ns
Write and XFER Pulse Width	t_W	$V_{IL} = 0V$, $V_{IH} = 5V$,								
		$T_A = 25°C$	8	150	60		320	200		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$	10	320	100		500	250		ns
Data Set Up Time	t_{DS}	$V_{IL} = 0V$, $V_{IH} = 5V$,								
		$T_A = 25°C$	10	150	80		320	170		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		320	120		500	250		ns
Data Hold Time	t_{DH}	$V_{IL} = 0V$, $V_{IH} = 5V$								
		$T_A = 25°C$	10	200	100		320	220		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		250	120		500	320		ns
Control Set Up Time	t_{CS}	$V_{IL} = 0V$, $V_{IL} = 5V$,								
		$T_A = 25°C$	10	150	60		320	180		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		320	100		500	260		ns
Control Hold Time	t_{CH}	$V_{IL} = 0V$, $V_{IH} = 5V$,								
		$T_A = 25°C$	10	10	0		10	0		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		10	0		10	0		ns

Note 1: *"Absolute Maximum Ratings"* are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these *"Absolute Maximum"* limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\,V_{DC}$ and $V_{REF} = \pm 1\,V_{DC}$.

Note 6: $T_{MIN} = 0°C$ and $T_{MAX} = 70°C$ for "LCN" suffix parts.
$T_{MIN} = -40°C$ and $T_{MAX} = 85°C$ for "LCD" suffix parts.
$T_{MIN} = -55°C$ and $T_{MAX} = 125°C$ for "LD" suffix parts.

Note 7: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC1000 is "0.05% of FSR (MAX)." This guarantees that after performing a zero and full scale adjustment (See Sections 2.5 and 2.6), the plot of the 1024 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

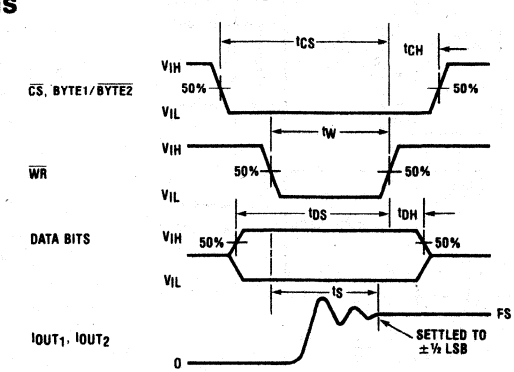
Note 8: This specification implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating, the feedthrough is typically 6 mV.

Note 10: Guaranteed by design but not tested.

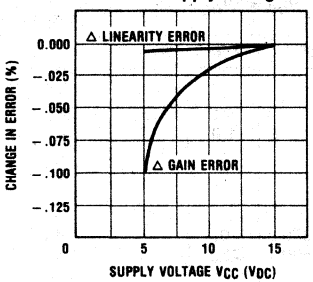
Note 11: A 200 nA leakage current with $R_{fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(200 \times 10^{-9} \times 20 \times 10^3) \times 100 \div 10$ which is 0.04% of FS.

Switching Waveforms

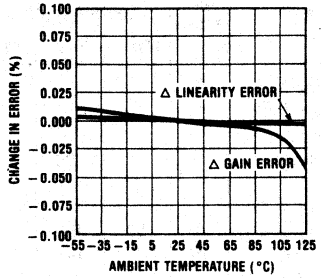


Typical Performance Characteristics

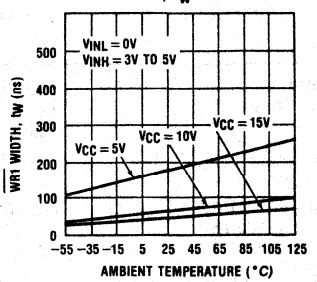
Errors vs. Supply Voltage



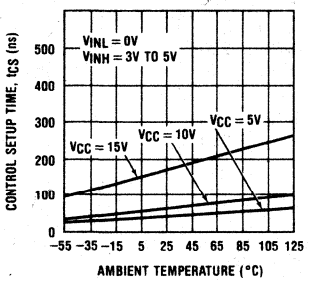
Errors vs. Temperature



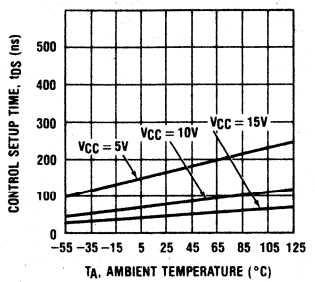
Write Width, t_W



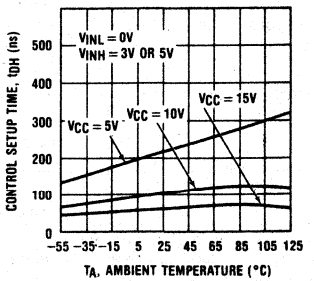
Control Setup Time, t_{CS}



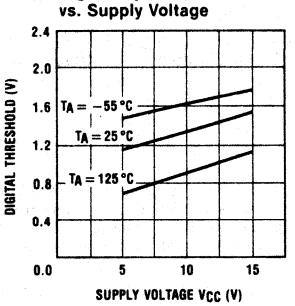
Data Setup Time, t_{DS}



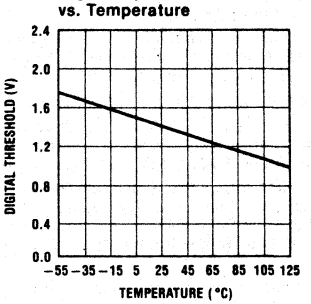
Data Hold Time, t_{DH}



Digital Input Threshold vs. Supply Voltage

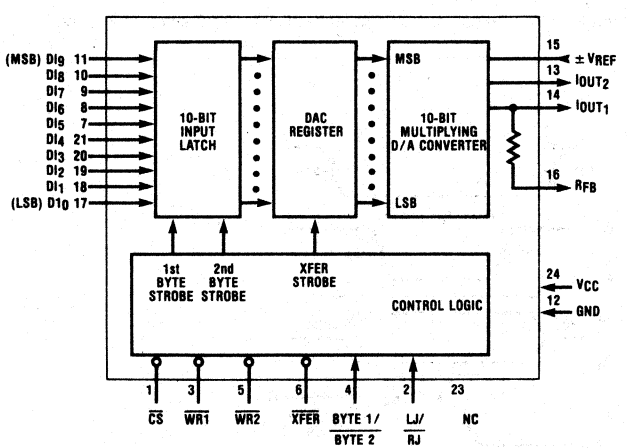


Digital Input Threshold vs. Temperature

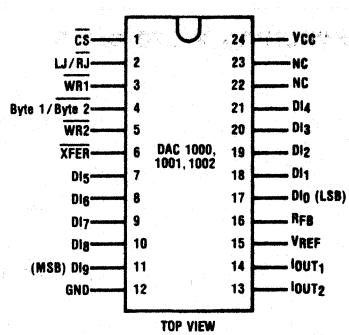


Block and Connection Diagrams

DAC1000/1001/1002 (24-Pin Parts)

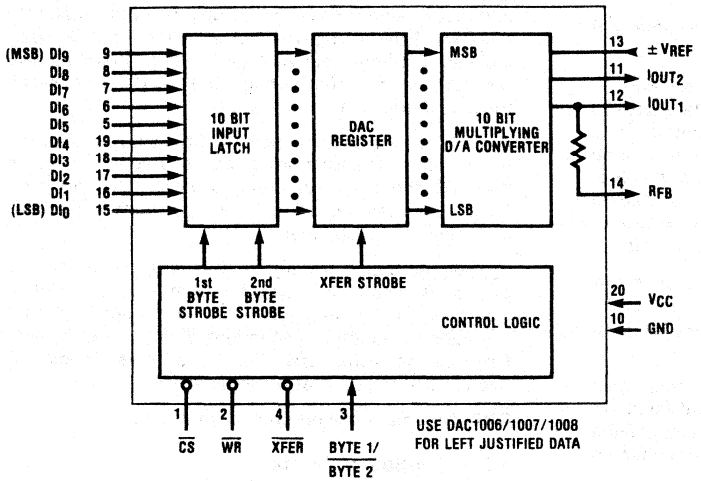


DAC1000/1001/1002 (24-Pin Parts)

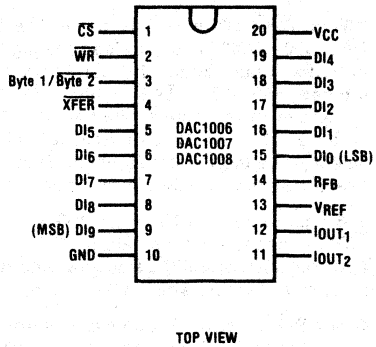


Block and Connection Diagrams (cont'd)

DAC1006/1007/1008 (20-Pin Parts)

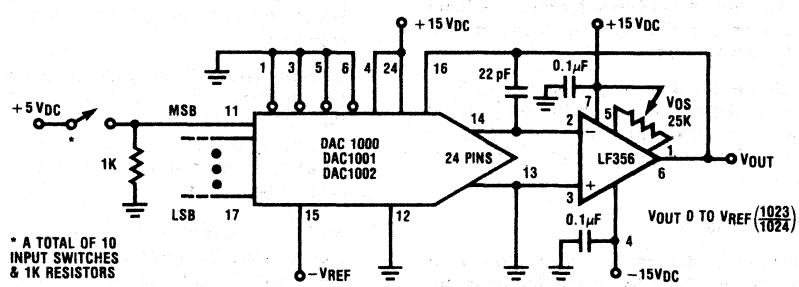


DAC1006/1007/1008 (20-Pin Parts)



TOP VIEW

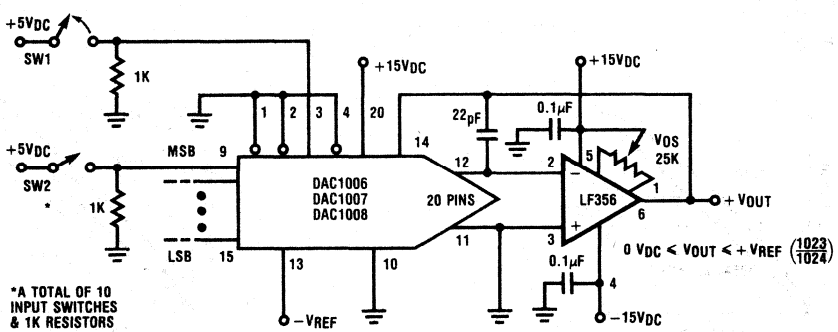
DAC1000/1001/1002 — Simple Hookup for a "Quick Look"



Notes:

1. For $V_{REF} = -10.240 V_{DC}$ the output voltage steps are approximately 10 mV each.
2. Operation is set up for flow through — no latching of digital input data.
3. Single point ground is strongly recommended.

DAC1006/1007/1008 Simple Hookup for a "Quick Look"



Notes:

1. For $V_{REF} = -10.240 V_{DC}$ the output voltage steps are approximately 10 mV each.
2. SW1 is a normally closed switch. While SW1 is closed, the DAC register is latched and new data can be loaded into the input latch via the 10 SW2 switches. When SW1 is momentarily opened the new data is transferred from the input latch to the DAC register and is latched when SW1 again closes.

1.0 Definition of Package Pinouts

1.1 Control Signals (All control signals are level actuated.)

$\overline{CS}$: Chip Select — active low, it will enable $\overline{WR}$ (DAC1003-1008) or WR_1 (DAC1000-1002).

$\overline{WR}$ or $\overline{WR_1}$: Write — The active low $\overline{WR}$ (or $\overline{WR_1}$ — DAC1000-1002) is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR}$ (or $\overline{WR_1}$) is high. The 10-bit input latch is split into two latches; one holds 8 bits and the other holds 2 bits. The Byte1/$\overline{Byte2}$ control pin is used to select both input latches when Byte1/$\overline{Byte2}$ = 1 or to overwrite the 2-bit input latch when in the low state.

$\overline{WR_2}$: Extra Write (DAC1000-1002) — The active low $\overline{WR_2}$ is used to load the data from the input latch to the DAC register while $\overline{XFER}$ is low. The data in the DAC register is latched when WR_2 is high.

Byte1/$\overline{Byte2}$: Byte Sequence Control — When this control is high, all ten locations of the input latch are enabled. When low, only two locations of the input latch are enabled and these two locations are overwritten on the second byte write.

$\overline{XFER}$: Transfer Control Signal, active low — This signal, in combination with others, is used to transfer the 10-bit data which is available in the input latch to the DAC register — see timing diagrams.

LJ/$\overline{RJ}$: Left Justify/Right Justify (DAC1000-1002) — When LJ/$\overline{RJ}$ is high the part is set up for left justified (fractional) data format. (DAC1006-1008 have this done internally.) When LJ/$\overline{RJ}$ is low, the part is set up for right justified (integer) data.

1.2 Other Pin Functions

DI_i (i = 0 to 9): Digital Inputs — DI_0 is the least significant bit (LSB) and DI_9 is the most significant bit (MSB).

I_{OUT1}: DAC Current Output 1 — I_{OUT1} is a maximum for a digital input code of all 1s and is zero for a digital input code of all 0s.

I_{OUT2}: DAC Current Output 2 — I_{OUT2} is a constant minus I_{OUT1}, or

$$I_{OUT1} + I_{OUT2} = \frac{1023}{1024} \frac{V_{REF}}{R}$$

where R ≅ 15kΩ.

R_{FB}: Feedback Resistor — This is provided on the IC chip for use as the shunt feedback resistor when an external op amp is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) because it matches the resistors used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input — This is the connection for the external precision voltage source which drives the R-2R ladder. V_{REF} can range from −10 to +10 volts. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage — This is the power supply pin for the part. V_{CC} can be from +5 to +15V_{DC}. Operation is optimum for +15V. The input threshold voltages are nearly independent of V_{CC}. (See Typical Performance Characteristics and Description in Section 3.0, T^2L compatible logic inputs.)

GND: Ground — the ground pin for the part.

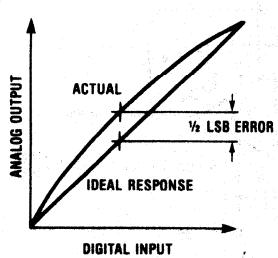
1.3 Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC1000 has 2^{10} or 1024 steps and therefore has 10-bit resolution.

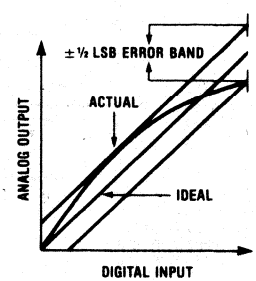
Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the "best straight line" test (b) used by other suppliers are illustrated below. The "best straight line" requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The "end point test" uses a standard zero and FS adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output (which is the worst case).



a. End Point Test After Zero and FS Adj.



b. Best Straight Line

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output (which is the worst case).

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within ±½ LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1000 series, full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = -10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 9.8mV = 9.9902V$. Full-scale error is adjustable to zero.

Monotonicity: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 10-bit DAC with 10-bit monotonicity will produce an increasing analog output when all 10 digital inputs are exercised. A 10-bit DAC with 9-bit monotonicity will be monotonic when only the most significant 9 bits are exercised. Similarly, 8-bit monotonicity is guaranteed when only the most significant 8 bits are exercised.

2.0 Double Buffering

These DACs are double-buffered, microprocessor compatible versions of the DAC1020 10-bit multiplying DAC. The addition of the buffers for the digital input data not only allows for storage of this data, but also provides a way to assemble the 10-bit input data word from two write cycles when using an 8-bit data bus. Thus, the next data update for the DAC output can be made with the complete new set of 10-bit data. Further, the double buffering allows many DACs in a system to store current data and also the next data. The updating of the new data for each DAC is also not time critical. When all DACs are updated, a common strobe signal can then be used to cause all DACs to switch to their new analog output levels.

3.0 T^2L Compatible Logic Inputs

To guarantee T^2L voltage compatibility of the logic inputs, a novel bipolar (NPN) regulator circuit is used. This makes the input logic thresholds equal to the forward drop of two diodes (and also matches the temperature variation) as occurs naturally in T^2L. The basic circuit is shown in Figure 1. A curve of digital input threshold as a function of power supply voltage is shown in the Typical Performance Characteristics section.

4.0 Application Hints

The DC stability of the V_{REF} source is the most important factor to maintain accuracy of the DAC over time and temperature changes. A good single point ground for the analog signals is next in importance.

These MICRO-DAC™ converters are CMOS products and reasonable care should be exercised in handling them prior to final mounting on a PC board. The digital inputs are protected, but permanent damage may occur if the part is subjected to high electrostatic fields. Store unused parts in conductive foam or anti-static rails.

4.1 Power Supply Sequencing & Decoupling

Some IC amplifiers draw excessive current from the Analog inputs to V− when the supplies are first turned on. To prevent damage to the DAC — an external Schottky diode connected from I_{OUT1} or I_{OUT2} to ground may be required to prevent destructive currents in I_{OUT1} or I_{OUT2}. If an LM741 or LF356 is used — these diodes are not required.

The standard power supply decoupling capacitors which are used for the op amp are adequate for the DAC.

4.2 Op Amp Bias Current & Input Leads

The op amp bias current (I_B) CAN CAUSE DC ERRORS. BI-FET™ op amps have very low bias current, and there-

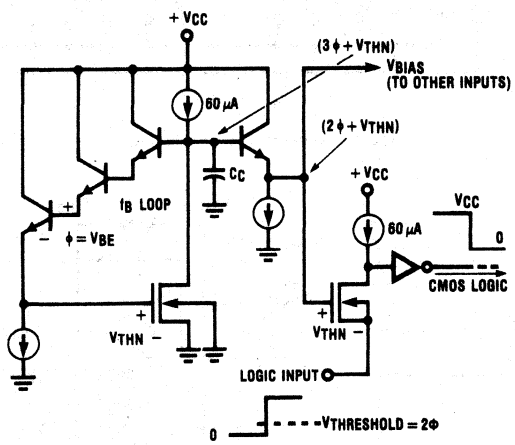


Figure 1. Basic Logic Threshold Loop

fore the error introduced is negligible. BI-FET™ op amps are strongly recommended for these DACs.

The distance from the I_{OUT1} pin of the DAC to the inverting input of the op amp should be kept as short as possible to prevent inadvertent noise pickup.

5.0 Analog Applications

The analog section of these DACs uses an R-2R ladder which can be operated both in the current switching mode and in the voltage switching mode.

The major product changes (compared with the DAC1020) have been made in the digital functioning of the DAC. The analog functioning is reviewed here for completeness. For additional analog applications, such as multipliers, attenuators, digitally controlled amplifiers and low frequency sine wave oscillators, refer to the DAC1020 data sheet. Some basic circuit ideas are presented in this section in addition to complete applications circuits.

5.1 Operation in Current Switching Mode

The analog circuitry, Figure 2, consists of a silicon-chromium (Si-Cr) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there is no parasitic diode connected to the V_{REF} pin as would exist if diffused resistors were used. The reference voltage input (V_{REF}) can therefore range from −10V to +10V.

The digital input code to the DAC simply controls the position of the SPDT current switches, SW0 to SW9. A logical 1 digital input causes the current switch to steer the available ladder current to the I_{OUT1} output pin. These MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

5.1.1 Providing a Unipolar Output Voltage with the DAC in the Current Switching Mode

A voltage output is provided by making use of an external op amp as a current-to-voltage converter. The idea is to use the internal feedback resistor, R_{FB}, from the output of the op amp to the inverting (−) input. Now, when current is entered at this inverting input, the feedback action of the op amp keeps that input at ground potential. This causes the applied input current to be diverted to the feedback resistor. The output voltage of the op amp is forced to a voltage given by:

$$V_{OUT} = -(I_{OUT1} \times R_{FB})$$

Notice that the sign of the output voltage depends on the direction of current flow through the feedback resistor.

In current switching mode applications, both current output pins (I_{OUT1} and I_{OUT2}) should be operated at $0\,V_{DC}$. This is accomplished as shown in Figure 3. The capacitor, C_C, is used to compensate for the output capacitance of the DAC and the input capacitance of the op amp. The required feedback resistor, R_{FB}, is available on the chip (one end is internally tied to I_{OUT1}) and must be used since an external resistor will not provide the needed matching and temperature tracking. This circuit can therefore be simplified as shown in

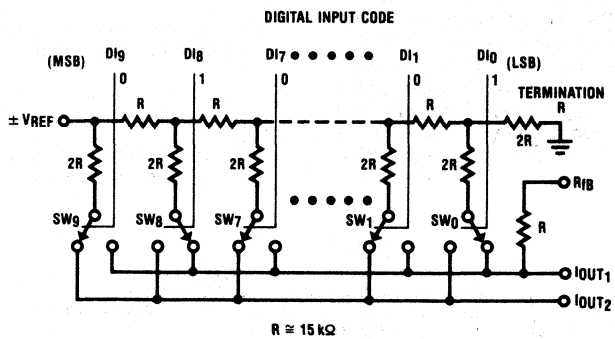


Figure 2. Current Mode Switching

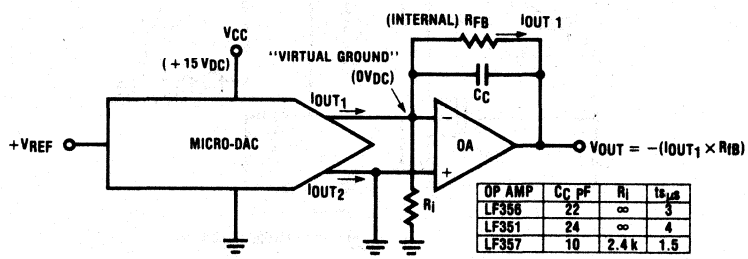


Figure 3. Converting I_{OUT} to V_{OUT}

Figure 4, where the sign of the reference voltage has been changed to provide a positive output voltage. Note that the output current, I_{OUT1}, now flows through the R_{FB} pin.

5.1.2 Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

The addition of a second op amp to the circuit of Figure 4 can be used to generate a bipolar output voltage from a fixed reference voltage (Figure 5). This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize the full four-quadrant multiplication.

The applied digital word is offset binary which includes a code to output zero volts without the need of a large valued resistor common to existing bipolar multiplying DAC circuits. Offset binary code can be derived from 2's complement data (most common for signed processor arithmetic) by inverting the state of the MSB in either software or hardware. After doing this the output then responds in accordance to the following expression:

$$V_O = V_{REF} \times \frac{D}{512}$$

where V_{REF} can be positive or negative and D is the signed decimal equivalent of the 2's complement processor data. ($-512 \leq D \leq +511$ or $1000000000 \leq D \leq 0111111111$). If the applied digital input is interpreted as the decimal equivalent of a true binary word, V_{OUT} can be found by:

$$V_O = V_{REF}\left(\frac{D-512}{512}\right) \qquad 0 \leq D \leq 1023$$

With this configuration, only the offset voltage of amplifier 1 need be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp has no effect on linearity. It presents a constant output voltage error and should be nulled only if absolute accuracy is needed. Another advantage of this configuration is that the values of the external resistors required do not have to match the value of the internal DAC resistors; they need only to match and temperature track each other.

A thin film 4 resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. Two of the four available 10 kΩ resistor can be paralleled to form R in Figure 5 and the other two can be used separately as the resistors labeled 2R.

Operation is summarized in the table below:

2's Comp. (Decimal)	2's Comp. (Binary)	Applied Digital Input	Applied True Binary (Decimal)	V_{OUT} $+V_{REF}$	V_{OUT} $-V_{REF}$
+511	0111111111	1111111111	1023	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
+256	0100000000	1100000000	768	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
0	0000000000	1000000000	512	0	0
−1	1111111111	0111111111	511	−1 LSB	+1 LSB
−256	1100000000	0100000000	256	$-V_{REF}/2$	$+\lvert V_{REF}\rvert/2$
−512	1000000000	0000000000	0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

with: 1 LSB $= \frac{|V_{REF}|}{512}$

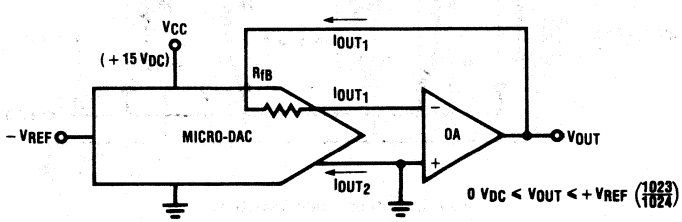


Figure 4. Providing a Unipolar Output Voltage

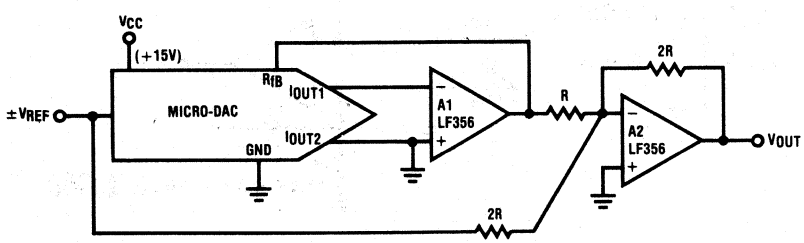


Figure 5. Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

5.2 Analog Operation in the Voltage Switching Mode

Some useful application circuits result if the R-2R ladder is operated in the voltage switching mode. There are two very important things to remember when using the DAC in the voltage mode. The reference voltage (+V) must always be positive since there are parasitic diodes to ground on the I_{OUT1} pin which would turn on if the reference voltage went negative. To maintain a degradation of linearity less than ±0.005%, keep $+V \leq 3V_{DC}$ and V_{CC} at least 10V more positive than +V. Figures 6 and 7 show these errors for the voltage switching mode. This operation appears unusual, since a reference voltage (+V) is applied to the I_{OUT1} pin and the voltage output is the V_{REF} pin. This basic idea is shown in Figure 8.

This V_{OUT} range can be scaled by use of a non-inverting gain stage as shown in Figure 9.

Notice that this is unipolar operation since all voltages are positive. A bipolar output voltage can be obtained by using a single op amp as shown in Figure 10. For a digital input code of all zeros, the output voltage from the V_{REF} pin is zero volts. The external op amp now has a single input of +V and is operating with a gain of −1 to this input. The output of the op amp therefore will be at −V for a digital input of all zeros. As the digital code increases, the output voltage at the V_{REF} pin increases.

Notice that the gain of the op amp to voltages which are applied to the (+) input is +2 and the gain to voltages which are applied to the input resistor, R, is −1. The output voltage of the op amp depends on both of these inputs and is given by:

$$V_{OUT} = (+V)(-1) + V_{REF}(+2)$$

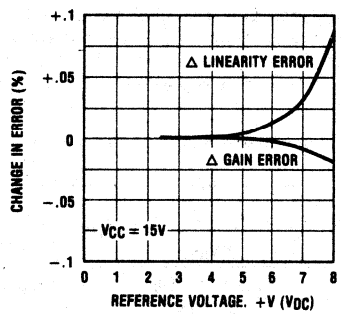


Figure 6.

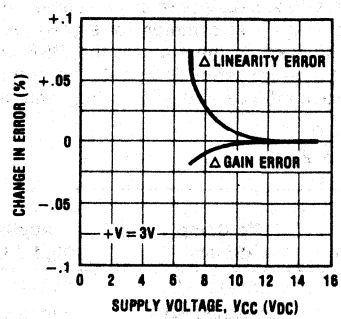


Figure 7.

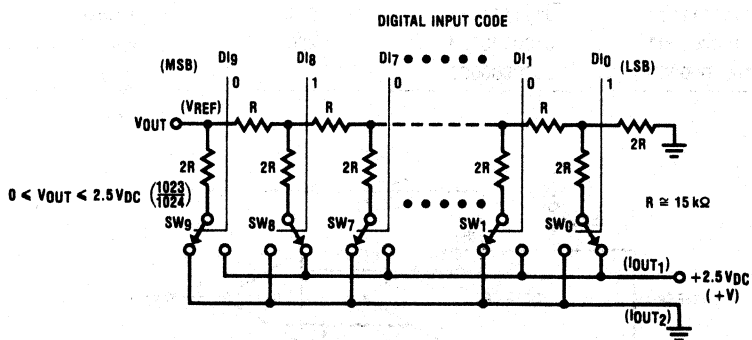


Figure 8. Voltage Mode Switching

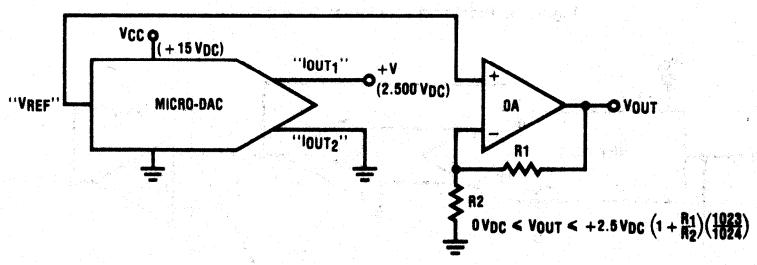


Figure 9. Amplifying the Voltage Mode Output (Single Supply Operation)

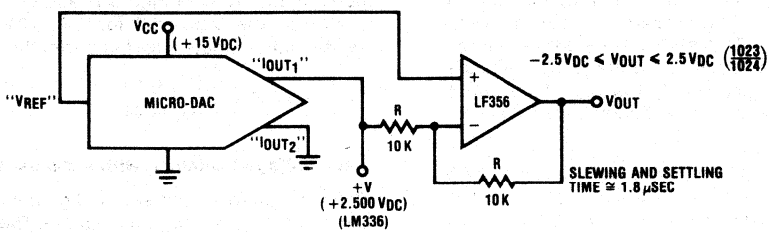


Figure 10. Providing a Bipolar Output Voltage with a Single Op Amp

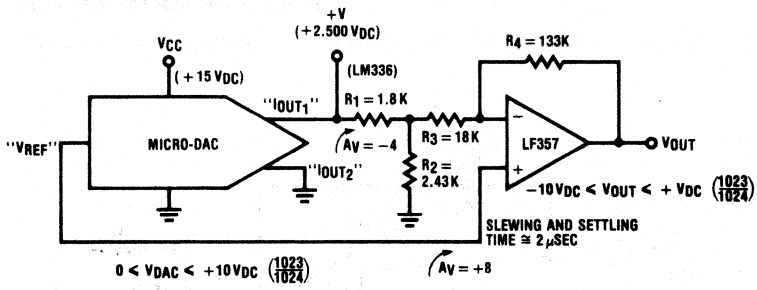


Figure 11. Increasing the Output Voltage Swing

The output voltage swing can be expanded by adding 2 resistors to Figure 10 as shown in Figure 11. These added resistors are used to attenuate the +V voltage. The overall gain, $A_V(-)$, from the +V terminal to the output of the op amp determines the most negative output voltage, −4(+V) (when the V_{REF} voltage at the + input of the op amp is zero) with the component values shown. The complete dynamic range of V_{OUT} is provided by the gain from the (+) input of the op amp. As the voltage at the V_{REF} pin ranges from 0V to +V(1023/1024) the output of the op amp will range from $-10\,V_{DC}$ to +10V(1023/1024) when using a +V voltage of $+2.500\,V_{DC}$. The $2.5\,V_{DC}$ reference voltage can be easily developed by using the LM336 zener which can be biased through the R_{FB} internal resistor, connected to V_{CC}.

5.3 Op Amp V_{OS} Adjust (Zero Adjust) for Current Switching Mode

Proper operation of the ladder requires that all of the 2R legs always go to exactly $0\,V_{DC}$ (ground). Therefore offset voltage, V_{OS}, of the external op amp cannot be tolerated as every millivolt of V_{OS} will introduce 0.01% of added linearity error. At first this seems unusually sensitive, until it becomes clear the 1mV is 0.01% of the 10V reference! High resolution converters of high accuracy require attention to every detail in an application to achieve the available performance which is inherent in the part. To prevent this source of error, the V_{OS} of the op amp has to be initially zeroed. This is the "zero adjust" of the DAC calibration sequence and should be done first.

If the V_{OS} is to be adjusted there are a few points to consider. Note that no "dc balancing" resistance should be used in the grounded positive input lead of the op amp. This resistance and the input current of the op amp can also create errors. The low input biasing current of the BI-FET™ op amps makes them ideal for use in DAC current to voltage applications. The V_{OS} of the op amp should be adjusted with a digital input of all zeros to force $I_{OUT} = 0$mA. A 1KΩ resistor can be temporarily connected from the inverting input to ground to provide a dc gain of approximately 15 to the V_{OS} of the op amp and make the zeroing easier to sense.

5.4 Full-Scale Adjust

The full-scale adjust procedure depends on the application circuit and whether the DAC is operated in the current switching mode or in the voltage switching mode. Techniques are given below for all of the possible application circuits.

5.4.1 Current Switching with Unipolar Output Voltage

After doing a "zero adjust," set all of the digital input levels HIGH and adjust the magnitude of V_{REF} for

$$V_{OUT} = -(\text{ideal } V_{REF})\,\frac{1023}{1024}$$

This completes the DAC calibration.

5.4.2 Current Switching with Bipolar Output Voltage

The circuit of Figure 12 shows the 3 adjustments needed. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) and then trim "zero adj." for zero volts at the inverting input (pin 2) of 0A1. Next, with a code of all zeros still applied, adjust "−FS adj.", the reference voltage, for $V_{OUT} = \pm|(\text{ideal } V_{REF})|$. The sign of the output voltage will be opposite that of the applied reference.

Finally, set all of the digital inputs HIGH and adjust "+FS adj." for $V_{OUT} = V_{REF}$ (511/512). The sign of the output at this time will be the same as that of the reference voltage. The addition of the 200Ω resistor in series with the V_{REF} pin of the DAC is to force the circuit gain error from the DAC to be negative. This insures that adding resistance to R_{fb}, with the 500Ω pot, will always compensate the gain error of the DAC.

5.4.3 Voltage Switching with a Unipolar Output Voltage

Refer to the circuit of Figure 13 and set all digital inputs LOW. Trim the "zero adj." for $V_{OUT} = 0V_{DC} \pm 1mV$. Then set all digital inputs HIGH and trim the "FS Adj." for:

$$V_{OUT} = (+V)\left(1 + \frac{R_1}{R_2}\right)\frac{1023}{1024}$$

5.4.4 Voltage Switching with a Bipolar Output Voltage

Refer to Figure 14 and set all digital inputs LOW. Trim the "− FS Adj." for $V_{OUT} = -2.5V_{DC}$. Then set all digital inputs HIGH and trim the "+ FS Adj." for $V_{OUT} = +2.5$ (511/512) V_{DC}. Test the zero by setting the MS digital input HIGH and all the rest LOW. Adjust V_{OS} of amp #3, if necessary, and recheck the full-scale values.

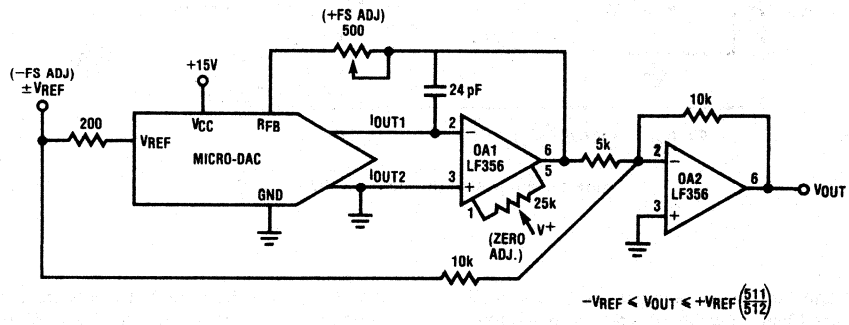


Figure 12. Full Scale Adjust — Current Switching with Bipolar Output Voltage

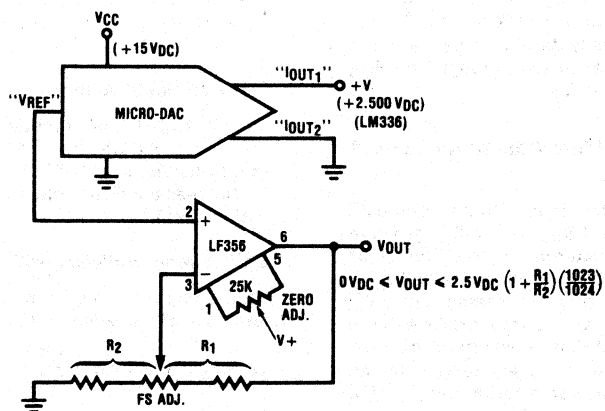


Figure 13. Full Scale Adjust — Unipolar Output Voltage

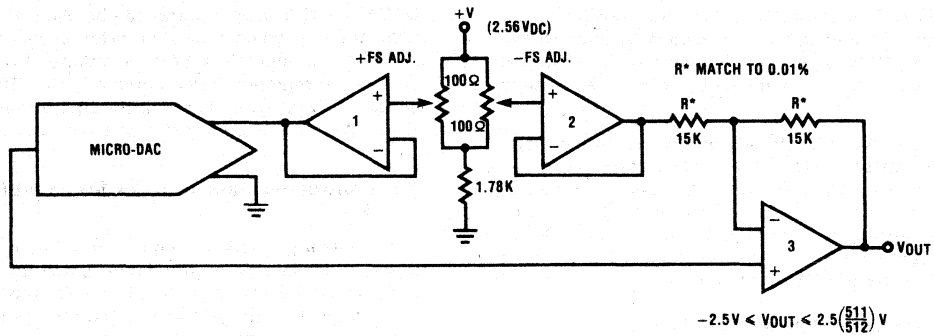


Figure 14. Voltage Switching with a Bipolar Output Voltage

6.0 Digital Control Description

The DAC1000 series of products can be used in a wide variety of operating modes. Most of the options are shown in Table I. Also shown in this table are the section numbers of this data sheet where each of the operating modes is discussed. For example, if your main interest is interfacing to a μP with an 8-bit data bus you will be directed to Section 6.1.0.

The first consideration is "will the DAC be interfaced to a μP with an 8-bit or a 16-bit data bus or used in the stand-alone mode?" For the 8-bit data bus, a second selection is made on how the 2nd digital data buffer (the DAC Latch) is updated by a transfer from the 1st digital data buffer (the Input Latch). Three options are provided: 1) an automatic transfer when the 2nd data byte is written to the DAC, 2) a transfer which is under the control of the μP and can include more than one DAC in a simultaneous transfer, or 3) a transfer which is under the control of external logic. Further, the data format can be either left justified or right justified.

When interfacing to a μP with a 16-bit data bus only two selections are available: 1) operating the DAC with a single digital data buffer (the transfer of one DAC does not have to be synchronized with any other DACs in the system), or 2) operating with a double digital data buffer for simultaneous transfer, or updating, of more than one DAC.

For operating without a μP in the stand alone mode, three options are provided: 1) using only a single digital data buffer, 2) using both digital data buffers — "double buffered," or 3) allowing the input digital data to "flow through" to provide the analog output without the use of any data latches.

To reduce the required reading, only the applicable sections of 6.1 through 6.4 need be considered.

6.1 Interfacing to an 8-Bit Data Bus

Transferring 10 bits of data over an 8-bit bus requires two write cycles and provides four possible combinations which depend upon two basic data format and protocol decisions:

1. Is the data to be left justified (considered as fractional binary data with the binary point to the left) or right justified (considered as binary weighted data with the binary point to the right)?
2. Which byte will be transferred first, the most significant byte (MS byte) or the least significant byte (LS byte)?

Table 1.

Operating Mode →	Automatic Transfer			μP Control Transfer			External Transfer		
	Section	Figure No. (24-Pin)	(20-Pin)	Section	Figure No. (24-Pin)	(20-Pin)	Section	Figure No. (24-Pin)	(20-Pin)
8-Bit Data Bus (6.1.0)									
Right Justified (6.1.1)	6.2.1	16		6.2.2	16		6.2.3	16	
Left Justified (6.1.2)	6.2.1	17	18	6.2.2	17	18	6.2.3	17	18
16-Bit Data Bus (6.3.0)	Single Buffered			Double Buffered			Flow Through		
	6.3.1	19	20	6.3.2	19	20	Not Applicable		
Stand Alone (6.4.0)	Single Buffered			Double Buffered			Flow Through		
	6.4.1	19	20	6.4.2	19	20	6.4.3	19	NA

These data possibilities are shown in Figure 15. Note that the justification of data depends on how the 10-bit data word is located within the 16-bit data source (CPU) register. In either case, there is a surplus of 6 bits and these are shown as "don't care" terms ("X") in this figure.

All of these DACs load 10 bits on the 1st write cycle. A particular set of 2 bits is then overwritten on the 2nd write cycle, depending on the justification of the data. This requires the 1st write cycle to contain the LS or L0 Byte data group for all right justified data options. For all left justified data options, the 1st write cycle must contain the MS or Hi Byte data group.

6.1.1 Providing for Optional Data Format

The DAC1000/1/2 (24-pin parts) can be used for either data formatting by tying the LJ/RJ pin either high or low, respectively. A simplified logic diagram which shows the external connections to the data bus and the internal functions of both of the data buffer registers (Input Latch and DAC Register) is shown in Figure 16 for the right justified data operation. Figure 17 is for left justified data.

6.1.2 For Left Justified Data

For applications which require left justified data, DAC1006-1008 (20-pin parts) can be used. A simplified logic diagram which shows the external connections to the data bus and the internal functions of both of the data buffer registers (Input Latch and DAC Register) is shown in Figure 18. These parts require the MS or Hi Byte data group to be transferred on the 1st write cycle.

6.2 Controlling Data Transfer for an 8-Bit Data Bus

Three operating modes are possible for controlling the transfer of data from the Input Latch to the DAC Register, where it will update the analog output voltage. The simplest is the automatic transfer mode, which causes the data transfer to occur at the time of the 2nd write cycle. This is recommended when the exact timing of the changes of the DAC analog output are not critical. This typically happens where each DAC is operating individually in a system and the analog updating of one DAC is not required to be synchronized to any other DAC. For synchronized DAC updating, two options are provided: μP control via a common XFER strobe or external update timing control via an external strobe. The details of these options are now shown.

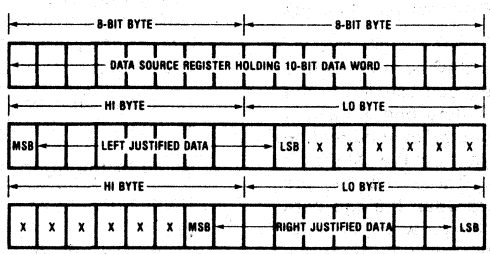


Figure 15. Fitting a 10-Bit Data Word into 16 Available Bit Locations

DAC1000/1001/1002 (24-Pin Parts)

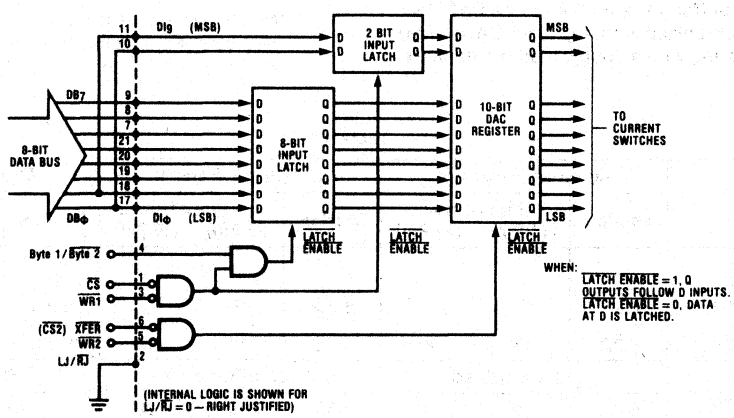


Figure 16. Input Connections and Controls for DAC1000-1002 Right Justified Data Option

DAC1000/1001/1002 (24-Pin Parts)

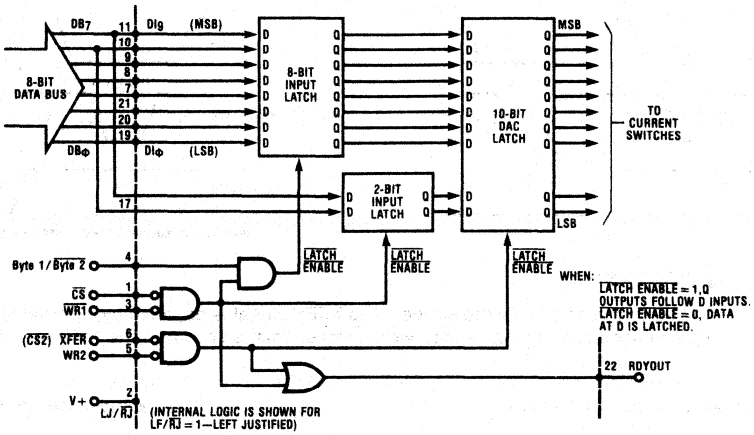


Figure 17. Input Connections and Controls for DAC1000-1002 Left Justified Data Option

DAC1006/1007/1008 (20-Pin Parts for Left Justified Data)

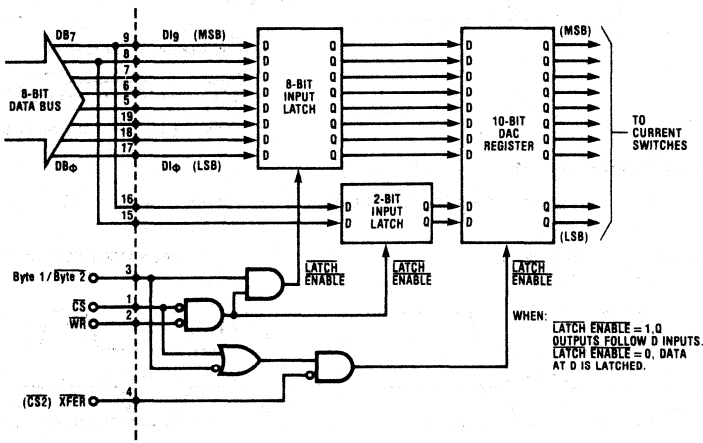
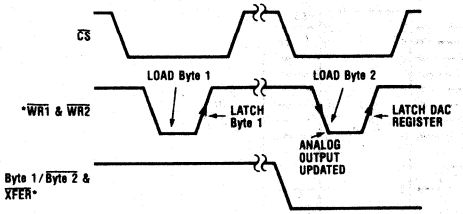


Figure 18. Input Connections and Controls for DAC1006/1007/1008 Left Justified Data

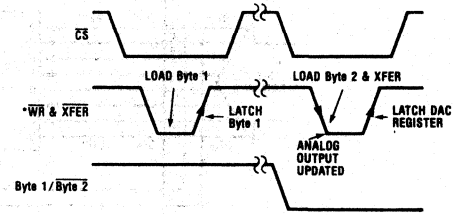
6.2.1 Automatic Transfer

This makes use of a double byte (double precision) write. The first byte (8 bits) is strobed into the input latch and the second byte causes a simultaneous strobe of the two remaining bits into the input latch and also the transfer of the complete 10-bit word from the input latch to the DAC register. This is shown in the following timing diagrams; the point in time where the analog output is updated is also indicated on these diagrams.

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)

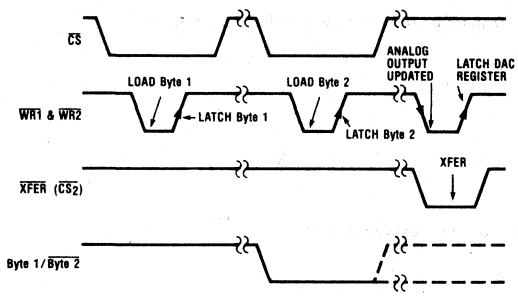


*SIGNIFIES CONTROL INPUTS WHICH ARE DRIVEN IN PARALLEL

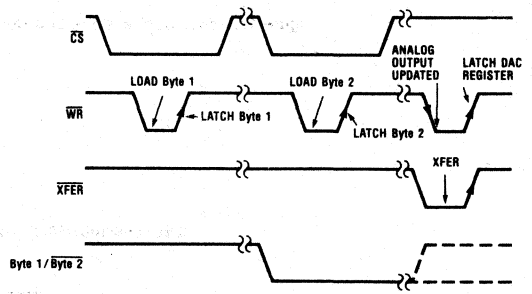
6.2.2 Transfer Using μP Write Strobe

The input latch is loaded with the first two write strobes. The $\overline{XFER}$ signal is provided by external logic, as shown below, to cause the transfer to be accomplished on a third write strobe. This is shown in the following diagrams:

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)



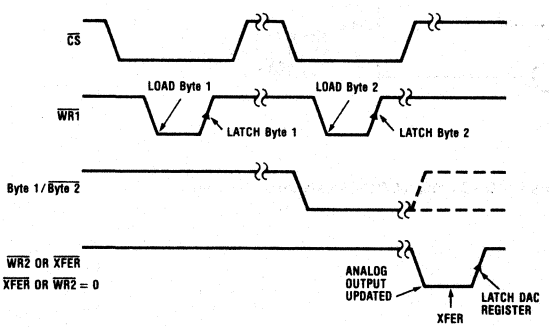
WHERE THE XFER CONTROL CAN BE GENERATED BY USING A SECOND CHIP SELECT AS:

AND THE BYTE CONTROL CAN BE DERIVED FROM THE ADDRESS BUS SIGNALS.

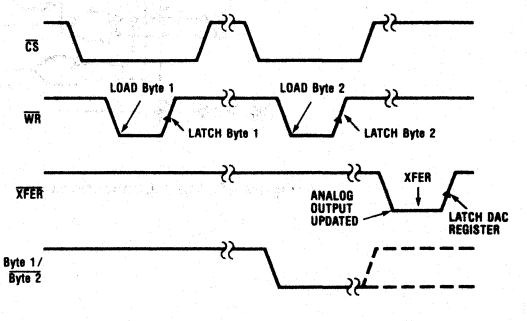
6.2.3 Transfer Using an External Strobe

This is similar to the previous operation except the $\overline{XFER}$ signal is not provided by the μP. The timing diagram for this is:

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)



6.3 Interfacing to a 16-Bit Data Bus

The interface to a 16-bit data bus is easily handled by connecting to 10 of the available bus lines. This allows a wiring selected right justified or left justified data format. This is shown in the connection diagrams of Figures 19 and 20, where the use of DB6 to DB15 gives left justified data operation. Note that any part number can be used and the Byte1/Byte2 control should be wired Hi.

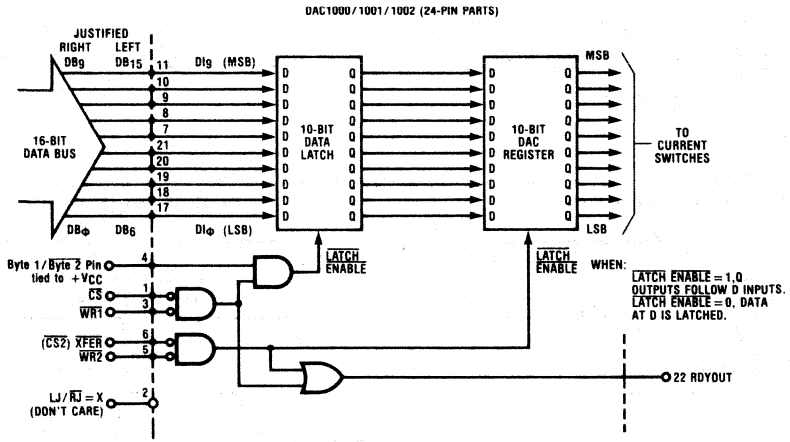


Figure 19. Input Connections and Logic for DAC1000-1002 with 16-Bit Data Bus

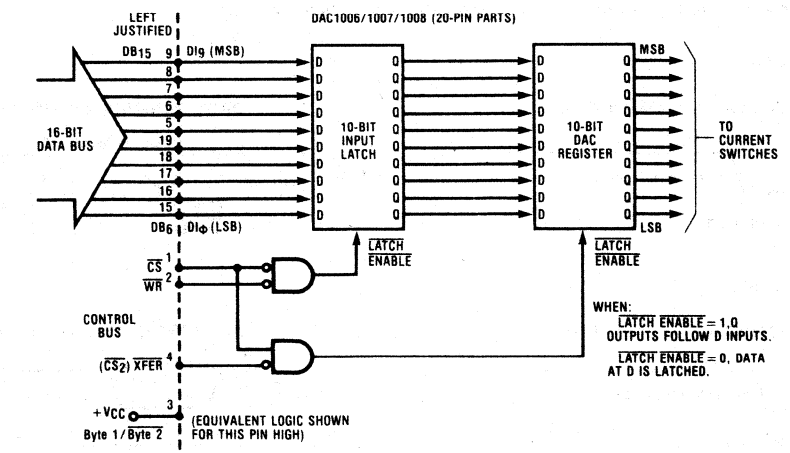
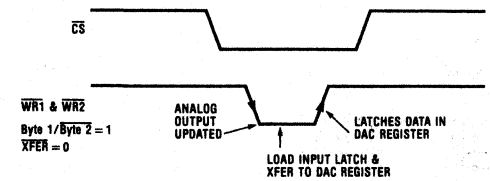


Figure 20. Input Connections and Logic for DAC1006/1007/1008 with 16-Bit Data Bus

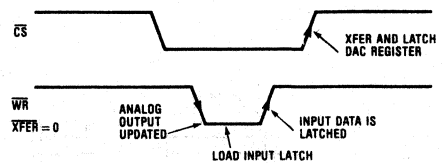
Three operating modes are possible: flow through, single buffered, or double buffered. The timing diagrams for these are shown below:

6.3.1 Single Buffered

DAC1000/1001/1002 (24-Pin Parts)

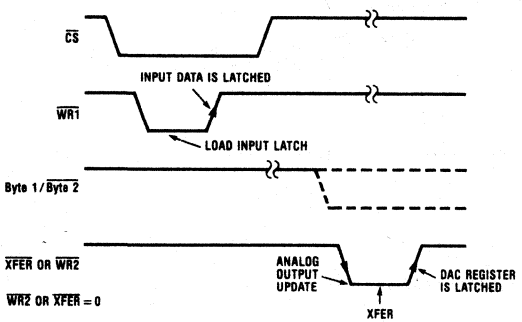


DAC1006/1007/1008 (20-Pin Parts)

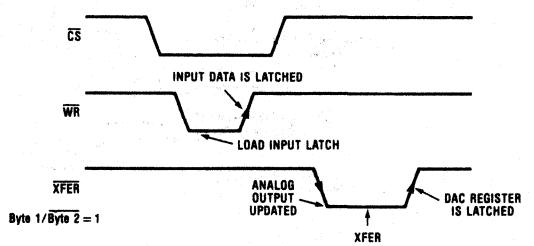


6.3.2 Double Buffered

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)

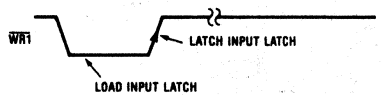


6.4 Stand Alone Operation

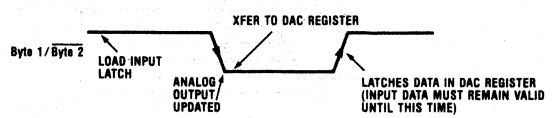
For applications for a DAC which are not under μP control (stand alone) there are two basic operating modes, single buffered and double buffered. The timing diagrams for these are shown below:

6.4.1 Single Buffered

DAC1000/1001/1002 (24-Pin Parts)

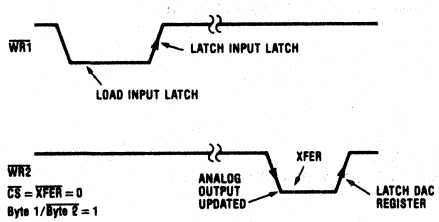


DAC1006/1007/1008 (20-Pin Parts)*

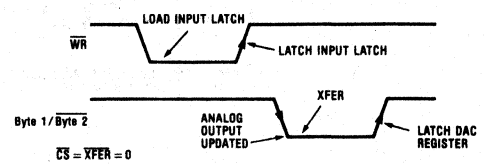


6.4.2 Double Buffered

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)*



*For a connection diagram of this operating mode use Figure 18 for the Logic and Figure 20 for the Data Input connections.

6.4.3 Flow Through

This operating mode causes the 10-bit input word to directly create the DAC output without any latching involved.

DAC1000/1001/1002 (24-Pin Parts)

$\overline{WR1} = \overline{WR2} = \overline{CS} = \overline{XFER} = 0$
Byte 1/$\overline{Byte\ 2} = 1$

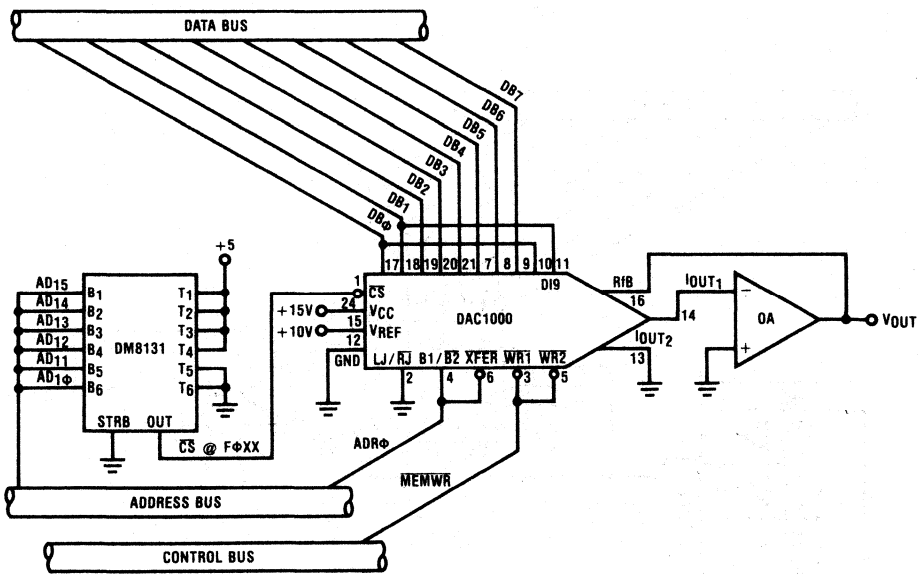
7.0 Microprocessor Interface

The logic functions of the DAC1000 family have been oriented towards an ease of interface with all popular μPs. The following sections discuss in detail a few useful interface schemes.

7.1 DAC1000/1/2 to INS8080A Interface

Figure 21 illustrates the simplicity of interfacing the DAC1000 to an INS8080A based microprocessor system. The circuit will perform an automatic transfer of the 10 bits of output data from the CPU to the DAC register as outlined in Section 6.2.1, "Controlling Data Transfer for an 8-Bit Data Bus."

Since a double byte write is necessary to control the DAC with the INS8080A, a possible instruction to achieve this is a PUSH of a register pair onto a "stack" in memory. The 16-bit register pair word will contain the 10 bits of the eventual DAC input data in the proper



NOTE: DOUBLE BYTE STORES CAN BE USED. e.g. THE INSTRUCTION SHLD F00 1 STORES THE L REG INTO B1 AND THE H REG INTO B2 AND TRANSFERS THE RESULT TO THE DAC REGISTER. THE OPERAND OF THE SHLD INSTRUCTION MUST BE AN ODD ADDRESS FOR PROPER TRANSFER.

Figure 21. Interfacing the DAC1000 to the INS8080A CPU Group

sequence to conform to both the requirements of the DAC (with regard to right or left justified data) and the implementation of the PUSH instruction which will output the higher order byte of the register pair (i.e., register B of the BC pair) first. The DAC will actually appear as a two-byte "stack" in memory to the CPU. The auto-decrementing of the stack pointer during a PUSH allows using address bit 0 of the stack pointer as the Byte1/Byte2 and XFER strobes if bit 0 of the stack pointer address – 1, (SP – 1), is a "1" as presented to the DAC. Additional address decoding by the DM8131 will generate a unique DAC chip select (CS) and synchronize this CS to the two memory write strobes of the PUSH instruction.

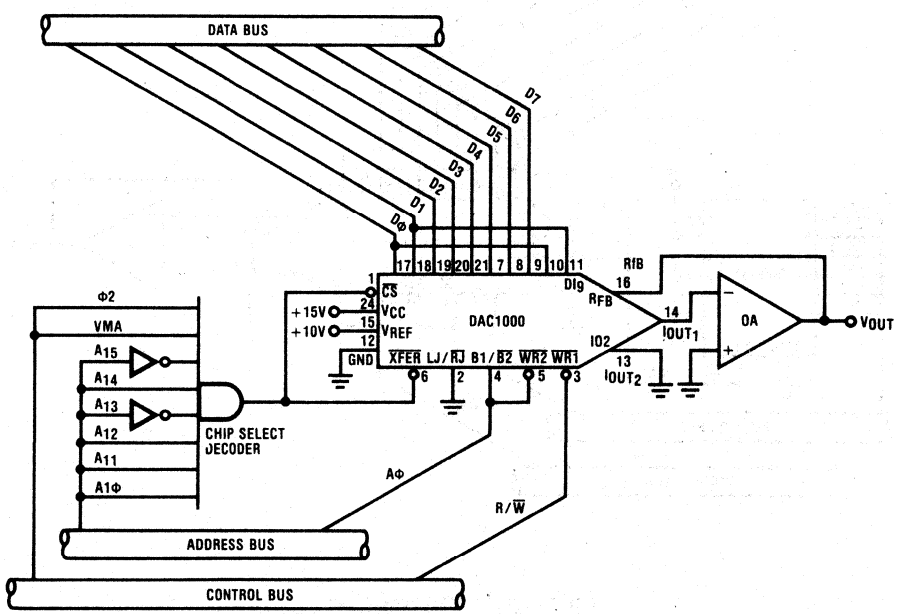
To reset the stack pointer so new data may be output to the same DAC, a POP instruction followed by instructions to insure that proper data is in the DAC data register pair before it is "PUSHED" to the DAC should be executed, as the POP instruction will arbitrarily alter the contents of a register pair.

Another double byte write instruction is Store H and L Direct (SHLD), where the HL register pair would temporarily contain the DAC data and the two sequential addresses for the DAC are specified by the instruction op code. The auto incrementing of the DAC address by the SHLD instruction permits the same simple scheme of using address bit 0 to generate the byte number and transfer strobes.

7.2 DAC1000 to M6800 Direct Interface

As in the INS8080A case, it is very simple to directly interface the DAC1000 to an M6800 system. Figure 22 illustrates such an interface assuming a right justified data structure. Except for address decoding, no external logic is necessary. The DAC1000 appears as two memory locations in the 6800 memory space. By using just an 8-input NAND gate and two inverters we have (arbitrarily) chosen these HEX addresses to be 5C00 and 5C01. Note, however, that any HEX address of the form 5CXX will also be decoded. This can easily be avoided by designing a more definitive address decoding scheme. Control lines 02 and VMA are included to insure stability of address and data lines before the DAC inputs are enabled.

In a normal operating mode the MPU would "store" two 8-bit bytes of right justified data into the DAC input latches: LOW byte first at location 5C01 and HIGH byte next at location 5C00. Upon storing the second byte, the 10-bit word is automatically transferred to the DAC register, therefore obtaining the desired analog output. This output will be maintained until the next two bytes of data are loaded into the DAC under MPU control.



NOTE: TWO SINGLE BYTE STORES (e.g. STA A, STA B) MUST BE USED SINCE A DOUBLE BYTE STORE (e.g. STX) WOULD TRANSFER AN INCOMPLETE WORD.

Figure 22. DAC1000 to MC6800 MPU Interface

7.3 DAC1000 to MC6820/1 PIA Interface

In Figure 23 the DAC1000 is interfaced to an M6800 system through an MC6820/1 Peripheral Interface Adapter (PIA). In this case the CS pin of the DAC is grounded since the PIA is already mapped in the 6800 system memory space and no decoding is necessary. Furthermore, by using both Ports A and B of the PIA the 10-bit data transfer, assumed right justified again in two 8-bit bytes, is greatly simplified. The HIGH byte is loaded into Output Register A (ORA) of the PIA, and the LOW byte is loaded into ORB. The 10-bit data transfer to the DAC and the corresponding analog output change occur simultaneously upon CB2 going LOW under program control. The 10-bit data word in the DAC register will be latched (and hence V_{OUT} will be fixed) when CB2 is brought back HIGH.

If both output ports of the PIA are not available, it is possible to interface the DAC1000 through a single port without much effort. However, additional logic at the CB2 (or CA2) lines or access to some of the 6800 system control lines will be required.

7.4 Noise Considerations

A typical digital/microprocessor bus environment is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz's and can cause noise spikes to appear at the DAC output. These noise spikes occur when the data bus changes state or when data is transferred between the latches of the device.

In low frequency or DC applications, low pass filtering can reduce these noise spikes. This is accomplished by over-compensating the DAC output amplifier by increasing the value of the feedback capacitor (C_C in Figure 3).

In applications requiring a fast transient response from the DAC and op amp, filtering may not be feasible. Adding a latch, DM74LS374, as shown in Figure 24 isolates the device from the data bus, thus eliminating noise spikes that occur every time the data bus changes state.

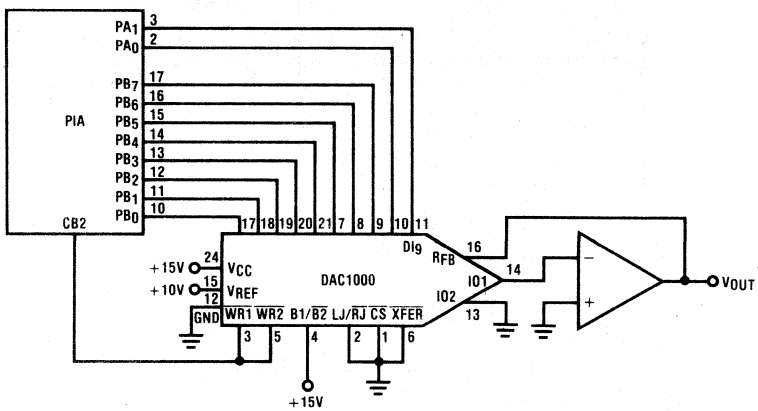


Figure 23. DAC1000 to MC6820/1 PIA Interface

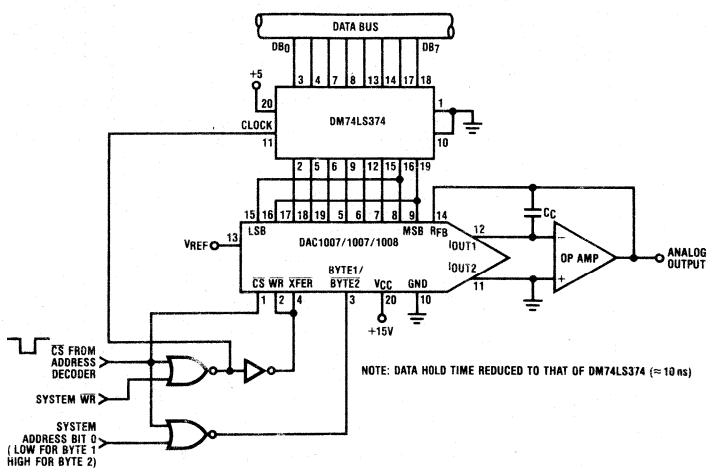


Figure 24. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling

Another method for eliminating noise spikes is to add a sample and hold after the DAC op amp. This also has the advantage of eliminating noise spikes when changing digital codes.

7.5 Digitally Controlled Amplifier/Attenuator

An unusual application of the DAC, Figure 25, applies the input voltage via the on-chip feedback resistor. The lower op amp automatically adjusts the $V_{REF\ IN}$ voltage such that I_{OUT1} is equal to the input current (V_{IN}/Rf_B). The magnitude of this $V_{REF\ IN}$ voltage depends on the digital word which is in the DAC register. I_{OUT2} then depends upon both the magnitude of V_{IN} and the digital word. The second op amp converts I_{OUT2} to a voltage, V_{OUT}, which is given by:

$$V_{OUT} = V_{IN}\left(\frac{1023 - N}{N}\right), \text{ where } 0 < N \leq 1023.$$

Note that N = 0 (or a digital code of all zeros) is not allowed or this will cause the output amplifier to saturate at either $\pm V_{MAX}$, depending on the sign of V_{IN}.

To provide a digitally controlled divider, the output op amp can be eliminated. Ground the I_{OUT2} pin of the DAC and V_{OUT} is now taken from the lower op amp (which also drives the V_{REF} input of the DAC). The expression for V_{OUT} is now given by

$$V_{OUT} = -\frac{V_{IN}}{M}$$ where M = Digital input (expressed as a fractional binary number). $0 < M < 1$.

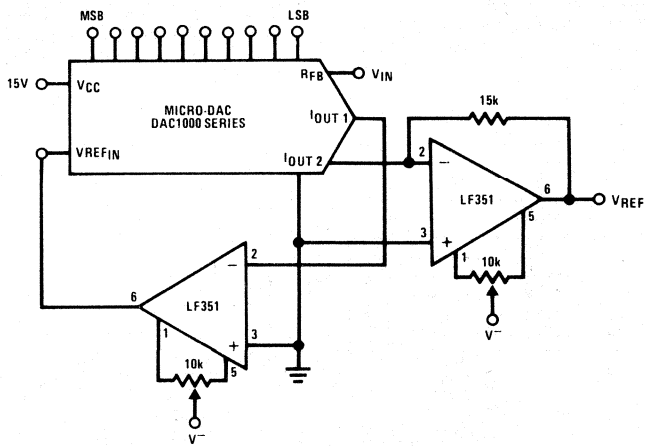


Figure 25. Digitally Controlled Amplifier/Attenuator

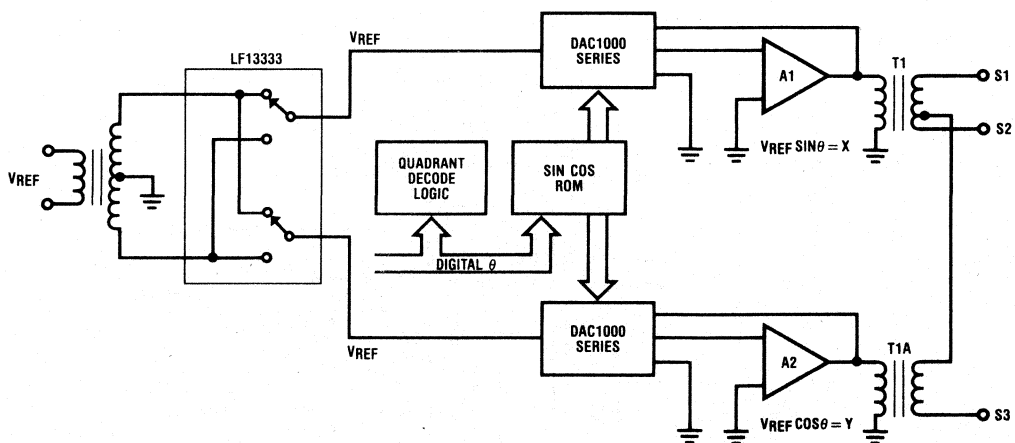


Figure 26. Digital to Synchro Converter

Ordering Information

1. **All Logic Features** — 24-pin package.

	Temperature Range		
Accuracy	**−40°C to +85°C**	**−55°C to +125°C**	**0°to +70°C**
0.05% (10-bit)	DAC1000LCD	DAC1000LD	DAC 1000LCN
0.10% (9-bit)	DAC1001LCD	DAC1001LD	DAC1001LCN
0.20% (8-bit)	DAC1002LCD	DAC1002LD	DAC1002LCN
Package Outline	D24C	D24C	N24A

2. **For Left Justified Data** — 20-pin package.

	Temperature Range		
Accuracy	**−40°C to +85°C**	**−55°C to +125°C**	**0°to +70°C**
0.05% (10-bit)	DAC1006LCD	DAC1006LD	DAC1006LCN
0.10% (9-bit)	DAC1007LCD	DAC1007LD	DAC1007LCN
0.20% (8-bit)	DAC1008LCD	DAC1008LD	DAC1008LCN
Package Outline	D20A	D20A	N20A

National Semiconductor

Digital-to-Analog Converters

DAC1020 10-Bit Binary Multiplying D/A Converter
DAC1220 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1020 and the DAC1220 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.0002%/°C linearity error temperature coefficient maximum). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference. All inputs are protected from damage due to static discharge by diode clamps to V^+ and ground.

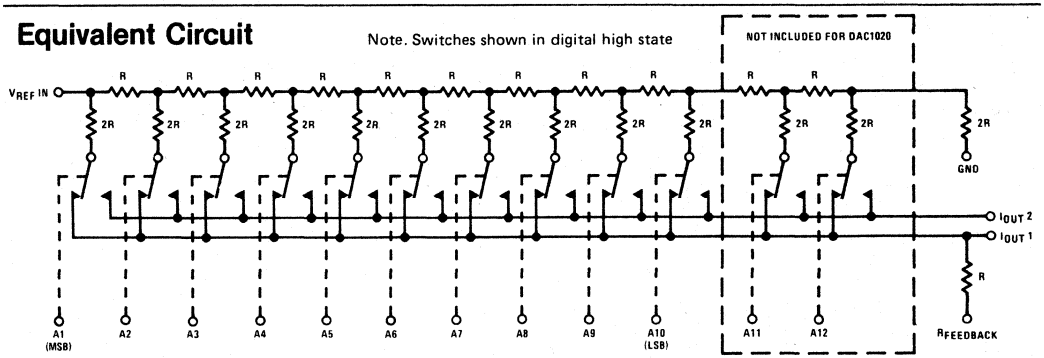
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity guarenteed over temperature (note 1 of electrical characteristics). The DAC1020, DAC1021 and DAC1022 are direct replacements for the 10-bit resolution AD7520 and AD7530 and equivalent to the AD7533 family. The DAC1220, DAC1221 and DAC1222 are direct replacements for the 12-bit resolution AD7521 and AD7531 family.

Features

- Linearity specified with zero and full-scale adjust only
- Non-linearity guaranteed over temperature
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @ 15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq +25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—500 ns typ
- Low feedthrough error—1/2 LSB @ 100 kHz typ

Equivalent Circuit

Note. Switches shown in digital high state



Ordering Information

10-BIT D/A CONVERTERS

TEMPERATURE RANGE		0°C to 70°C		-40°C to +85°C		-55°C to +125°C	
ACCURACY	0.05%	DAC1020LCN	AD7520LN AD7530LN	DAC1020LCD	AD7520LD AD7530LD	DAC1020LD	AD7520UD
	0.10%	DAC1021LCN	AD7520KN AD7530KN	DAC1021LCD	AD7520KD AD7530KD	DAC1021LD	AD7520TD
	0.20%	DAC1022LCN	AD7520JN AD7530JN	DAC1022LCD	AD7520JD AD7530JD	DAC1022LD	AD7520SD
PACKAGE OUTLINE		N16A		D16C		D16C	

12-BIT D/A CONVERTERS

TEMPERATURE RANGE		0°C to 70°C		-40°C to +85°C		-55°C to +125°C	
ACCURACY	0.05%	DAC1220LCN	AD7521LN AD7531LN	DAC1220LCD	AD7521LD AD7531LD	DAC1220LD	AD7521UD
	0.10%	DAC1221LCN	AD7521KN AD7531KN	DAC1221LCD	AD7521KD AD7531KD	DAC1221LD	AD7521TD
	0.20%	DAC1222LCN	AD7521JN AD7531JN	DAC1222LCD	AD7521JD AD7531JD	DAC1222LD	AD7521SD
PACKAGE OUTLINE		N18A		D18A		D18A	

Note. Devices may be ordered by either part number.

Absolute Maximum Ratings

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Temperature (T_A)			
DAC1020LD, DAC1021LD,	−55	+125	°C
DAC1022LD, DAC1220LD,	−55	+125	°C
DAC1221LD, DAC1222LD	−55	+125	°C
DAC1020LCD, DAC1021LCD,	−40	+85	°C
DAC1022LCD, DAC1220LCD,	−40	+85	°C
DAC1221LCD, DAC1222LCD	−40	+85	°C
DAC1020LCN, DAC1021LCN	0	+70	°C
DAC1022LCN, DAC1220LCN	0	+70	°C
DAC1221LCN, DAC1222LCN	0	+70	°C

Electrical Characteristics

(V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	DAC1020, DAC1021, DAC1022			DAC1220, DAC1221, DAC1222			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		10			12			Bits
Linearity Error	$T_{MIN} < T_A < T_{MAX}$, $-10V < V_{REF} < +10V$, (Note 1) End Point Adjustment Only (See Linearity Error in Definition of Terms)							
10-Bit Parts	DAC1020, DAC1220			0.05			0.05	% FSR
9-Bit Parts	DAC1021, DAC1221			0.10			0.10	% FSR
8-Bit Parts	DAC1022, DAC1222			0.20			0.20	% FSR
Linearity Error Tempco	$-10V \leq V_{REF} \leq +10V$, (Notes 1 and 2)			0.0002			0.0002	% FS/°C
Full-Scale Error	$-10V \leq V_{REF} \leq +10V$, (Notes 1 and 2)		0.3	1.0		0.3	1.0	% FS
Full-Scale Error Tempco	$T_{MIN} < T_A < T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current	$T_{MIN} \leq T_A \leq T_{MAX}$							
$I_{OUT\ 1}$	All Digital Inputs Low			200			200	nA
$I_{OUT\ 2}$	All Digital Inputs High			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \leq V^+ \leq 16V$, (Note 2), *(Figure 2)*		0.005	0.005		0.005	0.005	% FS/V
V_{REF} Input Resistance		10	15	20	10	15	20	kΩ
Full-Scale Current Settling Time	R_L = 100Ω from 0 to 99.95% FS							
	All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low, V_{REF} = 20 Vp-p @ 100 kHz			10			10	mVp-p
	D Package (Note 4)		6	9		6	9	mVp-p
	N Package		2	5		2	5	mVp-p
Output Capacitance								
$I_{OUT\ 1}$	All Digital Inputs Low		40			40		pF
	All Digital Inputs High		200			200		pF
$I_{OUT\ 2}$	All Digital Inputs Low		200			200		pF
	All Digital Inputs High		40			40		pF
Digital Input	*(Figure 1)*							
Low Threshold	$T_{MIN} < T_A < T_{MAX}$			0.8			0.8	V
High Threshold	$T_{MIN} < T_A < T_{MAX}$	2.4			2.4			V

Electrical Characteristics (Continued)

(V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	DAC1020, DAC1021 DAC1022			DAC1220, DAC1221 DAC1222			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Digital Input Current	$T_{MIN} \leq T_A \leq T_{MAX}$							
	Digital Input High		1	100		1	100	μA
	Digital Input Low		−50	−200		−50	−200	μA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range	*(Figures 1 and 2)*	5		15	5		15	V

Note 1: V_{REF} = ±10V and V_{REF} = ±1V. A linearity error temperature coefficient of 0.0002% FS for a 45°C rise only guarantees 0.009% maximum change in linearity error. For instance, if the linearity error at 25°C is 0.045% FS it could increase to 0.054% at 70°C and the DAC will be no longer a 10-bit part. Note, however, that the linearity error is specified over the device full temperature range which is a more stringent specification since *it includes* the linearity error temperature coefficient.

Note 2: Using internal feedback resistor as shown in *Figure 3*.

Note 3: Both $I_{OUT\ 1}$ and $I_{OUT\ 2}$ must go to ground or the virtual ground of an operational amplifier. If V_{REF} = 10V, every millivolt offset between $I_{OUT\ 1}$ or $I_{OUT\ 2}$, 0.005% linearity error will be introduced.

Note 4: To achieve this low feedthrough in the D package, the user must ground the metal lid.

Typical Performance Characteristics

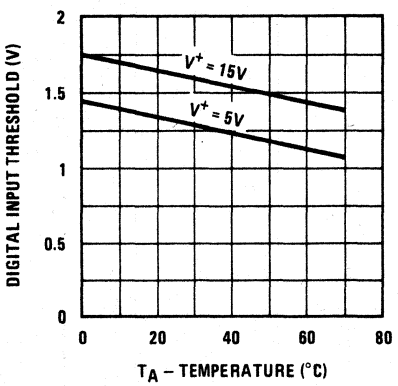


FIGURE 1. Digital Input Threshold vs Ambient Temperature

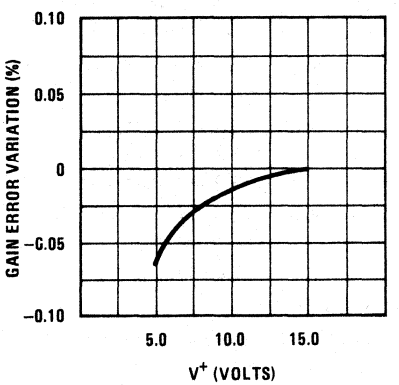


FIGURE 2. Gain Error Variation vs V^+

Typical Applications

The following applications are also valid for 12-bit systems using the DAC1220 and 2 additional digital inputs.

Operational Amplifier Bias Current *(Figure 3)*

The op amp bias current, I_b, flows through the 15k internal feedback resistor. BI-FET op amps have low I_b and, therefore, the 15k x I_b error they introduce is negligible; they are strongly recommended for the DAC1020 applications.

V_{OS} Considerations

The output impedance, R_{OUT}, of the DAC is modulated by the digital input code which causes a modulation of the operational amplifier output offset. It is therefore recommended to adjust the op amp V_{OS}. R_{OUT} is ~15k if more than 4 digital inputs are high; R_{OUT} is ~45k if a single digital input is high, and R_{OUT} approaches infinity if all inputs are low.

Operational Amplifier V_{OS} Adjust *(Figure 3)*

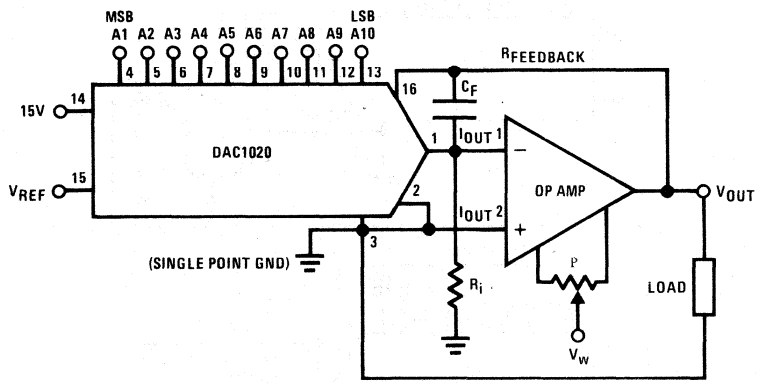
Connect all digital inputs, A1–A10, to ground and adjust the potentiometer to bring the op amp V_{OUT} pin to within ±1 mV from ground potential. If V_{REF} is less than 10V, a finer V_{OS} adjustment is required. It is helpful to increase the resolution of the V_{OS} adjust procedure by connecting a 1 kΩ resistor between the inverting input of the op amp to ground. After V_{OS} has been adjusted, remove the 1 kΩ.

Full-Scale Adjust *(Figure 4)*

Switch high all the digital inputs, A1–A10, and measure the op amp output voltage. Use a 500Ω potentiometer, as shown, to bring $||V_{OUT}||$ to a voltage equal to V_{REF} x 1023/1024.

SELECTING AND COMPENSATING THE OPERATIONAL AMPLIFIER

OP AMP FAMILY	C_F	R_i	P	V_w	CIRCUIT SETTLING TIME, t_s	CIRCUIT SMALL SIGNAL BW
LM357	10 pF	2.4k	25k	V^+	1.5 μs	1M
LM356	22 pF	∞	25k	V^+	3 μs	0.5M
LF351	24 pF	∞	10k	V^-	4 μs	0.5M
LM741	0	∞	10k	V^-	40 μs	200 kHz



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)$$

$$-10V \leq V_{REF} \leq 10V$$

$$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$$

where $A_N = 1$ if the A_N digital input is high
$A_N = 0$ if the A_N digital input is low

FIGURE 3. Basic Connection: Unipolar or 2-Quadrant Multiplying Configuration (Digital Attenuator)

Typical Applications (Continued)

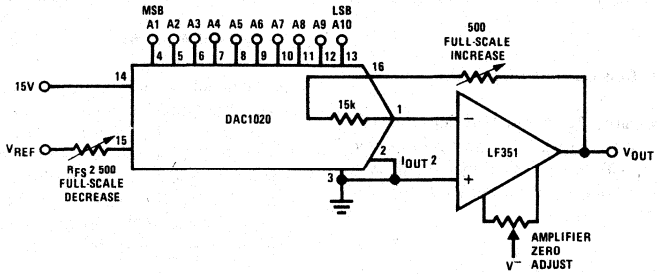


FIGURE 4: Full-Scale Adjust

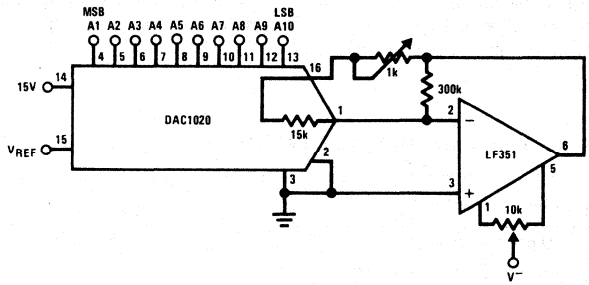
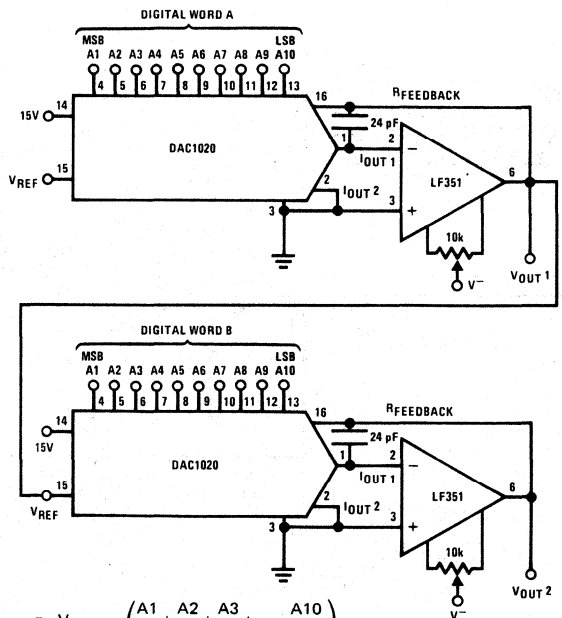


FIGURE 5. Alternate Full-Scale Adjust: (Allows Increasing or Decreasing the Gain)



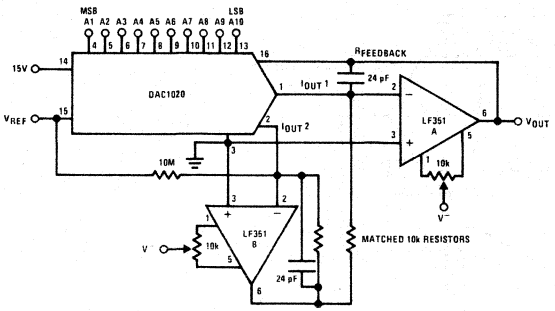
$$V_{OUT1} = -V_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\ldots\frac{A10}{1024}\right)$$

$$V_{OUT2} = V_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\ldots\frac{A10}{1024}\right) \times \left(\frac{B1}{2}+\frac{B2}{4}+\frac{B3}{8}+\ldots\frac{B10}{1024}\right)$$

where V_{REF} can be an AC signal

FIGURE 6. Precision Analog-to-Digital Multiplier

Typical Applications (Continued)



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \ldots + \frac{A10}{1024} - \frac{1}{1024}\right)$$

where: AN = +1 if A_N input is high
AN = −1 if A_N input is low

COMPLEMENTARY OFFSET BINARY (BIPOLAR) OPERATION

DIGITAL INPUT										V_{OUT}
0	0	0	0	0	0	0	0	0	0	$+V_{REF}$
0	0	0	0	0	0	0	0	0	1	V_{REF} x 1022/1024
0	1	1	1	1	1	1	1	1	1	V_{REF} x 2/1024
1	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	$-V_{REF}$ x 2/1024
1	1	1	1	1	1	1	1	1	1	$-V_{REF}$ (1022/1024)

Note that:

- $I_{OUT\,1} + I_{OUT\,2} = \frac{V_{REF}}{R_{LADDER}} \times \left(\frac{1023}{1024}\right)$
- By doubling the output range we get half the resolution
- The 10M resistor, adds a 1 LSB "thump", to allow full offset binary operation where the output reaches zero for the half-scale code. If symmetrical output excursions are required, omit the 10M resistor.

FIGURE 7. Bipolar 4-Quadrant Multiplying Configuration

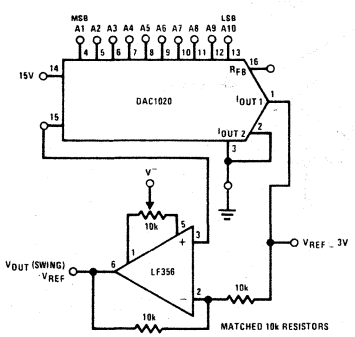
Operational Amplifiers V_{OS} Adjust *(Figure 7)*

a) Switch all the digital inputs high; adjust the V_{OS} potentiometer of op amp B to bring its output to a value equal to $-(V_{REF}/1024)$ (V).

b) Switch the MSB high and the remaining digital inputs low. Adjust the V_{OS} potentiometer of op amp A, to bring its output value to within a 1 mV from ground potential. For $V_{REF} < 10V$, a finer adjust is necessary, as already mentioned in the previous application.

Gain Adjust (Full-Scale Adjust)

Assuming that the external 10k resistors are matched to better than 0.1%, the gain adjust of the circuit is the same with the one previously discussed.

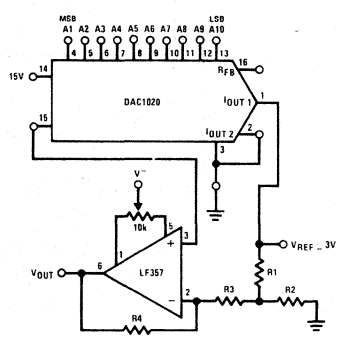


TRUE OFFSET BINARY OPERATION

DIGITAL INPUT										V_{OUT}
1	1	1	1	1	1	1	1	1	1	V_{REF} x 1022/1024
1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	$-V_{REF}$

t_S = 1.8 μs
use LM336 for a voltage reference

FIGURE 8. Bipolar Configuration with a Single Op Amp



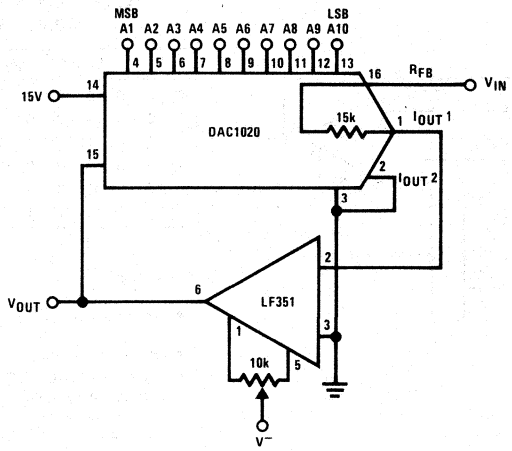
- $R4 = (2A_V^- - 1)R$, $\frac{R2}{R1} = \frac{A_V^-}{A_V^- - 1}$,

  $R3 + R1||R2 = R$; $A_V^- = \frac{V_{OUT(PEAK)}}{V_{REF}}$, R = 20k

- Example: V_{REF} = 2V, V_{OUT} (swing) ≃ ±10V: A_V^- = 5V
  Then R4 = 9R, R1 = 0.8 R2. If R1 = 0.2R then R2 = 0.25R, R3 = 0.64R

FIGURE 9. Bipolar Configuration with Increased Output Swing

Typical Applications (Continued)

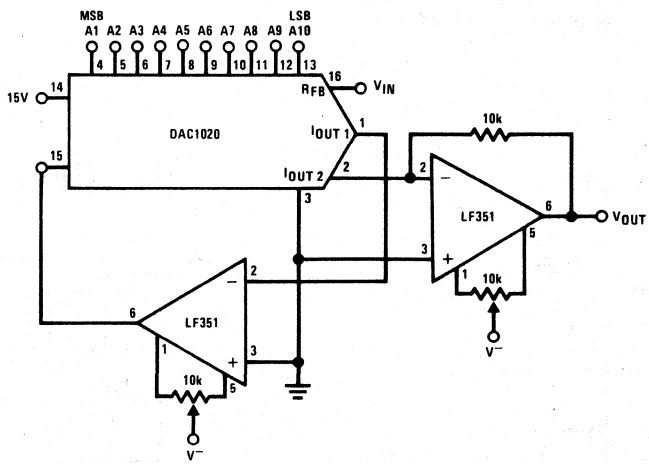


$$V_{OUT} = \frac{-V_{REF}}{\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)}$$

where: V_{REF} can be an AC signal

- By connecting the DAC in the feedback loop of an operational amplifier a linear digitally control gain block can be realized
- Note that with all digital inputs low, the gain of the amplifier is infinity, that is, the op amp will saturate. In other words, we cannot divide the V_{REF} by zero!

FIGURE 10. Analog-to-Digital Divider (or Digitally Gain Controlled Amplifier)

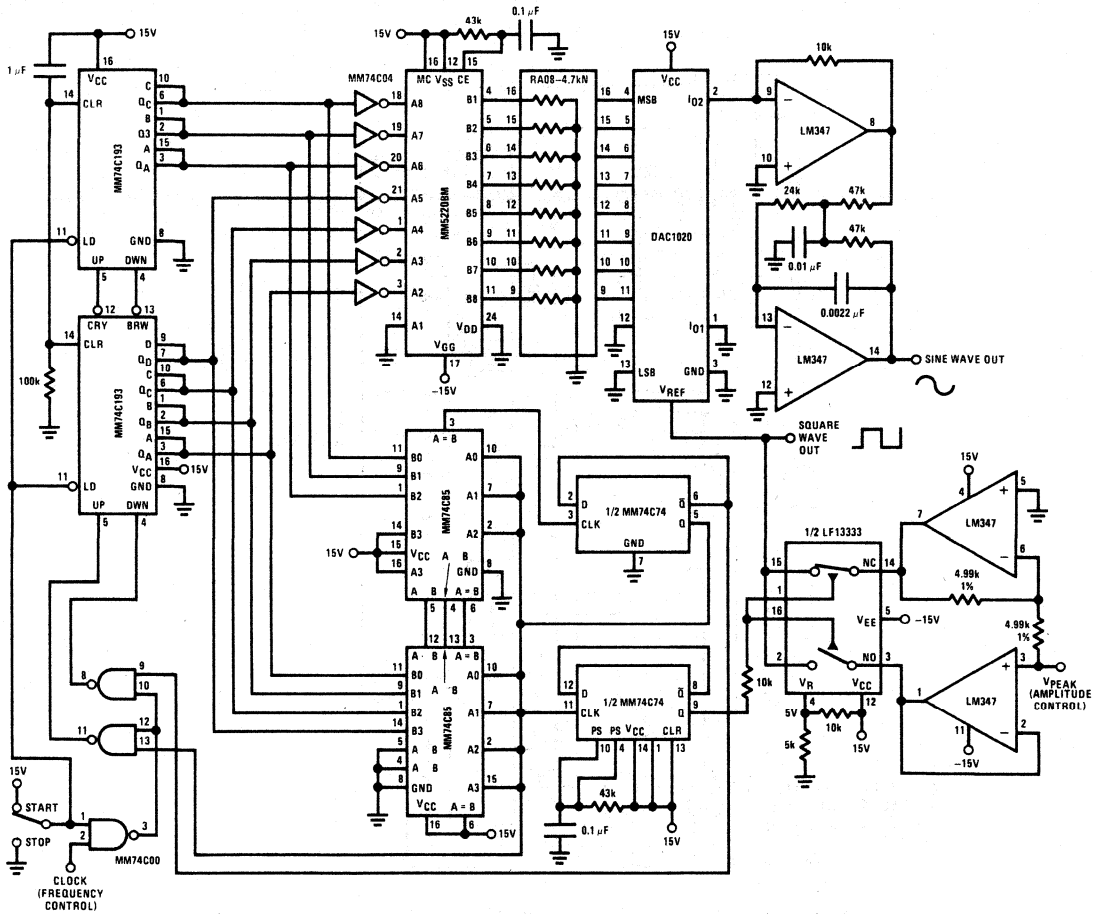


$$V_{OUT} = V_{REF}\left[\frac{\frac{\overline{A1}}{2} + \frac{\overline{A2}}{4} + \ldots + \frac{A10}{1024}}{\frac{A1}{2} + \frac{A2}{4} + \ldots + \frac{\overline{A10}}{1024}}\right] \quad \text{or} \quad V_{OUT} = V_{REF}\left(\frac{1023 - N}{N}\right)$$

where: $0 \leq N \leq 1023$
$N = 0$ for A_N = all zeros
$N = 1$ for A10 = 1, A1–A9 = 0
.
.
.
$N = 1023$ for A_N = all 1's

FIGURE 11. Digitally Controlled Amplifier-Attenuator

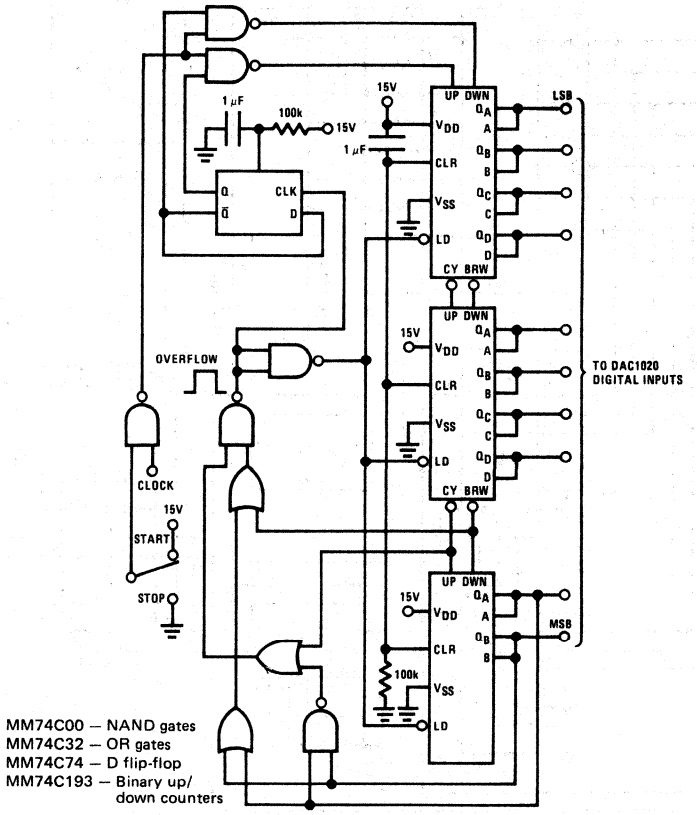
Typical Applications (Continued)



- Output frequency = $\frac{f_{CLK}}{512}$; $f_{MAX} \cong 2$ kHz
- Output voltage range = 0V–10V peak
- THD < 0.2%
- Excellent amplitude and frequency stability with temperature
- Low pass filter shown has a 1 kHz corner (for output frequencies below 10 Hz, filter corner should be reduced)
- Any periodic function can be implemented by modifying the contents of the look up table ROM
- No start up problems

FIGURE 12. Precision Low Frequency Sine Wave Oscillator Using Sine Look-Up ROM

Typical Applications (Continued)



- Binary up/down counter digitally "ramps" the DAC output
- Can stop counting at any desired 10-bit input code
- Senses up or down count overflow and automatically reverses direction of count

FIGURE 13. A Useful Digital Input Code Generator for DAC Attenuator or Amplifier Circuits

Definition of Terms

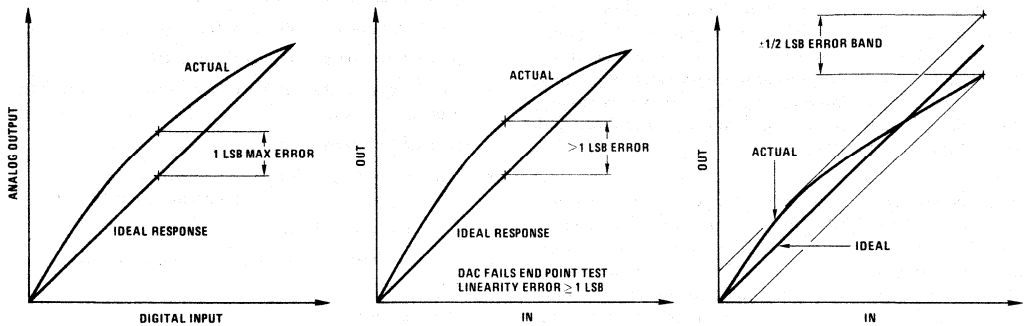
Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the D/A output. It is directly related to the number of switches or bits within the D/A. For example, the DAC1020 has 2^{10} or 1024 steps while the DAC1220 has 2^{12} or 4096 steps. Therefore, the DAC1020 has 10-bit resolution, while the DAC1220 has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from *a straight line passing through the endpoints of the D/A transfer characteristic.* It is measured after calibrating for zero (see V_{OS} adjust in typical applications) and full-scale. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time: Full-scale settling time requires a zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the D/A output reaches within ±1/2 LSB of final output value.

Full-Scale Error: Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1020 full-scale is V_{REF} − 1 LSB. For V_{REF} = 10V and unipolar operation, $V_{FULL\text{-}SCALE}$ = 10.0000V − 9.8 mV = 9.9902V. Full-scale error is adjustable to zero as shown in *Figure 5*.



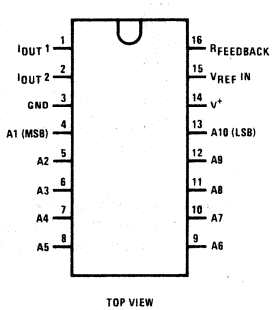
(a) End point test after zero and full-scale adjust. The DAC has 1 LSB linearity error

(b) By shifting the full-scale calibration on of the DAC of *Figure (b1)* we could pass the "best straight line" (b2) test and meet the ±1/2 LSB linearity error specification

Note. (a), (b1) and (b2) above illustrate the difference between "end point" National's linearity test (a) and "best straight line" test. Note that both devices in (a) and (b2) meet the ±1/2 LSB linearity error specification but the end point test is a more "real life" way of characterizing the DAC.

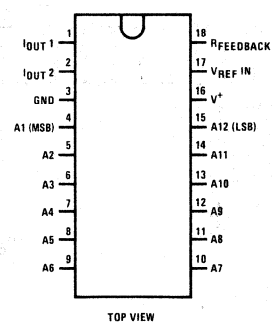
Connection Diagrams

DAC102X
Dual-In-Line Package



TOP VIEW

DAC122X
Dual-In-Line Package



TOP VIEW

National Semiconductor

Digital-to-Analog Converters

DAC1200, DAC1201 12-Bit Digital-to-Analog Converters

General Description

The DAC1200 series of D/A converters is a family of precision low-cost converter building blocks intended to fulfill a wide range of industrial and military D/A applications. These devices are complete functional blocks requiring only application of power for operation. The design combines a precision 12-bit weighted current source (12 current switches and 12-bit thin-film resistor network), a rapid-settling operational amplifier, and 10.24V buffered reference.

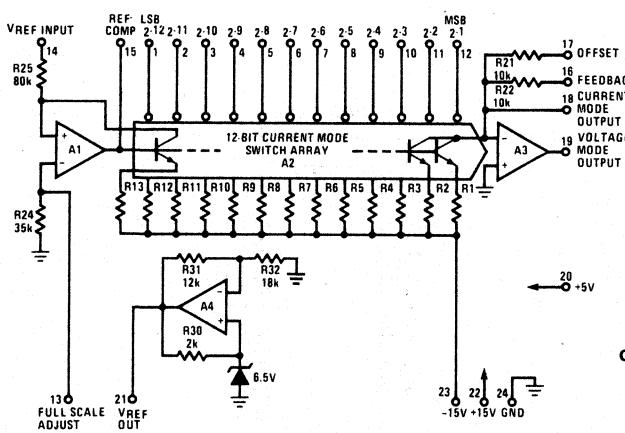
Input coding is complementary binary. In all instances, a logic "low" ($\leq$ 0.8V) turns a given bit ON, and a logic "high" ($\geq$ 2.0V) turns the bit OFF. Output format may be programmed for bipolar (±10V) or unipolar (0 to 10V) operation using internally supplied thin-film resistor pin strap options. Current mode operation is also available from 0 to 2 mA.

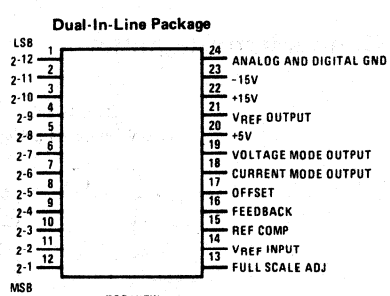
The entire series is available in hermetically sealed 24-lead DIP.

Features

- Circuit completely self-contained
- Both current and voltage-mode outputs
- Standard power supplies: ±15V and +5V
- Internal buffered reference: 10.24V
- 0 to 2 mA, ±10V or 0 to 10V output by strapping internal resistors; other scales by external resistors
- ±1/2 LSB linearity
- Fast settling time: 1.5 μs in current mode
  2.5 μs in voltage mode
- High slew rate: 15 V/μs
- TTL and CMOS compatible complementary binary input logic
- 12 bit linearity
- Standard 0.6" 24-pin DIP package

Block and Connection Diagrams





Order Number DAC1200HD, DAC1200HCD, DAC1201HD or DAC1201HCD
See NS Package D24D

Absolute Maximum Ratings

Supply Voltage (V^+ & V^-)	±18V
Logic Supply Voltage (V_{CC})	+10V
Logic Input Voltage	−0.7V to +18V
Reference Input Voltage	−0V, +18V
Power Dissipation	(see graphs)
Short Circuit Duration (pins 18, 19 & 21)	Continuous
Operating Temperature Range	
DAC1200HD, DAC1201HD	−55°C to +125°C
DAC1200HCD, DAC1201HCD	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec.)	300°C

DC Electrical Characteristics DAC1200,1201 Binary D/A (Notes 1, 2)

PARAMETER	CONDITIONS	DAC1200/1200C			DAC1201/1201C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		12			12			Bits
Linearity Error (Note 3)	T_A = 25°C			±0.0122			±0.0488	% FS
				±0.0244			±0.0976	% FS
Offset Voltage	T_A = 25°C		1	5		1	10	mV
				10			15	mV
Voltage Mode Full-Scale Error (Note 3)	V_{REF} = 10.240V		0.01	0.1		0.02	0.2	% FS
Voltage Mode Full-Scale Error	Pin 21 connected to Pin 14, T_A = 25°C		0.1	0.6		0.1	0.7	% FS
Monotonicity (Notes 3, 4)		Guaranteed over the temperature range						
Voltage Mode Power Supply Sensitivity	ΔV^+ = ±2V, ΔV^- = ±2V, ΔV_{CC} = ±1V; T_A = 25°C, V_{REF} = 10.240V		0.002	0.02		0.002	0.02	% FS/V
			0.002	0.02		0.002	0.02	% FS/V
			0.002	0.02		0.002	0.02	% FS/V
Output Voltage Range	R_L = 5k	±10.5	±12		±10.5	±12		V
Voltage Mode Output Short Circuit Current Limit	T_A = 25°C		20	50		20	50	mA
Current Mode Voltage Compliance	(Note 5)	±2.5			±2.5			V
Current Mode Output Impedance			15			15		kΩ
Reference Voltage	0mA ≤ I_{REF} ≤ 2mA, T_A = 25°C	10.190	10.240	10.290	10.190	10.240	10.290	V
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current (Bit OFF)	V_{IN} = 2.5V		1	10		1	10	μA
Logic "0" Input Current (Bit ON)	V_{IN} = 0V		-10	-100		-10	-100	μA
Power Supply Current I^+	V^+ = 15.0V		10	15		10	15	mA
Power Supply Current I^-	V^- = −15.0V; T_A = 25°C		25	30		25	30	mA
Power Supply Current I_{CC}	V_{CC} = 5.0V		20	25		20	25	mA

AC Electrical Characteristics DAC1200,1201

PARAMETER	CONDITIONS (T_A = 25°C)	MIN	TYP	MAX	UNITS
Voltage Mode ±1 LSB Settling Time (Note 5)	DAC1200, V_ϵ ≤ 1.25 mV		1.5	3.0	μs
	DAC1201, V_ϵ ≤ 5.0 mV		1	3.0	μs
Voltage Mode Full-Scale Change Settling Time (Note 5)	DAC1200, V_ϵ ≤ 1.25 mV		2.5	5.0	μs
	DAC1201, V_ϵ ≤ 5.0 mV		2.0	5.0	μs
Current Mode Full-Scale Settling Time	R_L = 1kΩ, C_L ≤ 20pF; 0 ≤ ΔI_{OUT} ≤ 2mA		1.5		μs
Voltage Mode Slew Rate	−10V ≤ ΔV_{OUT} ≤ +10V		15		V/μs

Note 1: Unless otherwise noted, these specifications apply for V^+ = 15.0V, V^- = −15.0V, and V_{CC} = 5.0V over the temperature range −55°C to +125°C for the DAC1200HD/1201HD and −25°C to +85°C for the DAC1200HCD/1201HCD.

Note 2: All typical values are for T_A = 25°C.

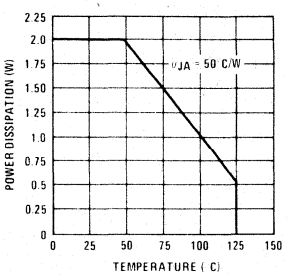
Note 3: Unless otherwise noted, this specification applies for V_{REF} = 10.24V, and over the temperature range −25°C to +85°C. Testing conditions include adjustment of offset to 0V and full-scale to 10.2375V.

Note 4: The DAC1200 is tested for monotonicity by stimulating all bits; the DAC1201 is tested for monotonicity by stimulating only the 10 MSBs and holding the 2 LSBs at 2.0V (i.e., 2 LSBs are OFF).

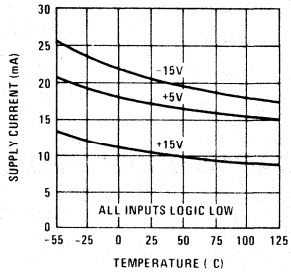
Note 5: Not tested — guaranteed by design.

Typical Performance Characteristics

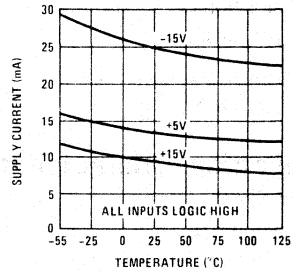
Maximum Power Dissipation



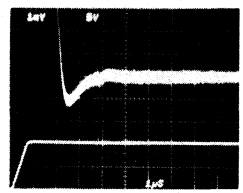
Supply Current vs Temperature



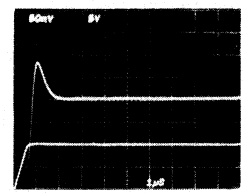
Supply Current vs Temperature



1 LSB Transition
1011 . . . 1 → 1100 . . . 0
V_O = 0, 10V
C_F = 30pF
T_A = 25°C



10V Full Scale Settling Time



10V Full Scale Pulse Response

Applications Information

1. Introduction

The DAC1200 series D/A converters are designed to minimize adjustments and user-supplied external components. For example, included in the package are a buffered reference, offset nulled output amplifier, and application resistors as well as the basic 12-bit current mode D/A.

However, the DAC1200 series is a sophisticated building block. **Its principles of operation and the following applications information should be read before applying power to the device.**

The user is referred to National Semiconductor Application Notes AN-156 and AN-157 for additional information.

2. Power Supply Selection & Decoupling

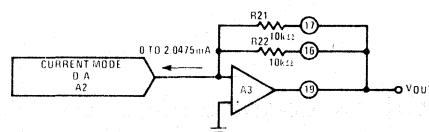
Selection of power supplies is important in applications requiring 0.01% accuracy. The ±15V supplies should be well regulated (±15V ± 0.1%) with less than 0.5mVrms of output noise and hum.

To realize the full speed capability of the device, all three power supply leads should be bypassed with 1μF tantalum electrolytic capacitors in shunt with 0.01μF ceramic disc capacitors no farther than ½ inch from the device package.

3. Unipolar and Bipolar Operation

The DAC1200 series D/A's may be configured for either unipolar or bipolar operation using resistors provided with the device. Figure 1A illustrates the proper connection for unipolar operation.

Bipolar operation is accomplished by offsetting the output amplifier A3 as shown in Figure 2A.



$$^{*}V_{OUT} = (I_{ZERO\ to\ I_{FULLSCALE}})\left(\frac{R21 \cdot R22}{R21 + R22}\right)$$

$$= (0mA \text{ to } 2.0475mA)(5k\Omega)$$

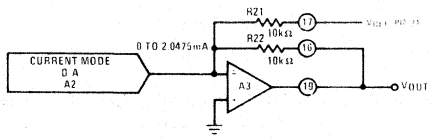
$$= 0V \text{ to } +10.2375V$$

*Values shown are for V_{REF} = 10.240V.

$$1 \text{ LSB Voltage Step} = \frac{10.240V}{4096} = 2.5mV.$$

$$1 \text{ LSB Current Step} = \frac{2.5mV}{5.0k\Omega} = 0.5\mu A$$

FIGURE 1A. DAC1200/DAC1201 Unipolar Operation



$$^{*}V_{OUT} = (0 \text{ to } 2.0475mA)R22 - \frac{V_{REF}}{R22} R21$$

$$= (0 \text{ to } 2.0475mA)R22 - V_{REF}, R21 \equiv R22$$

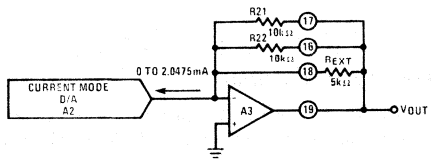
$$= -10.240 \text{ to } +10.235V$$

*Values shown are for V_{REF} = 10.240V

1 LSB = 5mV.

FIGURE 2A. DAC1200/DAC1201 Bipolar Operation

External resistors may be used to achieve alternate zero and full-scale voltages. It is advantageous to utilize R21 and R22 even in these applications since they are closely matched in TCR and temperature to the internal array. Figure 3 illustrates the recommended circuit for zero to 5V operation. R_{EXT} should be of metal film or wire-wound construction with a TCR of less than 10ppm/°C.



$$R_{TOTAL} = (R21) \parallel (R22) \parallel (R_{EXT}) = \frac{V_{FULLSCALE}}{2.0475mA} = 2.5k\Omega.$$

FIGURE 3. DAC1200 0 to 5.120V Operation

4. Offset and Full-Scale Adjust

If higher precision is required in the zero and full-scale, external adjustments may be made. The circuit of figure 4 illustrates the recommended circuit to adjust offset and full-scale of the DAC1200 series. The circuit will work equally well for unipolar or bipolar operation.

In bipolar operation, the offset is adjusted at minus full-scale; in the unipolar case at zero scale.

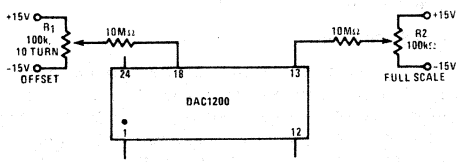


FIGURE 4. Offset & Full-Scale Adjust

For the values shown in figure 4, R1 will allow a ±7mV offset adjustment for the unipolar case and ±15mV for the bipolar case. R2 will allow a ±50mV adjustment of full scale.

5. Current Mode Operation

Access to the summing junction of A3 affords current mode operation either with a resistive load or to drive a fast-settling external operational amplifier. The loop around A3 should not be closed in current mode operation. There is a ±2.5V maximum compliance voltage at A2's output (pin 18) which restricts the maximum size of the load resistor; i.e., $R_L \times I_{FULLSCALE} \leq 2.5V$.

Note: $I_{FULLSCALE} \approx 2$ mA.

6. Settling Time & Glitch Minimization

The settling time of the DAC1200 series and the glitch which occurs between major input code changes may be improved by placing a 10 to 30pF capacitor between pins 18 (current-mode output) and 19 (voltage mode output). The capacitor is used to cancel output capacitance of the current mode D/A and stray capacitance at pin 18.

7. Current Output Boosting

The DAC1200 series may be operated as a "power D/A" by including a current buffer such as the LH0002 or LH0063 in the loop with A3 as shown in figure 5.

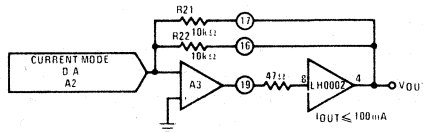


FIGURE 5. Current Boosted Output

8. Logic Input Coding

The sense of the logic inputs to the DAC1200 series is complementary; i.e., a given bit is turned ON by an active "low" input. Table I summarizes input status for the unipolar and bipolar complementary binary and BCD codes.

Other input codes may also be used. For example, the twos complement code, which is used extensively in computer and microprocessor applications, may be converted to the DAC1200 complementary bipolar format by inverting all bits except the MSB. The inversion may be accomplished in the microprocessor by software control, or by hardware using standard hex-inverters.

9. Reference Voltage

External reference voltages may be used with the DAC1200 series. Voltages other than 10.240 or 10.000V in the range of +5.0V to 11V will work satisfactorily for voltage mode operation. Full-scale voltage is always V_{REF} − 1 LSB where 1 LSB = $V_{REF}/4096$. Full-scale current may be predicted by:

$$I_{FULLSCALE} = (V_{REF})(0.19995117)mA$$

CODE TYPE	(Note 8) INPUT CODE MSB LSB	OUTPUT STATE	OUTPUT VOLTAGE V_{REF} = 10.240V	OUTPUT CURRENT
Unipolar Complementary Binary	0000 0000 0000	Full-Scale	+10.2375V	2.0475mA
	1111 1111 1110	1 LSB ON	+2.500mV	0.500μA
	1111 1111 1111	Zero Scale	Zero	Zero
Bipolar Complementary Binary	0000 0000 0000	Full-Scale	+10.235V	+1.0235mA
	0111 1111 1111	Half Full-Scale	-0.000V	0.000mA
	1111 1111 1110	1 LSB ON	-10.235V	-1.0235mA
	1111 1111 1111	Zero Scale	-10.240V	-1.0240mA

Note 8: Logic input sense is such that an active low ($V_{IN} \leq 0.8V$) turns a given bit ON and is represented as a logic "0" in the table.

Definition of Terms

Resolution

Resolution is defined as the reciprocal of the number of discrete steps in the D/A output (as designed). It is directly related to the number of switches or bits within the D/A. For example, the DAC1200 has 2^{12} or 4096 steps. Resolution may therefore be expressed variously as 12 bits, as 1 part in 2^{12}, as 1 part in 4096, or as a percentage (1/4096 x 100 = 0.0244%).

Linearity Error

Linearity error is the maximum deviation from a straight line passing through the endpoints of the D/A transfer characteristic. It is measured after calibrating for zero and full-scale. The linearity error of the DAC1200 series is guaranteed to be less than ±½ LSB or 0.0122% of F.S. for the DAC1200/1200C and ±0.0488% of F.S. for the DAC1201/DAC1201C. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Offset Voltage

Offset voltage is an output voltage other than zero volts for unipolar operation (and other than minus full-scale for bipolar operation) with all bits turned OFF. In the DAC1200 series this error resides primarily in the output amplifier, A3. Offset voltage is adjustable to zero as discussed in the applications section.

Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time

Two settling time parameters are specified for the DAC1200 series. Full-scale settling time requires a zero to full-scale or full-scale to zero output change. One LSB settling time requires one LSB output change. In both instances, settling time is the time required from a code transition until the D/A output reaches within ±½ LSB of final output value.

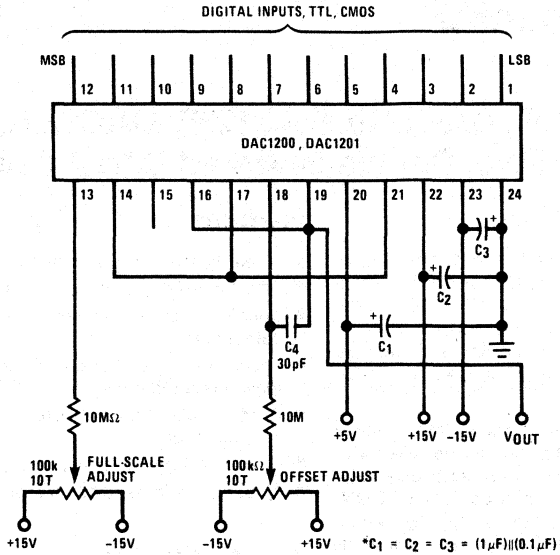
Monotonicity

Monotonicity is a characteristic of the D/A which requires a non-negative output step for an increasing input digital code. Monotonicity, therefore, demands no back steps or changes in sign of the slope of the D/A transfer characteristic.

Full-Scale Error

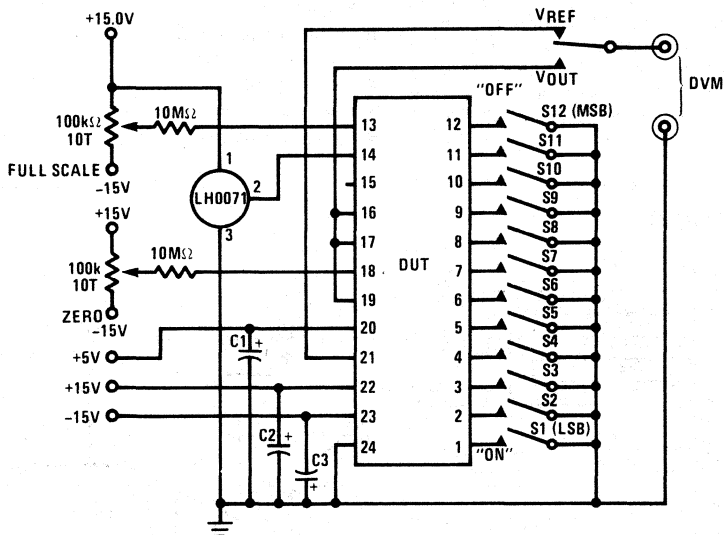
Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1200 full-scale is V_{REF} − 1 LSB. For V_{REF} = 10.240V and unipolar operation, $V_{FULLSCALE}$ = 10.240V − 2.5mV = 10.2375V. Departures from this value include internal gain, scaling, and reference errors. Full-scale error is adjustable to zero as discussed in the **Applications** section.

Typical Application



20 Volt Full-Scale Complementary D/A

DC Test Circuit



C1 = C2 = C3 = 4.7μF (solid tantalum) in parallel with a 0.01μF ceramic disc

Ordering Information

PART NUMBER	PACKAGE	25°C LINEARITY ERROR	OPERATING TEMPERATURE RANGE
DAC1200HD	Ceramic DIP	0.01%	−55°C to +125°C
DAC1201HD	Ceramic DIP	0.05%	−55°C to +125°C
DAC1200HCD	Ceramic DIP	0.01%	−25°C to +85°C
DAC1201HCD	Ceramic DIP	0.05%	−25°C to +85°C

National Semiconductor

Digital-to-Analog Converters
PRELIMINARY

MICRO-DAC™
DAC1208, DAC1209, DAC1210, DAC1230, DAC1231, DAC1232
12-Bit, μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1208 and the DAC1230 series are 12-bit multiplying D to A converters designed to interface directly with a wide variety of microprocessors (8080, 8048, 8085, Z-80, etc.). Double buffering input registers and associated control lines allow these DACs to appear as a two-byte "stack" in the system's memory or I/O space with no additional interfacing logic required.

The DAC1208 series provides all 12 input lines to allow single buffering for maximum throughput when used with 16-bit processors. These input lines can also be externally configured to permit an 8-bit data interface. The DAC1230 series can be used with an 8-bit data bus directly as it internally formulates the 12-bit DAC data from its 8 input lines. All of these DACs accept left-justified data from the processor.

The analog section is a precision silicon-chromium (Si-Cr) R-2R ladder network and twelve CMOS current switches. An inverted R-2R ladder structure is used with the binary weighted currents switched between the I_{OUT1} and I_{OUT2} maintaining a constant current in each ladder leg independent of the switch state. Special circuitry provides TTL logic input voltage level compatibility.

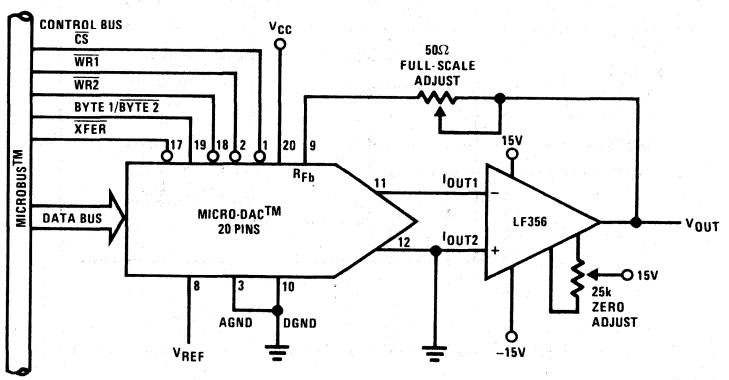
Features

- Linearity specified with zero and full-scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow through digital data inputs
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates stand-alone (without μP) if desired
- All parts guaranteed 12-bit monotonic

Key Specifications

■ Current Settling Time	1 μs
■ Resolution	12 Bits
■ Linearity (Guaranteed over temperature)	10, 11, or 12 Bits
■ Gain Tempco	1.5 ppm/°C
■ Low Power Dissipation	20 mW
■ Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



Ordering Information

Accuracy	Package	
	20-Pin D20A	24-Pin D24C
0.012%	DAC1230LCD	DAC1208LCD
0.024%	DAC1231LCD	DAC1209LCD
0.05%	DAC1232LCD	DAC1210LCD

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	± 25V
Storage Temperature Range	− 65°C to + 150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	− 100 mV to V_{CC}
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	− 40°C to + 85°C
Range of V_{CC}	4.75 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics T_A = 25°C, V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units	Notes
Resolution		12	12	12	Bits	
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted					4, 7
	$T_{MIN} < T_A < T_{MAX}$					6
	$-10V \le V_{REF} \le 10V$					5
	DAC1208, DAC1230			0.012	% of FSR	
	DAC1209, DAC1231			0.024	% of FSR	
	DAC1210, DAC1232			0.05	% of FSR	
Differential Non-Linearity	Zero and Full-Scale Adjusted					4, 7
	$T_{MIN} < T_A < T_{MAX}$					6
	$-10V \le V_{REF} \le 10V$					5
	DAC1208, DAC1230			0.012	% of FSR	
	DAC1209, DAC1231			0.024	% of FSR	
	DAC1210, DAC1232			0.05	% of FSR	
Monotonicity	$T_{MIN} < T_A < T_{MAX}$					4, 6
	$-10V \le V_{REF} \le 10V$	12	12	12	Bits	5
Gain Error	Using Internal R_{Fb}					
	$-10V \le V_{REF} \le 10V$	− 0.2	− 0.01	0.0	% of FSR	5
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$					6, 7
	Using Internal R_{Fb}		± 1.3	± 6.0	ppm of FS/°C	10
Power Supply Rejection	All Digital Inputs Latched High		± 3.0		ppm of FSR/V	7
Reference Input Resistance		10	15	20	kΩ	
Output Feedthrough Error	V_{REF} = 20 Vp-p, f = 100 kHz All Data Inputs Latched Low		3		mVp-p	9
Output Capacitance	All Data Inputs Latched High — I_{OUT1}		200		pF	
	I_{OUT2}		70		pF	
	All Data Inputs Latched Low — I_{OUT1}		70		pF	
	I_{OUT2}		200		pF	
Supply Current Drain	$T_{MIN} \le T_A \le T_{MAX}$		1.2	2.0	mA	6
Output Leakage Current	$T_{MIN} \le T_A \le T_{MAX}$					6, 11
I_{OUT1}	All Data Inputs Latched Low			10	nA	11
I_{OUT2}	All Data Inputs Latched High			10	nA	
Digital Input Threshold	$T_{MIN} \le T_A \le T_{MAX}$					6
	Low Threshold			0.8	V_{DC}	
	High Threshold	2.0			V_{DC}	
Digital Input Currents	$T_{MIN} \le T_A \le T_{MAX}$					6
	Digital Inputs < 0.8V		− 50	− 200	μA_{DC}	
	Digital Inputs > 2.0V		0.1	10	μA_{DC}	

Electrical Characteristics (Continued)

$T_A = 25°C$, $V_{REF} = 10.000\ V_{DC}$, $V_{CC} = 11.4\ V_{DC}$ to $15.75\ V_{DC}$ unless otherwise noted.

	Parameter	Conditions	Min	Typ	Max	Units	Notes
t_S	Full-Scale Current Settling Time	$R_L = 100\Omega$, Output Settled to 0.01% $\overline{CS} = \overline{WR1} = \overline{WR2} = \overline{XFER} = 0V$, Byte1/$\overline{Byte2} = 5V$, DI_0 through DI_{11} Switched Simultaneously		1		μs	
t_W	Write and XFER Pulse Width	$V_{IL} = 0V$, $V_{IH} = 5V$	320	50		ns	8, 10
		$T_{MIN} \le T_A \le T_{MAX}$	320	80	—	ns	6, 8, 10
t_{DS}	Data Set-Up Time	$V_{IL} = 0V$, $V_{IH} = 5V$	320	70		ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	320	80	—	ns	6, 10
t_{DH}	Data Hold Time	$V_{IL} = 0V$, $V_{IH} = 5V$	90	50		ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	90	60		ns	6, 10
t_{CS}	Control Set-Up Time	$V_{IL} = 0V$, $V_{IH} = 5V$	320	60	—	ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	320	100	—	ns	6, 10
t_{CH}	Control Hold Time	$V_{IL} = 0V$, $V_{IH} = 5V$	10	0		ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	10	0	—	ns	6, 10

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these "Absolute Maximum" limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

Note 6: $T_{MIN} = -40°C$ and $T_{MAX} = 85°C$.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1208 is 0.012% of FSR(max). This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% × V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR (parts per million of full-scale range) and ppm of FS (parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. In this instance, 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ±6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from −40°C to +85°C of $\pm(6)(V_{REF}/10^6)(125°C)$ or $\pm 0.75\ (10^{-3})\ V_{REF}$ which is ±0.075% of V_{REF}.

Note 8: This spec implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH} and t_S to apply.

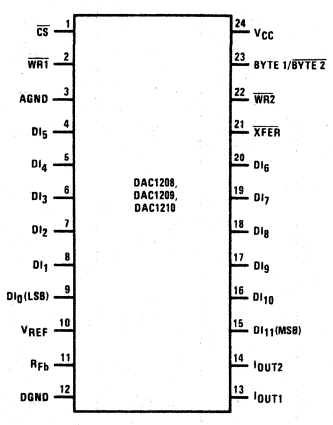
Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 10: Guaranteed by design but not tested.

Note 11: A 10 nA leakage current with $R_{Fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

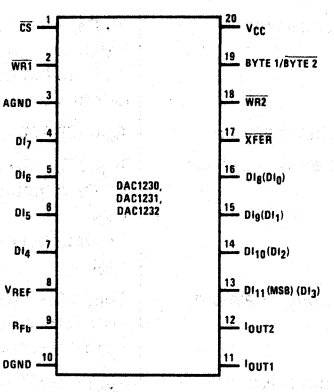
Connection Diagrams

Dual-In-Line Package



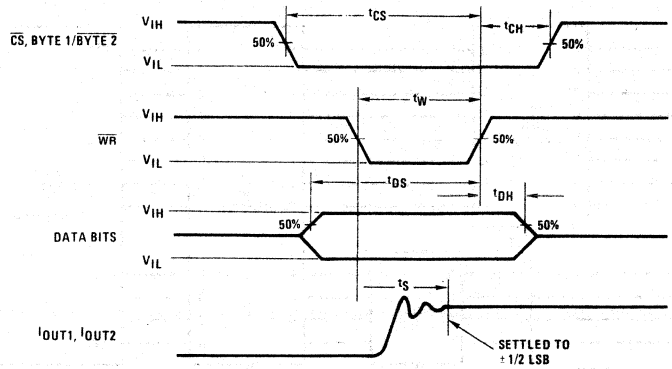
TOP VIEW

Dual-In-Line Package



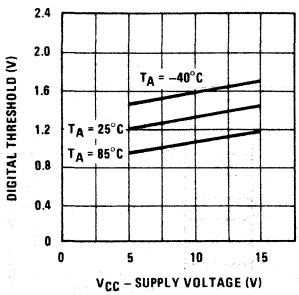
TOP VIEW

Switching Waveforms

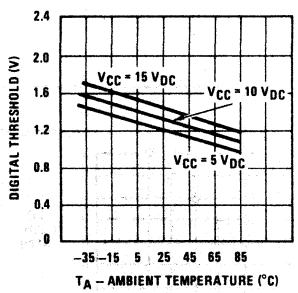


Typical Performance Characteristics

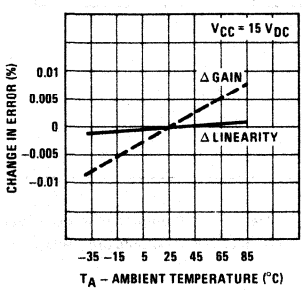
Digital Input Threshold vs V_{CC}



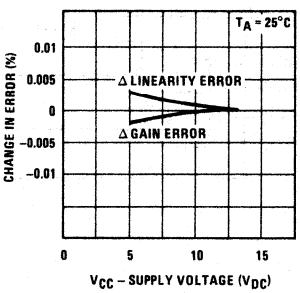
Digital Input Threshold vs Temperature



Gain and Linearity Error Variation vs Temperature

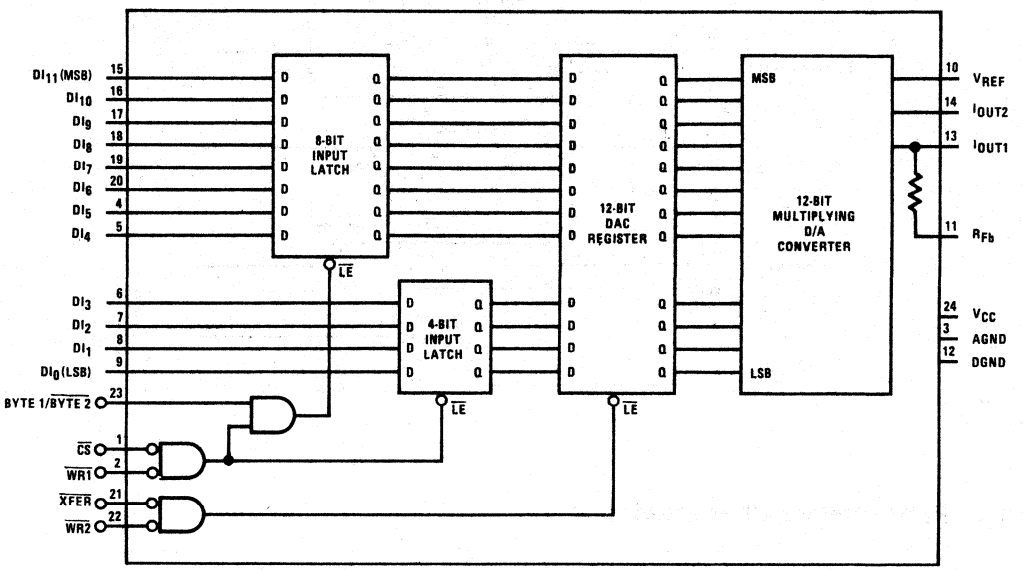


Gain and Linearity Error Variation vs Supply Voltage



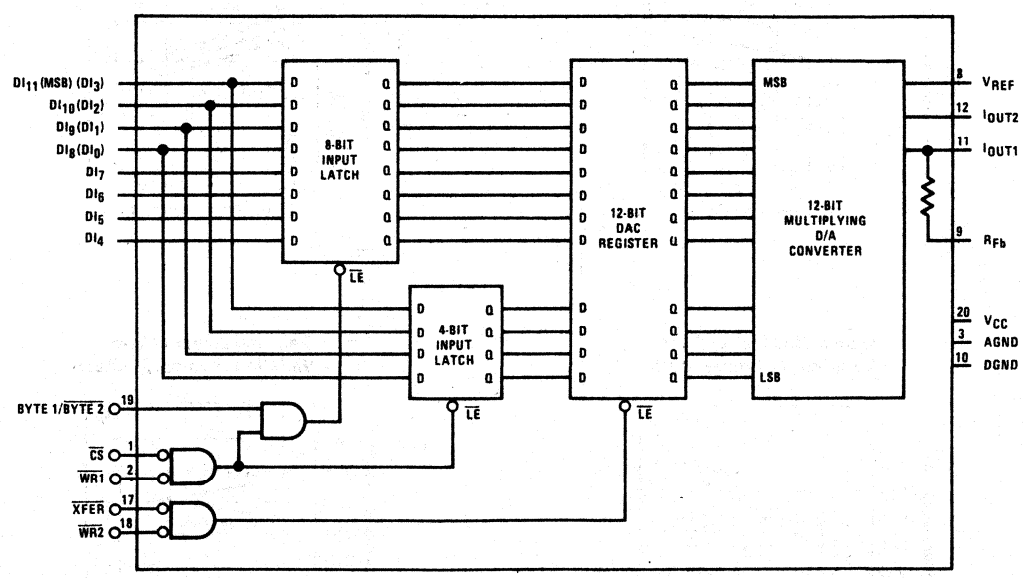
Functional Diagrams

DAC1208, DAC1209, DAC1210



When $\overline{LE}$ = 1, Q outputs follow D inputs
When $\overline{LE}$ = 0, Q outputs are latched

DAC1230, DAC1231, DAC1232



When $\overline{LE}$ = 1, Q outputs follow D inputs
When $\overline{LE}$ = 0, Q outputs are latched

Definition of Package Pinouts

CONTROL SIGNALS (all control signals are level actuated).

$\overline{CS}$: Chip Select (active low). The $\overline{CS}$ will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1. The active low $\overline{WR1}$ is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR1}$ is high. The 12-bit input latch is split into two latches, one holds the first 8 bits, while the other holds 4 bits. The Byte 1/$\overline{Byte\ 2}$ control pin is used to select both latches when Byte 1/$\overline{Byte\ 2}$ is high or to overwrite the 4-bit input latch when in the low state.

Byte 1/$\overline{Byte\ 2}$: Byte Sequence Control. When this control is high, all 12 locations of the input latch are enabled. When low, only the four least significant locations of the input latch are enabled.

$\overline{WR2}$: Write 2 (active low). The $\overline{WR2}$ will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer Control Signal (active low). This signal, in combination with $\overline{WR2}$, causes the 12-bit data which is available in the input latches to transfer to the DAC register.

OTHER PIN FUNCTIONS

DI_0 to DI_{11}: Digital Inputs. DI_0 is the least significant digital input (LSB) and DI_{11} is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1s in the DAC register, and is zero for all 0s in the DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} = \text{constant}$ (for a fixed reference voltage). This constant current is

$$V_{REF} \times \left(1 - \frac{1}{4096}\right)$$

divided by the reference input resistance.

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

AGND: Analog Ground. This is the ground for the analog circuitry.

DGND: Digital Ground. This is the ground for the digital logic.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1208 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

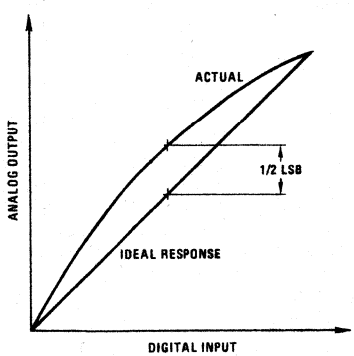
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± 1/2 LSB of the final output value.

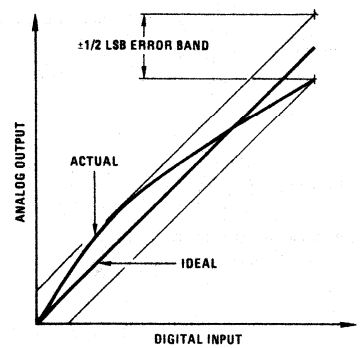
Full-Scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1208 or DAC1230 series, full-scale is V_{REF}−1 LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 2.44\ mV = 9.9976V$. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End point test after zero and FS adjust



b) Shifting FS adjust to pass best straight line test

National Semiconductor

Digital-to-Analog Converters
PRELIMINARY

DAC1218, DAC1219 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1218 and the DAC1219 are 12-bit binary, 4-quadrant multiplying D to A converters. The linearity, differential non-linearity and monotonicity specifications for these converters are all guaranteed over temperature. In addition, these parameters are specified with standard zero and full-scale adjustment procedures as opposed to the impractical best fit straight line guarantee.

This level of precision is achieved through the use of an advanced silicon-chromium (SiCr) R-2R resistor ladder network. This type of thin-film resistor eliminates the parasitic diode problems associated with diffused resistors to allow the applied reference voltage to range from −25V to 25V, independent of the logic supply voltage.

CMOS current switches and drive circuitry are used to achieve low power consumption (20 mW typical) and minimize output leakage current errors (10 nA maximum). Unique digital input circuitry maintains TTL compatible input threshold voltages over the full operating supply voltage range.

The DAC1218 and DAC1219 are direct replacements for the AD7541 series, AD7521 series, and AD7531 series with a significant improvement in the linearity specification. In applications where direct interface of the D to A converter to a microprocessor bus is desirable, the DAC1208 and DAC1230 series eliminate the need for additional interface logic.

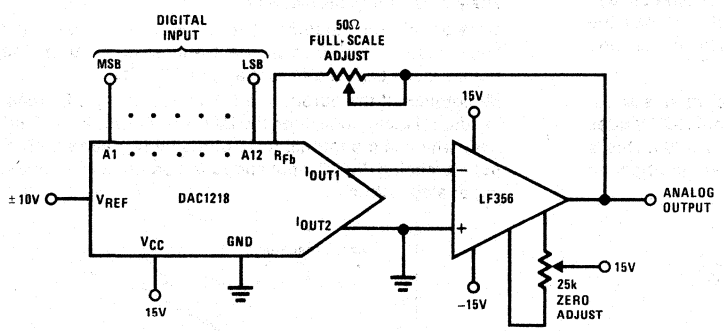
Features

- Linearity specified with zero and full-scale adjust only
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- All parts guaranteed 12-bit monotonic

Key Specifications

■ Current Settling Time	1 μs
■ Resolution	12 Bits
■ Linearity (Guaranteed over temperature)	12 Bits (DAC1218) 11 Bits (DAC1219)
■ Gain Tempco	1.5 ppm/°C
■ Low Power Dissipation	20 mW
■ Single Power Supply	$5 V_{DC}$ to $15 V_{DC}$

Typical Application

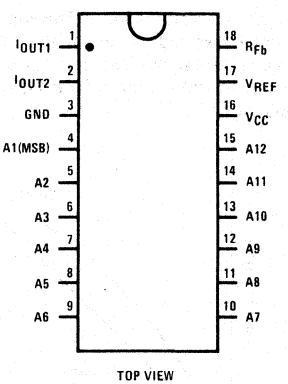


$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high
AN = 0 if digital input is low

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DAC1218LCD or DAC1219LCD
See NS Package D18A
Order Number DAC1218LCN or DAC1219LCN
See NS Package N18A

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	± 25V
Storage Temperature Range	− 65°C to + 150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	− 100 mV to V_{CC}
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	
LCD Suffix	− 40°C to + 85°C
Range of V_{CC}	5 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics T_A = 25°C, V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted.

	Parameter	Conditions	Min	Typ	Max	Units	Notes
	Resolution		12	12	12	Bits	
	Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted					4, 7
		$T_{MIN} < T_A < T_{MAX}$					6
		$-10V \le V_{REF} \le 10V$					5
		DAC1218			0.012	% of FSR	
		DAC1219			0.024	% of FSR	
	Differential Non-Linearity	Zero and Full-Scale Adjusted					4, 7
		$T_{MIN} < T_A < T_{MAX}$					6
		$-10V \le V_{REF} \le 10V$					5
		DAC1218			0.012	% of FSR	
		DAC1219			0.024	% of FSR	
	Monotonicity	$T_{MIN} < T_A < T_{MAX}$					4, 6
		$-10V \le V_{REF} \le 10V$	12	12	12	Bits	5
	Gain Error	Using Internal R_{Fb}					
		$-10V \le V_{REF} \le 10V$	− 0.2	− 0.01	0.0	% of FSR	5, 7
	Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$					6, 7
		Using Internal R_{Fb}		± 1.3	± 6.0	ppm of FS/°C	9
	Power Supply Rejection	All Digital Inputs High		± 3.0		ppm of FSR/V	7
	Reference Input Resistance		10	15	20	kΩ	
	Output Feedthrough Error	V_{REF} = 20 Vp-p, f = 100 kHz All Data Inputs Low		3		mVp-p	9
		D Package		3		mVp-p	8
	Output Capacitance	All Data Inputs High I_{OUT1}		200		pF	
		All Data Inputs High I_{OUT2}		70		pF	
		All Data Inputs Low I_{OUT1}		70		pF	
		All Data Inputs Low I_{OUT2}		200		pF	
	Supply Current Drain	$T_{MIN} \le T_A \le T_{MAX}$		1.2	2.0	mA	6
	Output Leakage Current	$T_{MIN} \le T_A \le T_{MAX}$					6, 10
	I_{OUT1}	All Data Inputs Low			10	nA	
	I_{OUT2}	All Data Inputs High			10	nA	
	Digital Input Threshold	$T_{MIN} \le T_A \le T_{MAX}$					6
		Low Threshold			0.8	V_{DC}	
		High Threshold	2.0			V_{DC}	
	Digital Input Currents	$T_{MIN} \le T_A \le T_{MAX}$					6
		Digital Inputs < 0.8V		− 50	− 200	μA_{DC}	
		Digital Inputs > 2.0V		0.1	10	μA_{DC}	
t_S	Current Settling Time	R_L = 100Ω, Output Settled to 0.01%, All Digital Inputs Switched Simultaneously					

Electrical Characteristics Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these "Absolute Maximum" limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

Note 6: $T_{MIN} = -40°C$ and $T_{MAX} = 85°C$ for "LCD" suffix parts.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1218 is 0.012% of FSR. This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% × V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR (parts per million of full-scale range) and ppm of FS (parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ±6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from −40°C to +85°C of $\pm(6)(V_{REF}/10^6)(125°C)$ or $\pm 0.75\ (10^{-3})\ V_{REF}$ which is ±0.075% of V_{REF}.

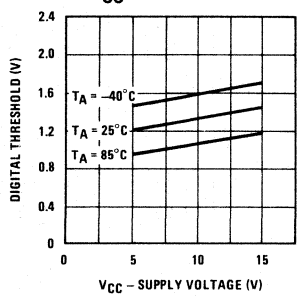
Note 8: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 9: Guaranteed by design but not tested.

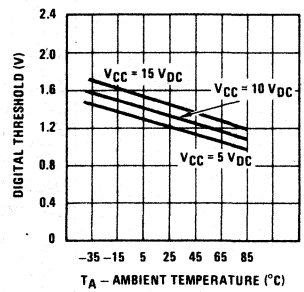
Note 10: A 10 nA leakage current with $R_{Fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

Typical Performance Characteristics

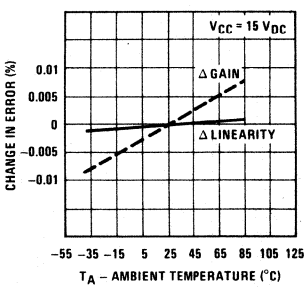
Digital Input Threshold vs V_{CC}



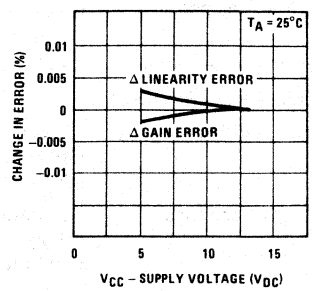
Digital Input Threshold vs Temperature



Gain and Linearity Error Variation vs Temperature



Gain and Linearity Error Variation vs Supply Voltage



Definition of Package Pinouts

A1 to A12: Digital Inputs. A12 is the least significant digital input (LSB) and A1 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital input of all 1s, and is zero for a digital input of all 0s.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2}$ = constant (for a fixed reference voltage).

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects to an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Ground. This is the ground for the circuit.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1218 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

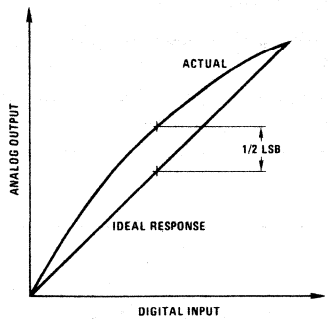
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± 1/2 LSB of the final output value.

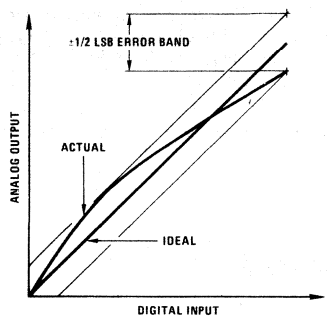
Full-Scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1218 full-scale is V_{REF}–1 LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} =$ 10.0000V - 2.44 mV = 9.9976V. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End point test after zero and FS adjust



b) Shifting FS adjust to pass best straight line test

National Semiconductor

DAC1280, DAC1285 12-Bit Digital-to-Analog Converters

General Description

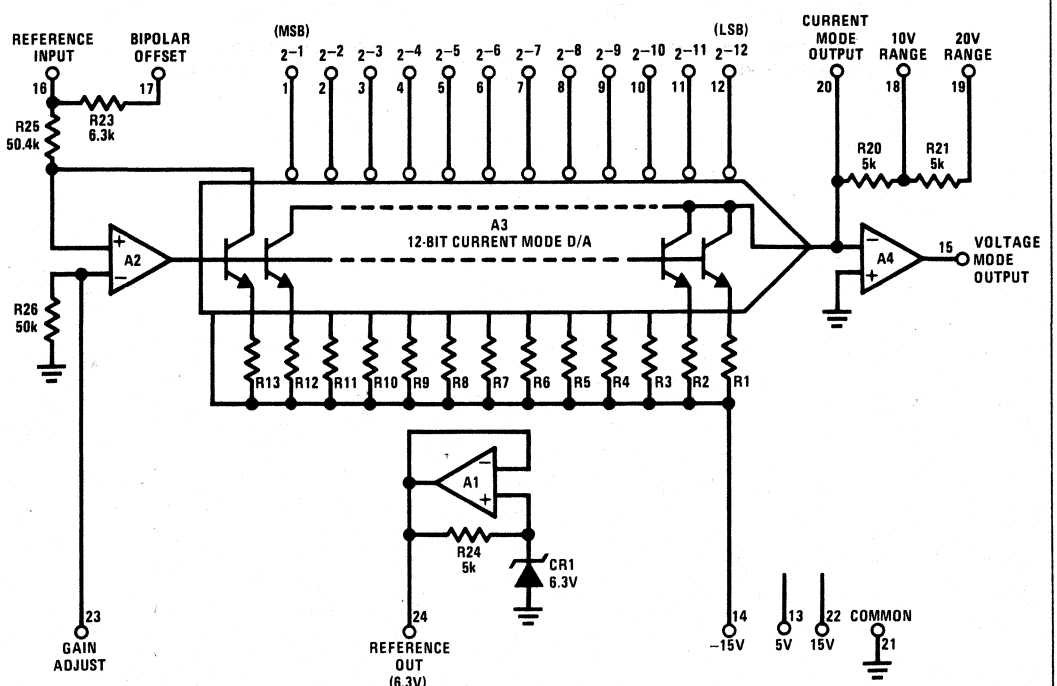
The DAC1280 series is a family of precision, low cost, fully self-contained digital-to-analog converters. The devices include 12 precision current switches, a 12-bit thin film resistor network, output amplifier, buffered internal reference, and several precision resistors, which allow the user to tailor his system needs to accommodate a variety of bipolar and unipolar output voltage and current ranges. Logic inputs are TTL, DTL and CMOS compatible, and are complementary binary (CBI) format. In all instances, a logic low ($\leq$ 0.8V) turns a given bit ON, and a logic high ($\geq$ 2V) turns a given bit OFF. Internally supplied resistor options provide low drift bipolar output voltage ranges of ±2.5V, ±5V, ±10V, and unipolar ranges of 0 to 5V or 0 to 10V. Current mode output is 0 to 2 mA.

The entire series is available in a side-brazed ceramic 24-lead DIP.

Features

- Completely self-contained with no external components required
- ±1/2 LSB linearity
- Standard power supplies: ±15V, 5V
- TTL, DTL, CMOS compatible binary input logic
- ±2.5V, ±5V, ±10V, 0 to 5V, 0 to 10V voltage outputs
- 0 to 2 mA current output
- Internal reference
- Fast settling time: 300 ns current mode, 2.5 μs voltage mode
- Pin compatible with DAC80, DAC85 and DAC87 series
- Full military temperature range operation

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V+ and V−)	±18V
Logic Supply Voltage (V_{CC})	10V
Logic Input Voltage	−0.7V, 18V
Reference Input Voltage (V_{REF})	0V, 18V
Power Dissipation	(See graph)
Short-Circuit Duration (Pins 15, 20 and 24)	Continuous

Operating Temperature Range	
DAC1285HD	−55°C to +125°C
DAC1285HCD DAC1280HCD	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics DAC1285H, DAC1285HC, DAC1280HC Binary D/A (Notes 1 and 2)

PARAMETER	CONDITIONS	DAC1285HD			DAC1285HCD			DAC1280HCD			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		12			12			12			Bits
Linearity Error	$T_A = 25°C$			±1/2			±1/2			±1	LSB
	$T_{MIN} \leq T_A \leq T_{MAX}$, (Note 3)			±1/2			±1/2			±2	LSB
Differential Non-Linearity			±1/2			±1/2			±1/2		LSB
Zero-Scale Error (Offset)	(Notes 4 and 5)		±0.05			±0.05			±0.05		% FSR
Zero-Scale Drift (Offset Drift)	Unipolar, $T_{MIN} \leq T_A \leq T_{MAX}$		±1			±1			±1		ppm of FSR/°C
	Bipolar, $T_{MIN} \leq T_A \leq T_{MAX}$		±3	±10		±3	±15		±10		ppm of FSR/°C
Full-Scale Error (Gain Error)	(Note 5)		±0.1			±0.1			±0.1		% of FSR
Full-Scale Drift (Gain Drift)	$T_{MIN} \leq T_A \leq T_{MAX}$			±20			±30		±10		ppm/°C
Output Voltage Range	Using Internally Supplied Resistors	±2.5, ±5.0, ±10, 0 to +5, 0 to +10									V
Output Voltage Swing	$R_L \geq 5\ k\Omega$, Pin 15	±10	±12		±10	±12		±10	±12		V
Output Short-Circuit Current	Pin 15		±20			±20			±20		mA
Output Impedance	Pin 15, Closed Loop		0.05			0.05			0.05		Ω
Current Mode Output Range	Unipolar, Pin 20	0 to −2 mA									mA
	Bipolar, Pin 20	±1.0									
Current Mode Compliance		±2.5			±2.5			±2.5			V
Current Mode Output Impedance	Unipolar		15			15			15		kΩ
	Bipolar		4.4			4.4			4.4		kΩ
Reference Voltage	$-2\ mA \leq I_{REF} \leq 2\ mA$	6.0	6.3	6.6	6.0	6.3	6.6		6.3		V
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8			0.8	V
Logic "1" Input Current	$V_{IN} = 2.5V$		1	10		1	10		1	10	μA
Logic "0" Input Current	$V_{IN} = 0V$		−10	−100		−10	−100		−10	−100	μA
Power Supply Current	I+		10			10			10		mA
	I−		25			25			25		mA
	I_{CC}		20			20			20		mA
Power Supply Sensitivity			0.002			0.002			0.002		% of FSR/%V

Note 1: Unless otherwise specified, these specifications apply for $V^+ = 15V$, $V^- = -15V$ and $V_{CC} = 5V$ over the entire temperature range −55°C to +125°C for DAC1285HD and −25°C to +85°C for DAC1285HCD and DAC1280HCD. For specified operation, the internal reference (pin 24) must be connected to the reference input (pin 16). The specifications are guaranteed after 30 seconds of warm-up after power turn-on.

Note 2: All typical values are for $T_A = 25°C$.

Note 3. These specifications apply to the limited temperature range $T_{MIN} = -25°C$ to $T_{MAX} = +85°C$ for the DAC1285HD, and $T_{MIN} = 0°C$ to $T_{MAX} = +70°C$ for DAC1285HCD and DAC1280HCD. For the entire temperature range, double the above specifications.

Note 4: FSR means "full-scale range" and is 20V for ±10V range, 10V for ±5V, etc.

Note 5: Externally adjustable to zero.

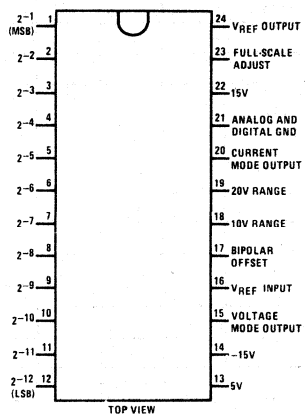
AC Electrical Characteristics $T_A = 25°C$, (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Mode ±1 LSB Settling Time					
DAC1285	$V_E \leq 1$ mV		1.5	3.0	μs
DAC1280C	$V_E \leq 5$ mV		1.5	3.0	μs
Voltage Mode Full-Scale Settling Time	$V_E \leq 1$ mV		2.5	5.0	μs
Current Mode Full-Scale Settling Time	$R_L = 100\Omega$		300		ns
Voltage Mode Slew Rate	$-10V \leq V_{OUT} \leq +10V$		20		V/μs

Note 6: Not tested, guaranteed by design.

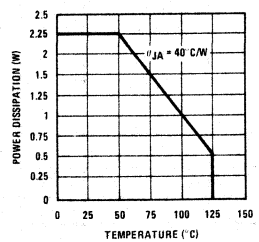
Connection Diagram

Dual-In-Line Package



Typical Performance Characteristics

Maximum Power Dissipation



Functional Description

The DAC1280 series is a sophisticated D/A building block. The user is encouraged to read the following applications information before applying power to the device. Refer to National Semiconductor Application Notes AN-156 and AN-159 for additional applications information.

Selection of power supplies is important in applications requiring 0.01% accuracy. The ±15V supplies should be well regulated (±15V ±0.1% with less than 0.5 mVrms of output noise and ripple.

To realize full speed capability of the device, all 3 power supply leads should be bypassed no further than 1/2 inch from the device, with 1 μF tantalum electrolytic capacitors in parallel with 0.01 μF ceramic disc capacitors.

VOLTAGE MODE OPERATION

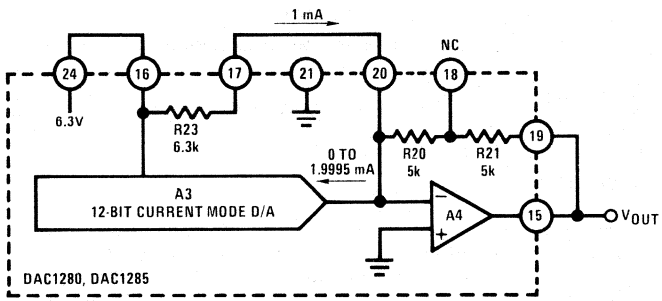
The DAC1280 and DAC1285 D/A's provide internal scaling resistors which permit a wide range of bipolar and unipolar output configurations. Bipolar output formats of ±2.5V, ±5V, ±10V and unipolar formats of 0 to 5V and 0 to 10V are possible using resistor strap options included within the device. Table I and *Figures 1–3* summarize the proper pin connections required for these formats.

Functional Description (Continued)

TABLE I. Output Voltage/Current Ranges for DAC1280 Series

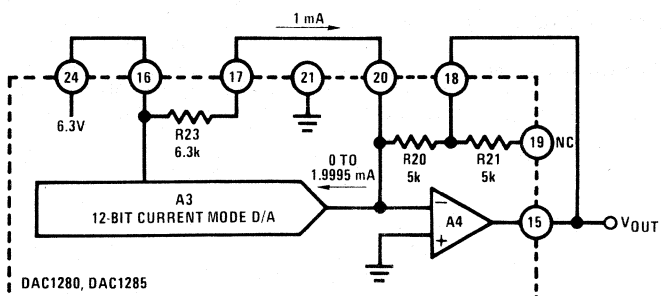
OUTPUT VOLTAGE RANGE	DIGITAL INPUT CODE	CONNECT PIN 15 TO	CONNECT PIN 16 TO	CONNECT PIN 17 TO	CONNECT PIN 19 TO
±10V	Complementary Offset Binary	19	24	20	15
±5V	Complementary Offset Binary	18	24	20	NC
±2.5V	Complementary Offset Binary	18	24	20	20
+10V	Complementary Binary	18	24	21*	NC
+5V	Complementary Binary	18	24	21*	20
±1 mA	Complementary Offset Binary	NC	24	20	NC
−2 mA	Complementary Binary	NC	24	21*	NC

*Optional, no connection necessary



V_{OUT} = (0 to 1.9995 mA) (R20 + R21) − (6.3V/R23)(R21 + R22)
= (0 to 1.9995 mA) (10k) − (1 mA) (10k)
= −10V to +9.995V
1 LSB = 20V/4096 = 4.88 mV

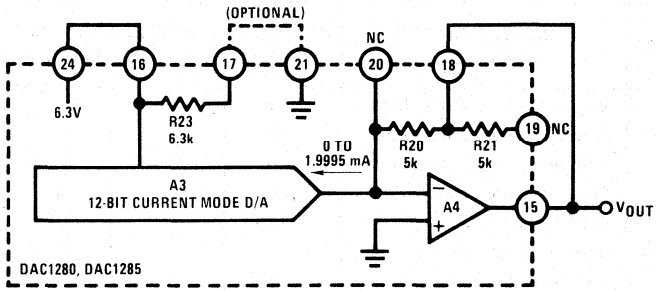
FIGURE 1. ±10V Bipolar Operation



V_{OUT} = (0 to 1.9995 mA) (R20) − (R20/R23)(6.3V)
= (0 to 1.9995 mA) (5k) − (5k/6.3k) (6.3V)
= −5V to 4.9975V
1 LSB = 10V/4096 = 2.44 mV

FIGURE 2. ±5V Bipolar Operation

Functional Description (Continued)



V_{OUT} = (0 to 1.9995 mA) (R20)
= (0 to 1.9995 mA) (5k)
= 0 to 9.9976V
1 LSB = 2.44 mV

FIGURE 3. 10V Unipolar Operation

CURRENT MODE OPERATION

Current mode applications which make use of an external op amp, comparator, or a resistive load are possible with the DAC1280 series using pin 20. When an external op amp is used, the internal scaling resistors should be utilized to minimize full-scale drift. Configurations shown in Table I apply directly. *Figure 4* shows one application using an external fast operational amplifier.

Current mode operation into a resistive load should also utilize the internally supplied resistors. A compliance restriction of ±2.5V at pin 20 is required for operation in the current output mode.

OFFSET AND FULL-SCALE ADJUST

The DAC1280 series may be offset and full-scale adjusted using the circuit shown in *Figure 5*. Offset voltage should be adjusted first. A logic "1" ($\geq$ 2V) should be applied to all logic inputs. In bipolar mode, the offset is adjusted to equal minus full-scale. In unipolar mode, the offset is adjusted to read 0V at the output. Full-scale is then adjusted by applying a logic "0" ($\leq$ 0.8V) to all inputs for operation. The range of R1 and R2 shown in *Figure 5* is approximately ±0.2% of full-scale for the values shown.

A 30 second "warm-up" period should be allowed (after power turn-on) before making the above adjustments.

LOGIC INPUT CODING

The logic inputs to the DAC1280 series are complementary; i.e., a given bit is turned ON by an active low input. Table II summarizes input status for unipolar and bipolar codes.

Functional Description (Continued)

REFERENCE SUPPLY

The DAC1280 series is supplied with an internal 6.3V reference supply voltage (pin 24). In order to obtain the specified performance, pin 24 should be connected to the Reference Voltage Input (pin 16). Since the reference is buffered by an op amp, the reference may be used externally at currents up to 5 mA. The reference output is short-circuit limited to a nominal 20 mA. An external reference voltage may be used with the DAC1280 series. Voltage values between 5V and 11V will work satisfactorily. Full-scale current may be predicted by:

$$I_{FULL\text{-}SCALE} = (V_{REF})\ (0.317381\ mA/V)$$

LOGIC INPUT COMPATIBILITY

The design of the current mode switches in the DAC1280 series give the device true TTL compatibility. It is TTL compatible over the entire operating temperature range and is independent of the reference voltage and V_{CC}. Furthermore, since the input breakdown ratings are in excess of 18V, the DAC1280 series may be driven directly from high (or low) voltage CMOS.

TABLE II

CODE TYPE	INPUT CODE (Note 7) MSB											LSB	OUTPUT STATE	UNIPOLAR OUTPUT RANGES 0 to 10V	0 to 5V	0–2 mA 0–1.25 mA
Unipolar	0	0	0	0	0	0	0	0	0	0	0	0	Full-Scale	9.9976V	4.9988V	−1.9995 mA
Complementary	1	1	1	1	1	1	1	1	1	1	1	0	1 LSB ON	0.0024V	0.0012V	0.0005 mA
Binary	1	1	1	1	1	1	1	1	1	1	1	1	Zero-Scale	0.0000V	0.0000V	0.0000 mA

CODE TYPE	INPUT CODE (Note 7) MSB											LSB	OUTPUT STATE	BIPOLAR OUTPUT VOLTAGE RANGES ±10V	±5V	±2.5V	±1 mA
Bipolar	0	0	0	0	0	0	0	0	0	0	0	0	Full-Scale	9.9951V	4.9976V	2.4988V	−0.9995 mA
Complementary	0	1	1	1	1	1	1	1	1	1	1	1	Half-Scale	0.0000V	0.0000V	0.0000V	0.0000 mA
Binary	1	1	1	1	1	1	1	1	1	1	1	0	1 LSB ON	−9.9951V	−4.9976V	−2.4988V	0.9995 mA
	1	1	1	1	1	1	1	1	1	1	1	1	Zero-Scale	−10.0000V	−5.0000V	−2.5000V	1.0000 mA

Note 7: Logic input sense is such that an active low ($V_{IN} \leq 0.8V$) turns a given bit ON and is represented as a logic "0" in the table.

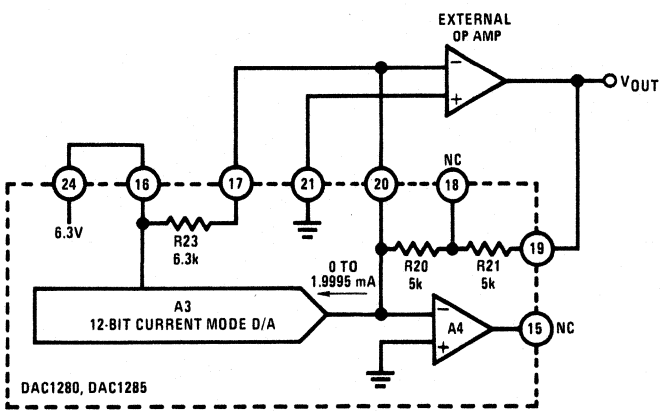


FIGURE 4. ±10V Bipolar Operation with External Operational Amplifier

Functional Description (Continued)

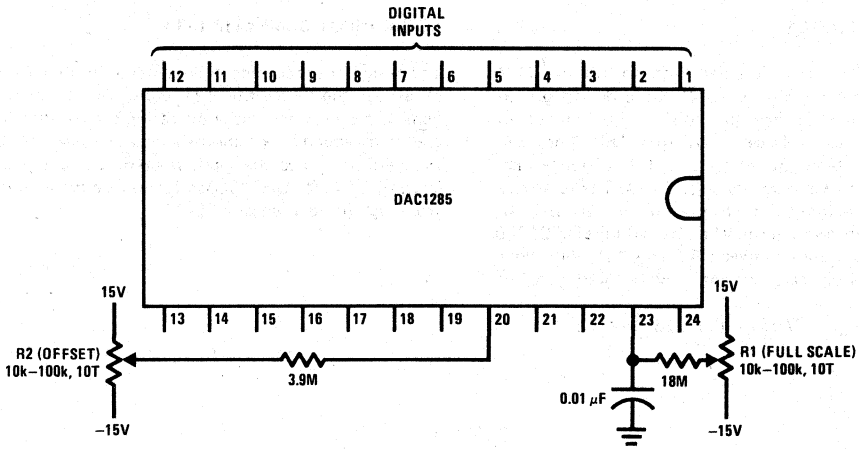


FIGURE 5. Full-Scale and Adjustment Circuits

Ordering Information

PART NUMBER BINARY	25°C LINEARITY	PACKAGE	TEMPERATURE RANGE
DAC1285HD	0.01%	DIP	−55°C to +125°C
DAC1285HCD	0.01%	DIP	−25°C to +85°C
DAC1280HCD	0.025%	DIP	−25°C to +85°C

*See NS Package D24D

National Semiconductor

LM1508/LM1408 8-Bit D/A Converter

General Description

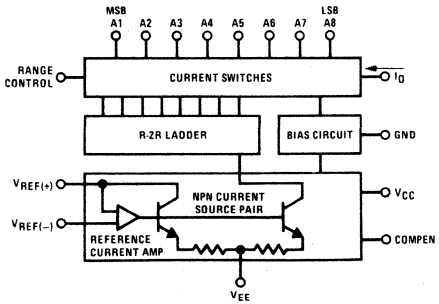
The LM1508/LM1408 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the LM1508/LM1408 are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The LM1508/LM1408 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet. For more information, see DAC0808 data sheet.

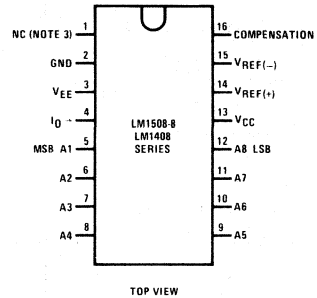
Features

- Relative accuracy: ±0.19% error maximum LM1508-8 and LM1408-8
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Typical Application

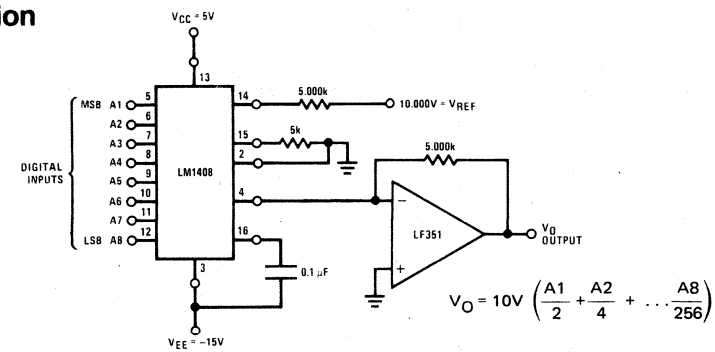


FIGURE 1. ±10V Output Digital to Analog Converter

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS*		
		HERMETIC PACKAGE (D16C)	HERMETIC PACKAGE (J16A)	PLASTIC PACKAGE (N16A)
8-Bit	$-55°C \leq T_A \leq +125°C$	LM1508D-8	LM1508J-8	
8-Bit	$0°C \leq T_A \leq +75°C$		LM1408J-8	LM1408N-8
7-Bit	$0°C \leq T_A \leq +75°C$		LM1408J-7	LM1408N-7
6-Bit	$0°C \leq T_A \leq +75°C$		LM1408J-6	LM1408N-6

*Note. Devices may be ordered by using either order number.

Absolute Maximum Ratings

Power Supply Voltage	
V_{CC}	5.5 V_{DC}
V_{EE}	−16.5 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Package Limitation)	
Cavity Package	1000 mW
Derate above T_A = 25°C	6.7 mW/°C
Operating Temperature Range	
LM1508-8	−55°C ≤ T_A ≤ +125°C
LM1408-8 Series	0 ≤ T_A ≤ +75°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, LM1508-8: T_A = −55°C to +125°C; LM1408-8, LM1408-7, LM1408-6, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
E_r	Relative Accuracy (Error Relative to Full Scale I_O)					%
	LM1508-8				±0.19	%
	LM1408-8					
	LM1408-7, (Note 1)				±0.39	%
	LM1408-6, (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	T_A = 25°C (Note 2)		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels					
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current					
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current			−1	−3	μA
	Output Current Range					
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω	1.9	1.99	2.1	mA
	Output Current, All Bits Low			0	4	μA
	Output Voltage Compliance	E_r ≤ 0.19%, T_A = 25°C				
	Pin 1 Grounded,				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}
SRI_{REF}	Reference Current Slew Rate			8		mA/μs
	Output Current Power Supply Sensitivity	−5V ≤ V_{EE} ≤ −16.5V		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)					
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

Section 9

Functional Blocks

Section Contents

National Semiconductor

LH0091 True RMS to DC Converter

General Description

The LH0091, rms to dc converter, generates a dc output equal to the rms value of any input per the transfer function:

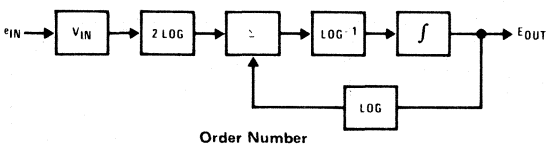
$$E_{OUT(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2\,(t)\,dt}$$

The device provides rms conversion to an accuracy of 0.1% of reading using the external trim procedure. It is possible to trim for maximum accuracy (0.5 mV ±0.05% typ) for decade ranges i.e., 10 mV → 100 mV, 0.7V → 7V, etc.

Features

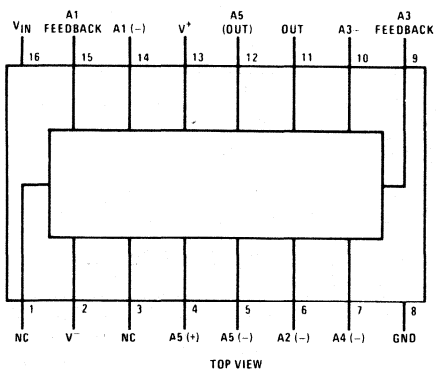
- Low cost
- True rms conversion
- 0.5% of reading accuracy untrimmed
- 0.05% of reading accuracy with external trim
- Minimum component count
- Input voltage to ±15V peak for V_S = ±15V
- Uncommitted amplifier for filtering, gain, or high crest factor configuration
- Military or commercial temperature range.

Block and Connection Diagrams



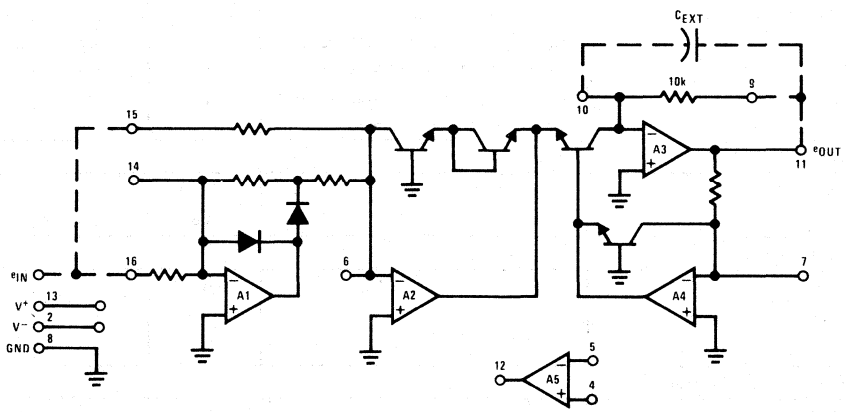
Order Number
LH0091D
LH0091CD
See Package D16D

Dual-In-Line Package



TOP VIEW

Simplified Schematic



Note: Dotted lines denote external connections.

Absolute Maximum Ratings

Supply Voltage		±22V
Input Voltage		±15V peak
Output Short Circuit Duration		Continuous
Operating Temperature Range	T_{MIN}	T_{MAX}
LH0091	−55°C	125°C
LH0091C	−25°C	85°C
Storage Temperature Range		
LH0091		−65°C to +150°C
LH0091C		−25°C to +85°C
Lead Temperature (Soldering, 10 seconds)		300°C

Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

Transfer Function = $E_{O(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2\,(t)\,dt}$

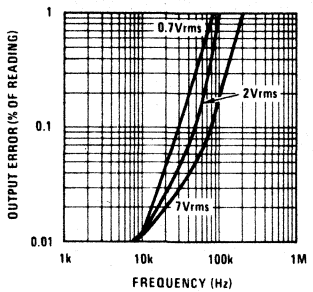
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (See Definition of Terms)					
Total Unadjusted Error	50 mVrms ≤ V_{IN} ≤ 7Vrms *(Figure 1)*		20, ±0.5	40, ±1.0	mV, %
Total Adjusted Error	50 mVrms ≤ V_{IN} ≤ 7Vrms *(Figure 3)*		0.5, ±0.05	1, ±0.2	mV, %
Total Unadjusted Error vs Temperature	−25°C ≤ T_A ≤ +70°C		0.25, ±0.02%		mV, %/°C
Total Unadjusted Error vs Supply Voltage			1		mV/V
AC PERFORMANCE					
Frequency for Specified Adjusted Error	Input = 7Vrms, Sinewave *(Figure 3)*	30	70		kHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		40		kHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		20		kHz
Frequency for 1% Additional Error	Input = 7Vrms, Sinewave *(Figure 3)*	100	200		kHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		75		kHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		50		kHz
Bandwidth (3 dB)	Input = 7Vrms, Sinewave *(Figure 3)*		2		MHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		1.5		MHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		0.8		MHz
Crest Factor	Rated Adjusted Accuracy Using the High Crest Factor Circuit *(Figure 5)*	5	10		
INPUT CHARACTERISTICS					
Input Voltage Range	For Rated Performance	±0.05		±11	Vpeak
Input Impedance		4.5	5		kΩ
OUTPUT CHARACTERISTICS					
Rated Output Voltage	$R_L \geq 2.5\,k\Omega$	10			V
Output Short Circuit Current			22		mA
Output Impedance			1		Ω
POWER SUPPLY REQUIREMENTS					
Operating Range		±5		±20	V
Quiescent Current	$V_S = \pm 15V$		14	18	mA

Op Amp Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified

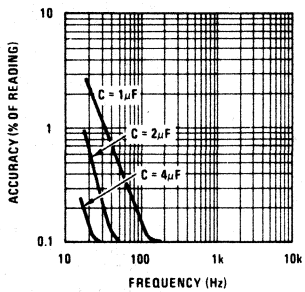
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	10	mV
I_{OS}	Input Offset Current			4.0	200	nA
I_B	Input Bias Current			30	500	nA
R_{IN}	Input Resistance			2.5		MΩ
A_{OL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	15	160		V/mV
V_O	Output Voltage Swing	$R_L = 10\ k\Omega$	±10	±13		V
V_I	Input Voltage Range		±10			V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$		90		dB
PSRR	Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		96		dB
I_{SC}	Output Short-Circuit Current			25		mA
S_r	Slew Rate (Unity Gain)			0.5		V/μs
BW	Small Signal Bandwidth			1.0		MHz

Typical Performance Characteristics

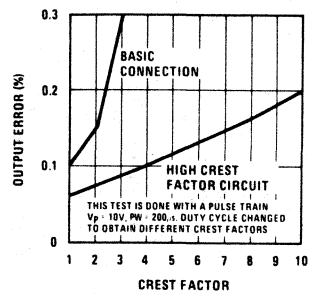
Error vs Frequency



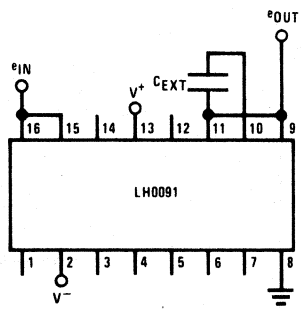
Error vs Frequency



Error vs Crest Factor



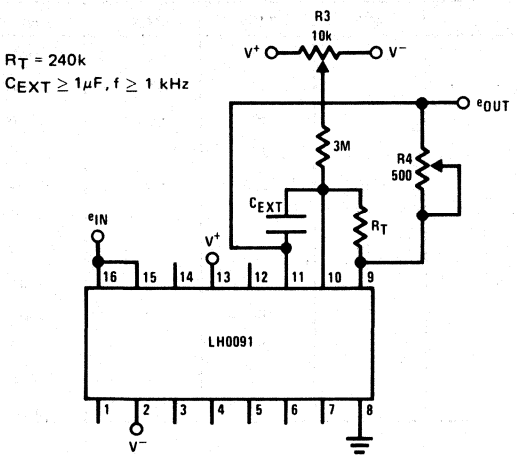
Typical Applications (All applications require power supply by-pass capacitors.)



$C_{EXT} \geq 1\mu F$; frequency ≥ 1 kHz

FIGURE 1. LH0091 Basic Connection (No Trim)

Typical Applications (Continued)

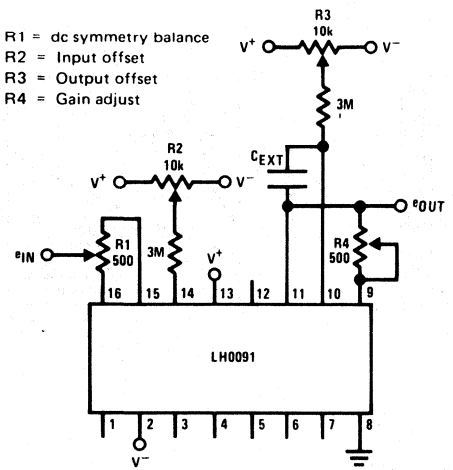


Note. The easy trim procedure is used for ac coupled input signals. It involves two trims and can achieve accuracies of 2 mV offset ±0.1% reading.

Procedure:

1. Apply 100 mV rms (sine wave) to input, adjust R3 until the output reads 100 mV_{DC}.
2. Apply 5 V_{rms} (sine wave) to input, adjust R4 until the output reads 5 V_{DC}.
3. Repeat steps 1 and 2 until the desired initial accuracy is achieved.

FIGURE 2. LH0091 "Easy Trim" (For ac Inputs Only)

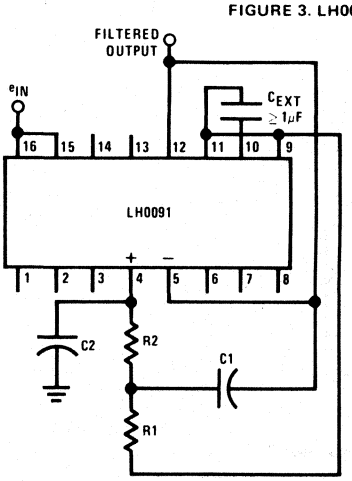


Note. This procedure will give accuracies of 0.5 mV offset ±0.05% reading for inputs from 0.05V peak to 10V peak.

Procedure:

1. Apply 50 mV_{DC} to the input. Read and record the output.
2. Apply −50 mV_{DC} to the input. Use R2 to adjust for an output of the same magnitude as in step 1.
3. Apply 50 mV to the input. Use R3 to adjust the output for 50 mV.
4. Apply −50 mV to input. Use R2 to adjust the output for 50 mV.
5. Apply ±10V alternately to the input. Adjust R1 until the output readings for both polarities are equal (not necessary that they be exactly 10V).
6. Apply 10V to the input. Use R4 to adjust for 10V at the output.
7. Repeat this procedure to obtain the desired accuracy.

FIGURE 3. LH0091 Standard dc Trim Procedure



Note. The additional op amp in the LH0091 may be used as a low pass filter as shown in *Figure 4*.

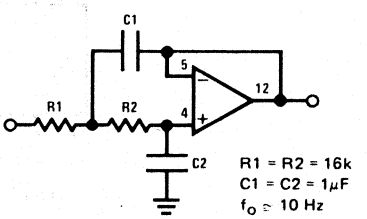
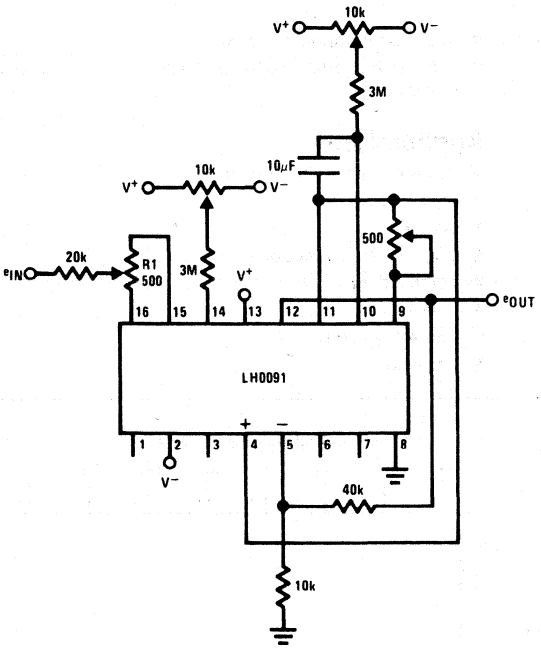


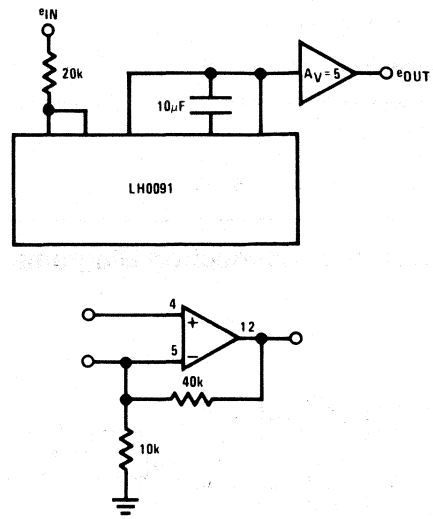
FIGURE 4. Output Filter Connection Using the Internal Op Amp

Typical Applications (Continued)



Note. When converting signals with a crest factor ≥ 2, the LH0091 should be connected as shown. Note that this circuit utilizes a 20k resistor to drop the input current by a factor of five. The frequency response will correspond to a voltage which is 1/5 e_{IN}.

Note that the extra op amp in the LH0091 may be used to build a gain of 5 amplifier to restore the output voltage.



Note. Response time of the dc output voltage is dominated by the RC time constant consisting of the total resistance between pins 9 and 10 and the external capacitor, C_{EX}.

FIGURE 5. High Crest Factor Circuit

Definition of Terms

True rms to dc Converter: A device which converts any signal (ac, dc, ac + dc) to the dc equivalent of the rms value.

Error: is the amount by which the actual output differs from the theoretical value. Error is defined as a sum of a fixed term and a percent of reading term. The fixed term remains constant, regardless of input while the percent of reading term varies with the input.

Total Unadjusted Error: The total error of the device without any external adjustments.

Bandwidth: The frequency at which the output dc voltage drops to 0.707 of the dc value at low frequency.

Frequency for Specified Error: The error at low frequency is governed by the size of the external averaging capacitor. At high frequencies, error is dependent on the frequency response of the internal circuitry. The frequency for specified error is the maximum input frequency for which the output will be within the specified error band (i.e., frequency for 1% error means the input frequency must be less than 200 kHz to maintain an output with an error of less than 1% of the initial reading.

Crest Factor: is the peak value of a waveform divided by the rms value of the same waveform. For high crest factor signals, the performance of the LH0091 can be improved by using the high crest factor connection.

National Semiconductor

LH0094 Multifunction Converter

General Description

The LH0094 multifunction converter generates an output voltage per the transfer function:

$$E_o = V_Y \left(\frac{V_Z}{V_X}\right)^m, \quad 0.1 \leq m \leq 10, \text{ m continuously adjustable}$$

m is set by 2 resistors.

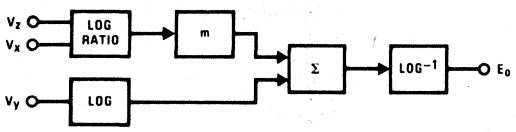
Features

- Low cost
- Versatile
- High accuracy—0.05%
- Wide supply range—±5V to ±22V
- Minimum component count
- Internal matched resistor pair for setting m = 2 and m = 0.5

Applications

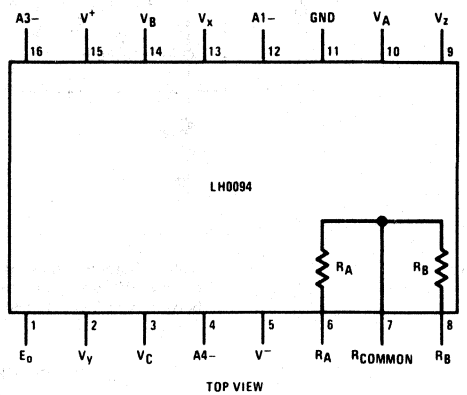
- Precision divider, multiplier
- Square root
- Square
- Trigonometric function generator
- Companding
- Linearization
- Control systems
- Log amp

Block and Connection Diagrams



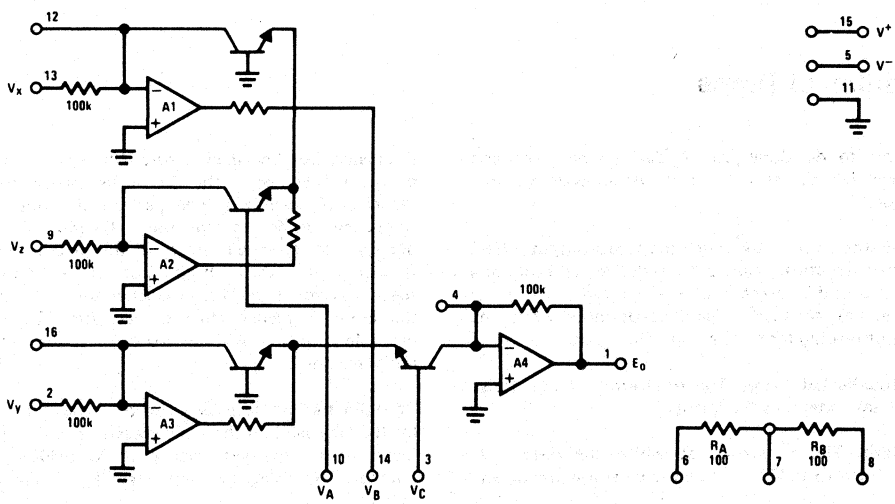
Order Number
LH0094D
LH0094CD
See Package D16D

Dual-In-Line Package



TOP VIEW

Simplified Schematic



Absolute Maximum Ratings

Supply Voltage	±22V
Input Voltage	±22V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LH0094CD	−25°C to +85°C
LH0094D	−55°C to +125°C
Storage Temperature Range	
LH0094D	−65°C to +150°C
LH0094CD	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified. Transfer function: $E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$; $0.1 \leq m \leq 10$; $0V \leq V_X, V_Y, V_Z \leq 10V$

PARAMETER	CONDITIONS	LH0094			LH0094C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Multiply	$E_O = \frac{V_Z V_Y}{10}$ $(0.03 \leq V_Y \leq 10V; 0.01 \leq V_Z \leq 10V)$							% F.S.
Untrimmed	*(Figure 2)*		0.25	0.45		0.45	0.9	(10V)
External Trim	*(Figure 3)*		0.10			0.1		% F.S.
	vs Temperature		0.2			0.2		mV/°C
Divide	$E_O = 10 V_Z/V_X$							
Untrimmed	*(Figure 4)*, $(0.5 \leq V_X \leq 10; 0.01 \leq V_Z \leq 10)$		0.25	0.45		0.45	0.9	% F.S.
External Trim	*(Figure 5)*, $(0.1 \leq V_X \leq 10; 0.01 \leq V_Z \leq 10)$		0.10			0.1		% F.S.
	vs Temperature		0.2			0.2		mV/°C
Sq. Root	$E_O = 10\sqrt{V_Z/10}$							
Untrimmed	*(Figure 8)*, $(0.03 \leq V_Z \leq 10)$		0.25	0.45		0.45	0.9	% F.S.
External Trim	*(Figure 9)*, $(0.01 \leq V_Z \leq 10)$		0.15			0.15		% F.S.
Square	$E_O = 10 (V_Z/10)^2$ $(0.1 \leq V_Z \leq 10)$							
Untrimmed	*(Figure 6)*		0.5	1.0		1.0	2.0	% F.S.
External Trim	*(Figure 7)*		0.15			0.15		% F.S.
Low Level Sq. Root	$E_O = \sqrt{10 V_Z}$; $5 mV \leq V_Z \leq 10V$ *(Figure 10)*		0.05			0.05		% F.S.
Exponential Circuits	**m = 0.2** $E_O = 10 (V_Z/10)^2$ *(Figure 11)*, $(0.1 \leq V_Z \leq 10)$		0.05			0.08		% F.S.
	m = 5 $E_O = 10 (V_Z/10)^5$ *(Figure 11)*, $(1 \leq V_Z \leq 10)$		0.05			0.08		% F.S.
OUTPUT OFFSET								
	$V_X = 10.0V$, $V_Y = V_Z = 0.0$		2	5		5	10	mV
AC CHARACTERISTICS								
3 dB BANDWIDTH	m = 1.0 $V_X = V_Z = 10.0V$ $V_Y = 0.1$ Vrms		10			10		kHz
NOISE	10 Hz to 1 kHz m = 1, $V_Y = V_Z = 0.0V$							
	$V_X = 10V$		100			100		μVrms
	$V_X = 0.1V$		300			300		μVrms
EXPONENTS								
m		0.2 to 5	0.1 to 10		0.2 to 5	0.1 to 10		
INPUT CHARACTERISTICS								
Input Voltage	(For Rated Performance)	0		10	0		10	V
Input Impedance	(All Inputs)	98	100		98	100		kΩ
OUTPUT CHARACTERISTICS								
Output Swing	$(R_L \geq 10k)$	10	12		10	12		V
Output Impedance			1			1		Ω
Supply Current	$(V_S = \pm 15V)$, Note 1		3	5		3	5	mA

Applications Information

GENERAL INFORMATION

Power supply bypass capacitors (0.1 μF) are recommended for all applications.

The LH0094 series is designed for positive input signals only. However, negative input up to the supply voltage will not damage the device.

A clamp diode *(Figure 1)* is recommended for those applications in which the inputs may be subjected to open circuit or negative input signals.

For basic applications (multiply, divide, square, square root) it is possible to use the device without any external adjustments or components. Two matched resistors are provided internally to set m for square or square root.

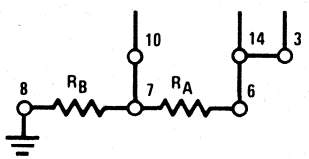
When using external resistors to set m, such resistors should be as close to the device as possible.

SELECTION OF RESISTORS TO SET m

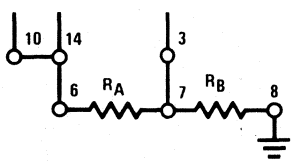
Internal Matched Resistors

R_A and R_B are matched internal resistors. They are 100Ω ±10%, but matched to 0.1%.

(a) m = 2*



(b) m = 0.5*

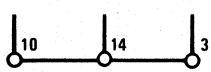


*No external resistors required, strap as indicated

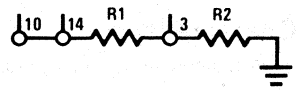
External Resistors

The exponent is set by 2 external resistors or it may be continuously varied by a single trim pot. (R1 + R2 $\leq$ 500Ω.

(a) m = 1

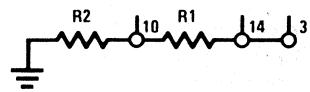


(b) m < 1



$$m = \frac{R2}{R1 + R2} \qquad R1 + R2 \approx 200\Omega$$

(c) m > 1



$$m = \frac{R1 + R2}{R2}$$

ACCURACY (ERROR)

The accuracy of the LH0094 is specified for both externally adjusted and unadjusted cases.

Although it is customary to specify the errors in percent of full-scale (10V), it is seen from the typical performance curves that the actual errors are in percent of reading. Thus, the specified errors are overly conservative for small input voltages. An example of this is the LH0094 used in the multiplication mode. The specified typical error is 0.25% of full-scale (25 mV). As seen from the curve, the unadjusted error is $\approx$ 25 mV at 10V input, but the error is less than 10 mV for inputs up to 1V. Note also that if either the multiplicand or the multiplier is at less than 10V, (5V for example) the unadjusted error is less. Thus, the errors specified are at full-scale—the worst case.

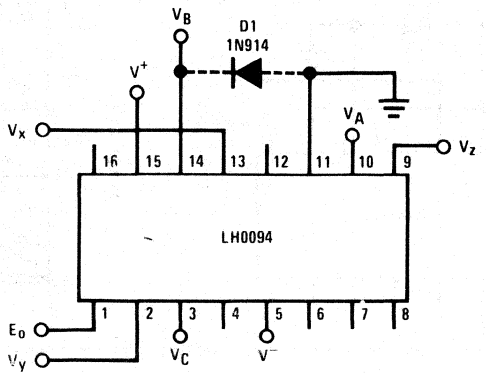
The LH0094 is designed such that the user is able to externally adjust the gain and offset of the device—thus trim out all of the errors of conversion. In most applications, the gain adjustment is the only external trim needed for super accuracy—except in division mode, where a denominator offset adjust is needed for small denominator voltages.

EXPONENTS

The LH0094 is capable of performing roots to 0.1 and powers up to 10. However, care should be taken when applying these exponents—otherwise, results may be misinterpreted. For example, consider the 1/10th power of a number: i.e., 0.001 raised to 0.1 power is 0.5011; 0.1 raised to the 0.1 power is 0.7943; and 10 raised to the 0.1 power is 1.2589. Thus, it is seen that while the input has changed 4 decades, the output has only changed a little more than a factor of 2. It is also seen that with as little as 1 mV of offset, the output will also be greater than zero with zero input.

Applications Information (Continued)

1. CLAMP DIODE CONNECTION



$$E_o = V_y \left(\frac{V_z}{V_x}\right)^m$$

$0.1 \leq m \leq 10$

Note. This clamp diode connection is recommended for those applications in which the inputs may be subject to open circuit or negative signals.

FIGURE 1. Clamp Diode Connection

2. MULTIPLY

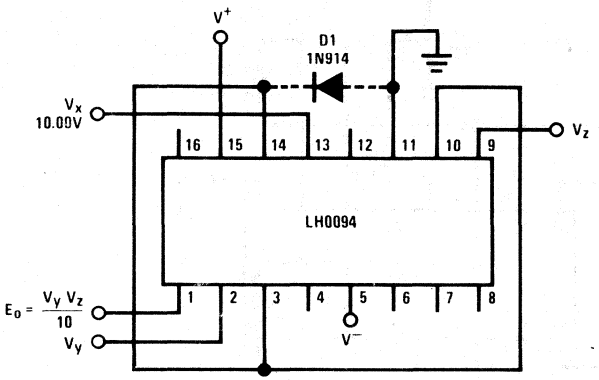


FIGURE 2a. LH0094 Used to Multiply (No External Adjustment)

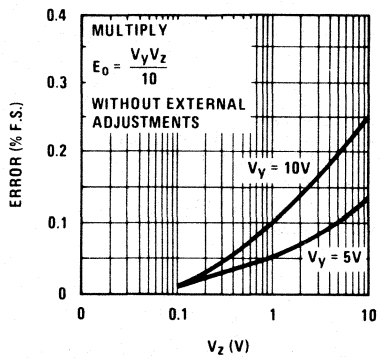


FIGURE 2b. Typical Performance of LH0094 in Multiply Mode Without External Adjustment

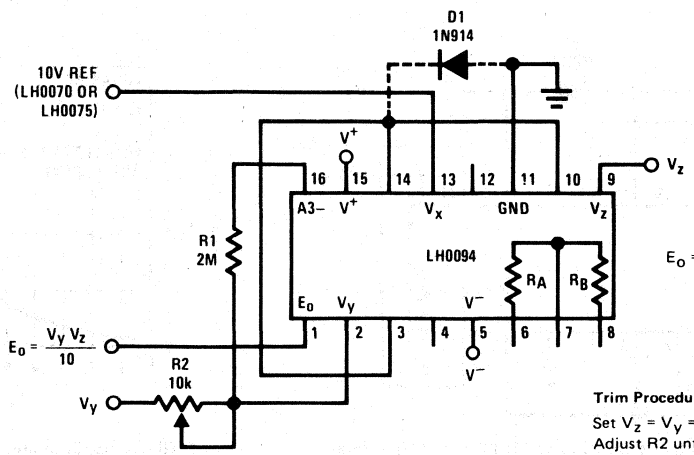


FIGURE 3. Precision Multiplier (0.02% Typ) with 1 External Adjustment

Applications Information (Continued)

3. DIVIDE

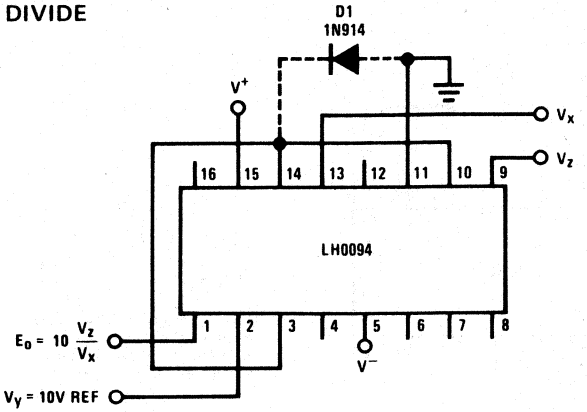


FIGURE 4a. LH0094 Used to Divide (No External Adjustment)

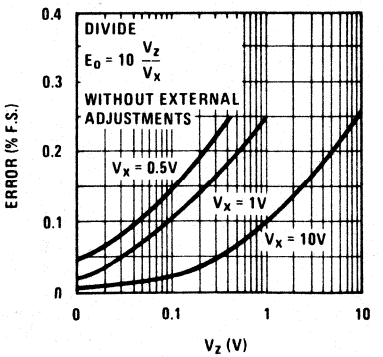


FIGURE 4b. Typical Performance, Divide Mode, Without External Adjustments

Trim Procedures

Apply 10V to V_y, 0.1V to V_x and V_z.
Adjust R3 until E_o = 10.000V.

Apply 10.000V to all inputs.
Adjust R2 until E_o = 10.000V

Repeat procedure.

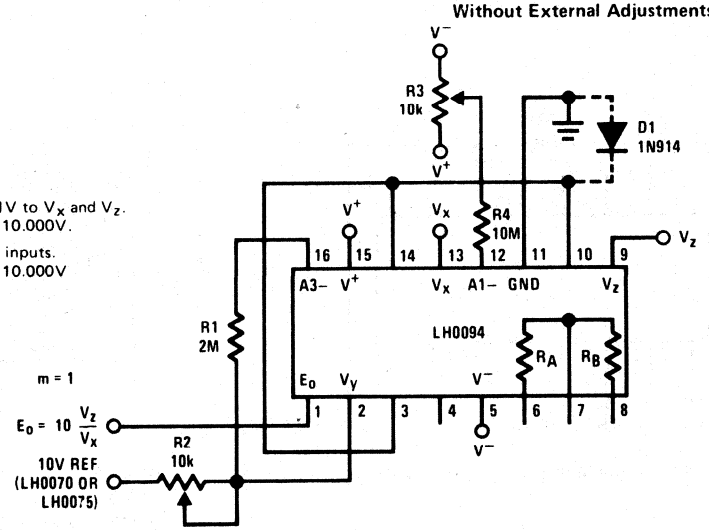


FIGURE 5. Precision Divider (0.05% Typ)

4. SQUARE

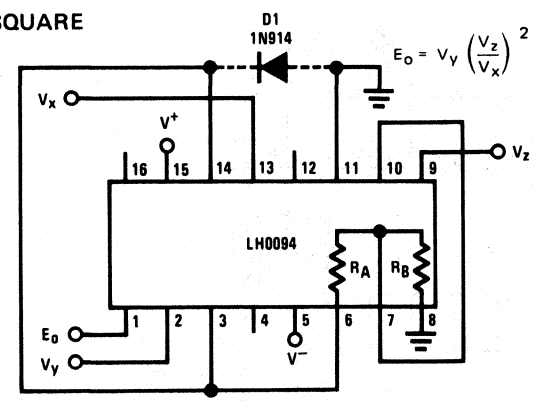


FIGURE 6a. Basic Connection of LH0094 (m = 2) without External Adjustment Using Internal Resistors to Set m

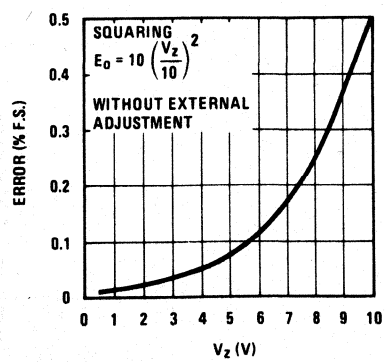


FIGURE 6b. Squaring Mode without External Adjustment

Applications Information (Continued)

4. SQUARE (Continued)

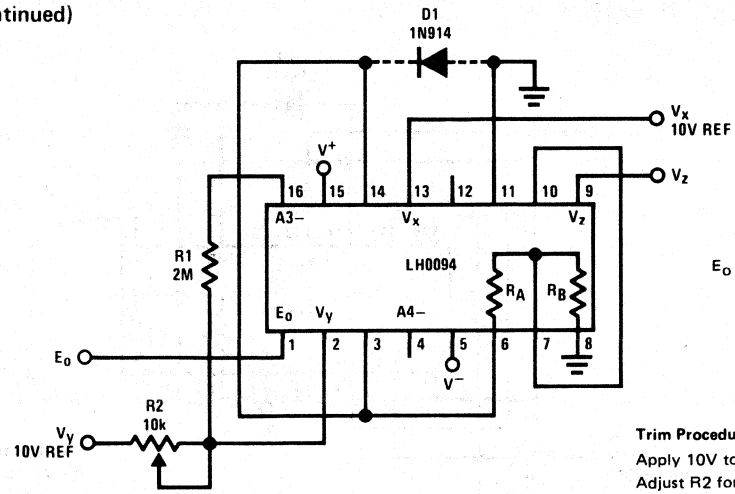


FIGURE 7. Precision Squaring Circuit (0.15% Typ)

5. SQUARE ROOT

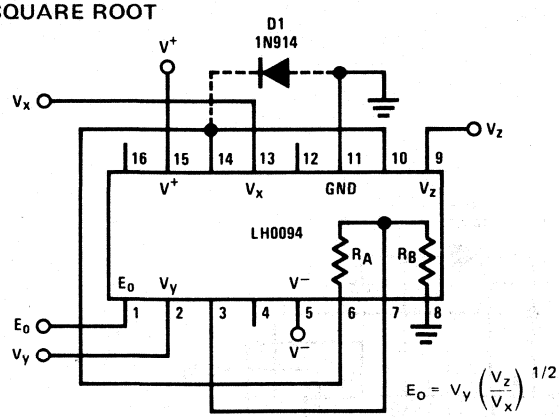


FIGURE 8a. Basic Connection of LH0094 (m = 0.5) without External Adjustment Using Internal Resistors to Set m

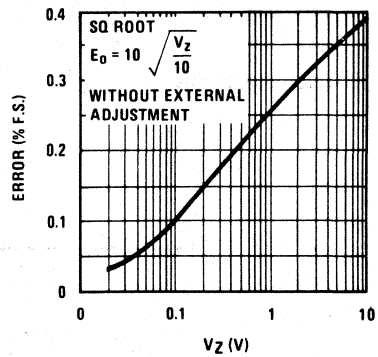


FIGURE 8b. Typical Performance Curve Square Root, No External Adjustment

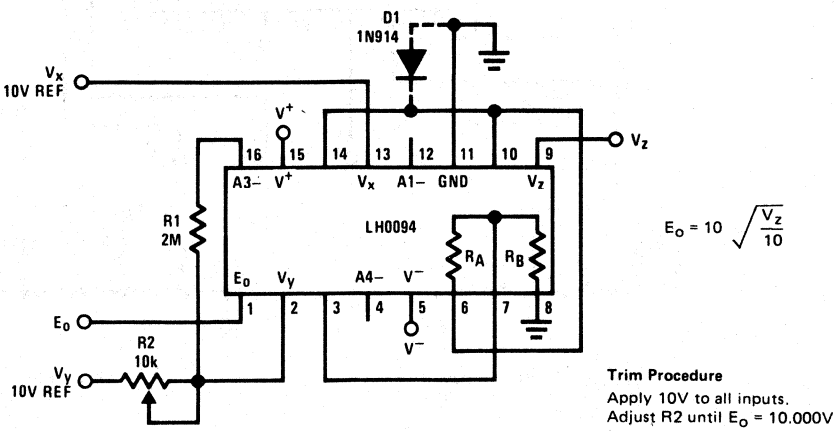


FIGURE 9. Precision Square Rooter (0.15% Typ)

Applications Information (Continued)

6. LOW LEVEL SQUARE ROOT

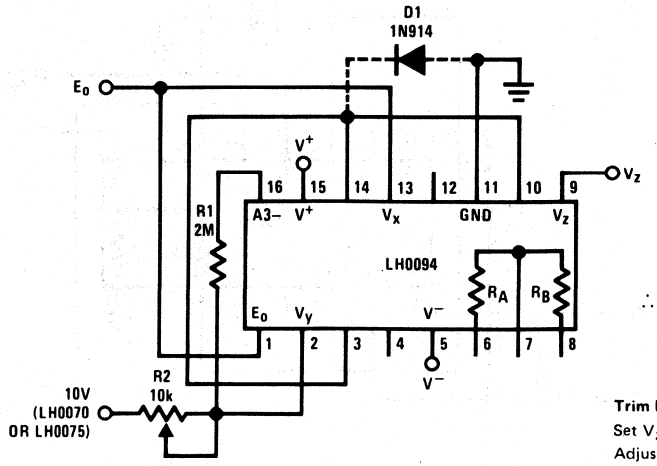
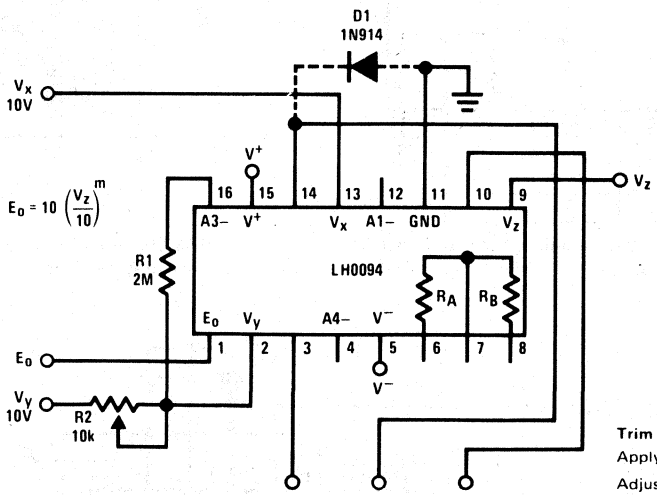


FIGURE 10. 3-Decade Precision Square Root Circuit Using the LH0094 with m = 1

Typical Applications

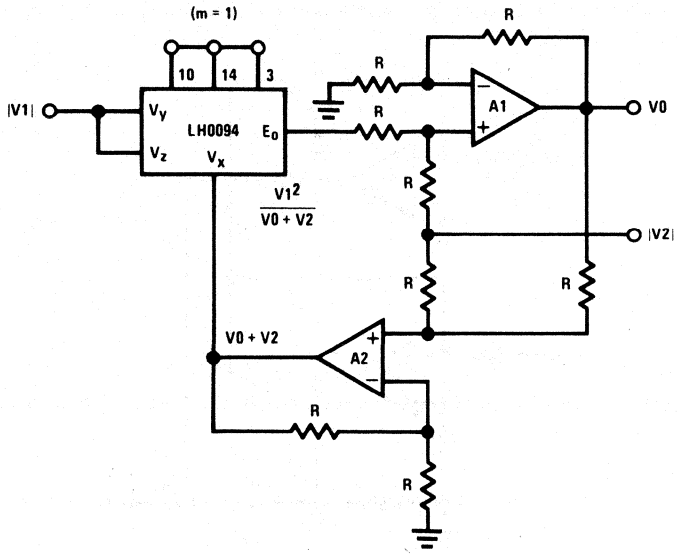


$m = \frac{R2}{R1 + R2}$; Choose R1 = 200Ω
$\therefore$ R2 = 50Ω

$m = \frac{R1 + R2}{R2}$; Choose R2 = 50Ω
$\therefore$ R1 = 200Ω

FIGURE 11. Precision Exponentiator (m = 0.2 to 5)

Typical Applications (Continued)



Note. The LH0094 may be used to generate a voltage equivalent to:

$$V0 = \sqrt{V1^2 + V2^2}$$

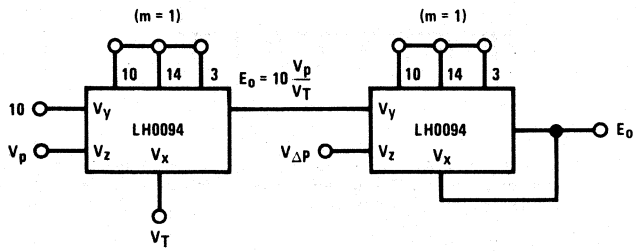
$$V0 = V2 + \frac{V1^2}{V0 + V2}$$

$$V0^2 + V0\,V2 = V2\,V0 + V2^2 + V1^2$$
$$V0^2 = V1^2 + V2^2$$

$$\therefore \quad V0 = \sqrt{V1^2 + V2^2} \qquad V1, V2\ 0 \rightarrow 10V$$

$R \approx 10k$
National Semiconductor resistor array RA08–10k is recommended

FIGURE 12. Vector Magnitude Function



Note. The LH0094 may be used in direct measurement of gas flow.

$$\text{Flow} = k\sqrt{\frac{P\Delta P}{T}}$$

$$E_o = 10\,\frac{V_P}{V_T} \times \frac{V_{\Delta P}}{E_o}$$

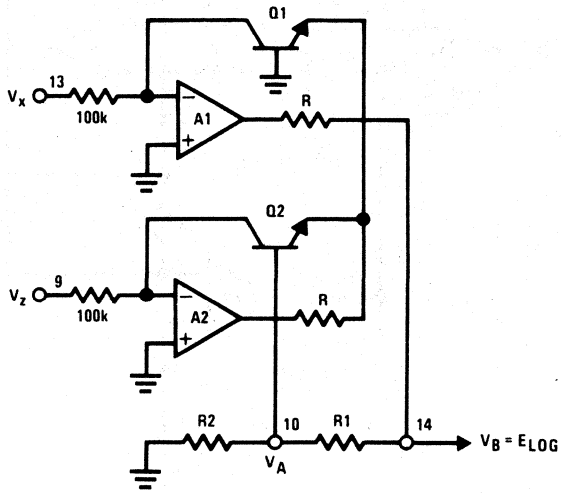
$$E_o^2 = 10\,\frac{V_P\,V_{\Delta P}}{V_T}$$

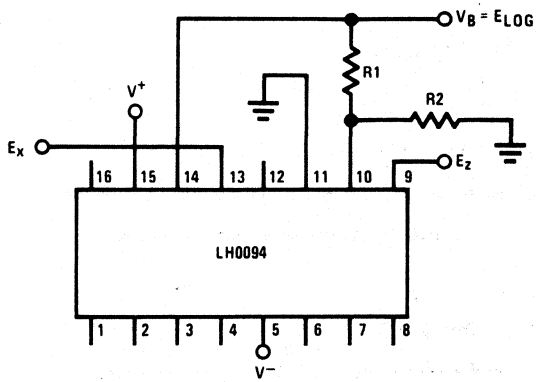
$$E_o = \sqrt{10\,\frac{V_P\,V_{\Delta P}}{V_T}}$$

P = Absolute pressure
T = Absolute temperature
ΔP = Pressure drop

FIGURE 13. Mass Gas Flow Circuit

Typical Applications (Continued)





Note. The LH0094 may also be used to generate the Log of a ratio of 2 voltages. The output is taken from pin 14 of the LH0094 for the Log application.

$$E_{LOG} = K1 \frac{KT}{q} \ln \frac{V_z}{V_x}$$

$$\text{where } K1 = \frac{R1 + R2}{R2}$$

$$\text{If } K1 = \frac{1}{KT/q \ln 10}$$

$$\text{then } E_{LOG} = \text{Log}_{10} \frac{V_z}{V_x}$$

$R1 = 15.9\ R2$
$R2 \approx 400\Omega$

R2 must be a thermistor with a tempco of $\approx 0.33\%/^{\circ}C$ to be compensated over temperature.

FIGURE 14. Log Amp Application

MM74C925, MM74C926, MM74C927, MM74C928 4-Digit Counters with Multiplexed 7-Segment Output Drivers

General Description

These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero, and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.

The MM74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The MM74C926 is like the MM74C925 except that it has a display select and a carry-out used for cascading counters. The carry-out signal goes high at 6000, goes back low at 0000.

The MM74C927 is like the MM74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The MM74C928 is like the MM74C926 except the most significant digit divides by 2 rather than 10 and the carry-out is an overflow indicator which is high at 2000, and it goes back low only when the counter is reset. Thus, this is a 3 1/2-digit counter.

Features

- Wide supply voltage range — 3V to 6V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} typ
- High segment sourcing current — 40 mA @ $V_{CC} - 1.6V$, $V_{CC} = 5V$
- Internal multiplexing circuitry

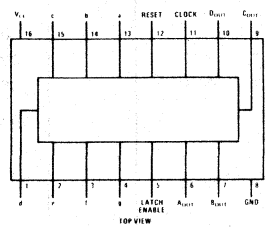
Design Considerations

Segment resistors are desirable to minimize power dissipation and chip heating. The DM75492 serves as a good digit driver when it is desired to drive bright displays. When using this driver with a 5V supply at room temperature, the display can be driven without segment resistors to full illumination. The user must use caution in this mode however, to prevent overheating of the device by using too high a supply voltage or by operating at high ambient temperatures.

The input protection circuitry consists of a series resistor, and a diode to ground. Thus input signals exceeding V_{CC} will not be clamped. This input signal should not be allowed to exceed 15V.

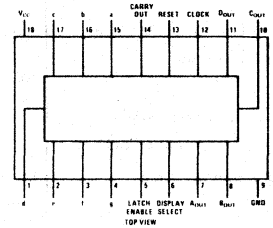
Connection Diagrams

Dual-In-Line Package



Order Number MM74C925N
See NS Package N16A

Dual-In-Line Package



Order Number MM74C926N, MM74C927N
or MM74C928N
See NS Package N18A

Functional Description

Reset — Asynchronous, active high

Display Select — High, displays output of counter
Low, displays output of latch

Latch Enable — High, flow through condition
Low, latch condition

Clock — Negative edge sensitive

Segment Output — Current sourcing with 80 mA @ $V_{OUT} = V_{CC} - 1.6V$ typical. Also, sink capability = 2 LTTL loads

Digit Output — Current sourcing with 1 mA @ $V_{OUT} = 1.75V$. Also, sink capability = 2 LTTL loads

Carry-out — 2 LTTL loads. See carry-out waveforms.

Absolute Maximum Ratings (Note 1)

Voltage at Any Output Pin	Gnd − 0.3V to V_{CC}+0.3V
Voltage at Any Input Pin	Gnd − 0.3V to +15V
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply at −40°C ≤ T_j ≤ +85°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-out and Digit Output Only)	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 μA			0.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.0V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.0V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5.0V, Outputs Open Circuit, V_{IN} = 0V or 5V		20	1000	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		V_{CC}−1.3		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C	V_{CC}−1.6	V_{CC}−1.2		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C	V_{CC}−2	V_{CC}−1.4		V
R_{ON}	Output Resistance (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		20		Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C		30	40	Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C		35	50	Ω
	Output Resistance (Segment Output) Temperature Coefficient			0.6	0.8	%/°C
I_{SOURCE}	Output Source Current (Digit Output)	V_{CC} = 4.75V, V_{OUT} = 1.75V, T_j = 150°C	−1	−2		mA
I_{SOURCE}	Output Source Current (Carry-out)	V_{CC} = 5V, V_{OUT} = 0V, T_j = 25°C	−1.75	−3.3		mA
I_{SINK}	Output Sink Current (All Outputs)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_j = 25°C	1.75	3.6		mA
θ_{jA}	Thermal Resistance	MM74C925 (Note 4)		75	100	°C/W
		MM74C926, MM74C927, MM74C928		70	90	°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

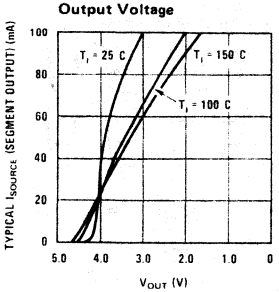
Note 4: θ_{jA} measured in free-air with device soldered into printed circuit board.

AC Electrical Characteristics $T_j = 25°C$, $C_L = 50$ pF, unless otherwise specified

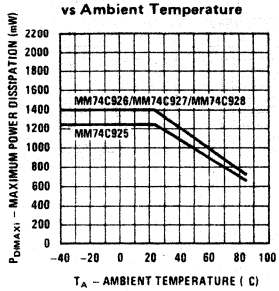
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency	V_{CC} = 5.0V,	$T_j = 25°C$	2	4		MHz
		Square Wave Clock	$T_j = 100°C$	1.5	3		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	V_{CC} = 5.0V				15	μs
t_{WR}	Reset Pulse Width	V_{CC} = 5.0V	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
t_{WLE}	Latch Enable Pulse Width	V_{CC} = 5.0V	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
$t_{SET(CK,LE)}$	Clock to Latch Enable Set-Up Time	V_{CC} = 5.0V	$T_j = 25°C$	2500	1250		ns
			$T_j = 100°C$	3200	1600		ns
t_{LR}	Latch Enable to Reset	V_{CC} = 5.0V	$T_j = 25°C$	0	−100		ns
	Wait Time		$T_j = 100°C$	0	−100		ns
$t_{SET(R,LE)}$	Reset to Latch Enable Set-Up Time	V_{CC} = 5.0V	$T_j = 25°C$	320	160		ns
			$T_j = 100°C$	400	200		ns
f_{MUX}	Multiplexing Output Frequency	V_{CC} = 5.0V			1000		Hz
C_{IN}	Input Capacitance	Any Input (Note 2)			5		pF

Typical Performance Characteristics

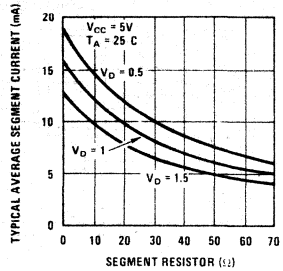
Typical Segment Current vs Output Voltage



Maximum Power Dissipation vs Ambient Temperature



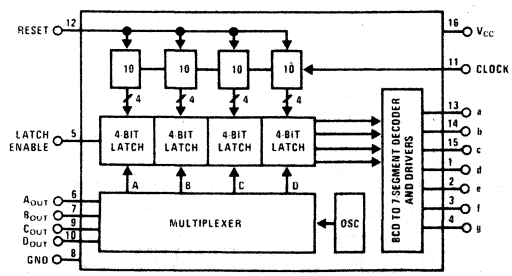
Typical Average Segment Current vs Segment Resistor Value



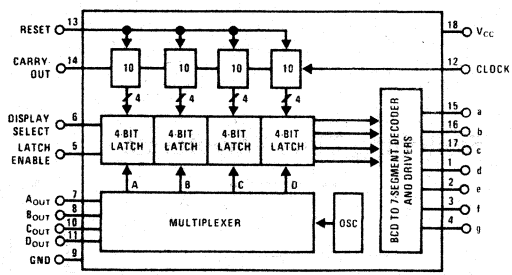
Note. V_D = Voltage across digit driver.

Logic and Block Diagrams

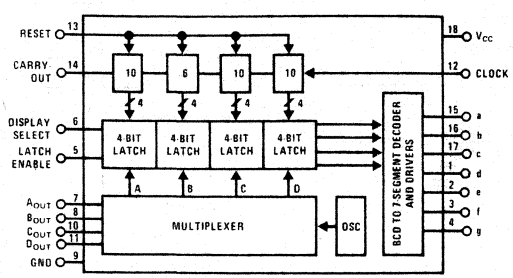
MM74C925



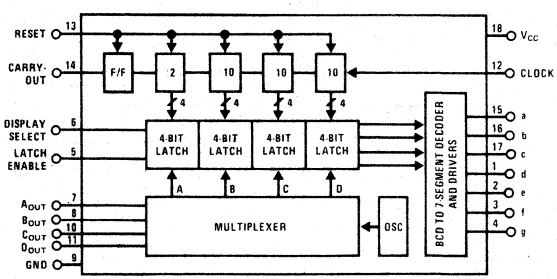
MM74C926



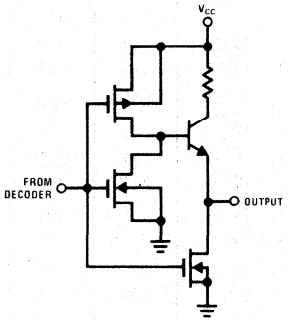
MM74C927



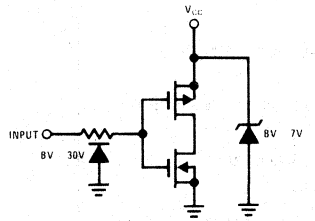
MM74C928



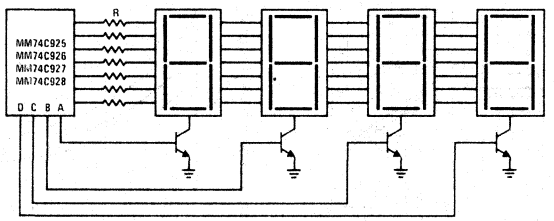
Segment Output Driver



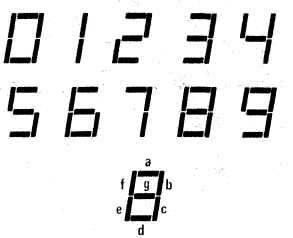
Input Protection



Common Cathode LED Display

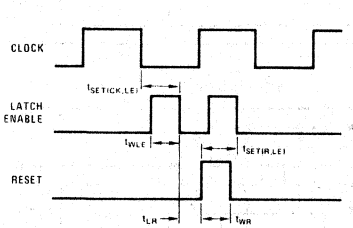


Segment Identification

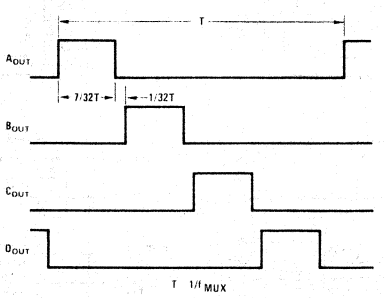


Switching Time Waveforms

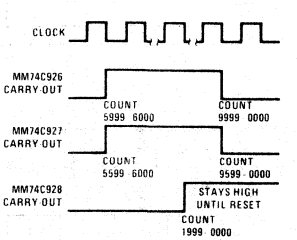
Input Waveforms



Multiplexing Output Waveforms



Carry-Out Waveforms



NSB5388 3 1/2-Digit 0.5 Inch (12.70 mm) LED Display

General Description

The NSB5388 is a 3 1/2-digit, 0.5 inch (12.70 mm) high GaAsP LED display. Basically a common cathode multiplexed display, the NSB5388 features separate access to the ± sign and decimal points and is directly compatible with the ADD3500, ADD3501 DVM circuit. Electrical connection is by PCB type terminals on the edge of the display.

The optical design of this unit creates a distinct, easy to read display with a wide viewing angle, excellent ON/OFF contrast and segment uniformity. The NSB5388 provides the designer with an effective, easy to implement answer to the need for an inexpensive large numeric display.

Recommended Display Processing

The multidigit series display is constructed on a standard printed circuit board substrate and covered with a plastic lens. The edge connector tab will stand 230°C for 5 seconds. Permanent damage to the display will result if lens temperature exceeds 70°C. Since the display is not hermetic, immersion of the entire package during flux and clean operation may cause condensation of flux or cleaner on the underside of the lens. Only the edge connectors should be immersed.

Rosin core solder, solid core solder, and low activity organic fluxes are recommended. Freon TF, Isopropanol, Methanol or Ethanol solvents are recommended only at room temperature and for short periods. The use of other solvents or elevated temperature use of the recommended solvents may cause permanent damage to the lens or display.

Applications

- Digital instrumentation
  - Power supply readouts
  - Multimeters
  - Panel meters

Absolute Ratings

Average Current per Segment	20 mA max
Peak Current per Segment	75 mA max
Reverse Voltage per Segment	3.0V max
Operating and Storage Temperature	−20°C to +70°C
Relative Humidity at 35°C	98%
Lead Temperature (Soldering, 5 seconds)	230°C

Electrical and Optical Characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Segment Light Intensity (Peak)	10 mA/Seg. Peak	0.10	0.20		mcd
Digit and D.P. Light Intensity (Peak)	10 mA/Seg. Peak	0.80	1.6		mcd
Segment Forward Voltage	10 mA/Seg. Peak		1.7	2.0	V
Segment Reverse Voltage	100 μA/Seg.	3.0	8.0		V
Peak Wavelength			660		nm
Spectral Width, Half-Intensity			40		nm
Viewing Angle, Off Axis			60		degrees
Intensity Matching	10 mA/Seg. Avg.		±33		%

National Semiconductor

NSB5918 3 3/4-Digit 0.5 Inch (12.70 mm) LED Display

General Description

The NSB5918 is a 3 3/4-digit, 0.5 inch (12.70 mm) high GaAsP LED display. Basically a common cathode multiplexed display, the NSB5918 features separate access to the ± sign and decimal points and is directly compatible with the ADD3701 DVM circuit. Electrical connection is by PCB type terminals on the edge of the display. The 3 3/4-digit is distinguished from the 3 1/2 and 4 1/2-digit designs by the fact that the overflow sign is followed by 4 full 7-segment digits.

The optical design of this unit creates a distinct, easy to read display with a wide viewing angle, excellent ON/OFF contrast and segment uniformity. The NSB5918 provides the designer with an effective, easy to implement answer to the need for an inexpensive large numeric display.

Recommended Display Processing

The multidigit series display is constructed on a standard printed circuit board substrate and covered with a plastic lens. The edge connector tab will stand 230°C for 5 seconds. Permanent damage to the display will result if lens temperature exceeds 70°C. Since the display is not hermetic, immersion of the entire package during flux and clean operation may cause condensation of flux or cleaner on the underside of the lens. Only the edge connectors should be immersed.

Rosin core solder, solid core solder, and low activity organic fluxes are recommended. Freon TF, Isopropanol, Methanol or Ethanol solvents are recommended only at room temperature and for short periods. The use of other solvents or elevated temperature use of the recommended solvents may cause permanent damage to the lens or display.

Applications

- Digital instrumentation
  - Power supply readouts
  - Multimeters
  - Panel meters

Absolute Ratings

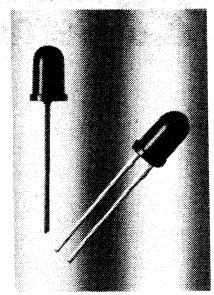
Average Current per Segment	20 mA max
Peak Current per Segment (100 μsec pulse)	150 mA max
Reverse Voltage per Segment	3.0V max
Operating and Storage Temperature	−20°C to +70°C
Relative Humidity at 35°C	98%
Lead Temperature (Soldering, 5 seconds)	230°C

Electrical and Optical Characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Segment Light Intensity	10 mA/Seg. Avg.	0.10	0.20		mcd
Digit and D.P. Light Intensity	10 mA/Seg. Avg.	0.80	1.6		mcd
Segment Forward Voltage	10 mA/Seg.		1.7	2.0	V
Segment Reverse Voltage	100 μA/Seg.	3.0	8.0		V
Peak Wavelength			660		nm
Spectral Width, Half-Intensity			40		nm
Viewing Angle, Off Axis			60		degrees
Intensity Matching	10 mA/Seg. Avg.		±33		%

National Semiconductor

Functional Blocks



NSL4944 Current Regulated, Universal LED Lamp

General Description

The NSL4944 lamp is a GaAsP red diffused solid-state high intensity LED encapsulated in a plastic package containing a current regulating IC that provides constant intensity over a wide voltage range. For applications information, see AN-153.

Applications

- Indicator lamps for back-lit panels
- Optical coupling
- Front-viewed pilot lights
- Back-lit switches
- Annunciators
- AC indicator lamps
- Battery charging circuits

Features

- 2V startup
- No series resistor required
- 18V forward voltage
- 18V reverse voltage
- Very low turn-on voltage
- AC or DC operation
- Very wide useful voltage range
- Long life
- Wide angle view
- T1 3/4 size

Maximum Ratings

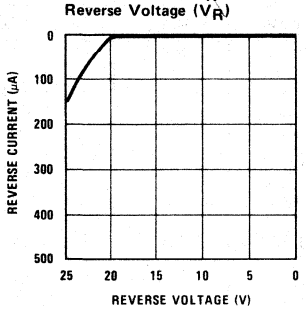
Forward Voltage @ 25°C	18V
Derate voltage linearly from 25°C	0.136V/°C
Reverse Voltage	18.0V
Power Dissipation @ 25°C	360 mW
Operating and Storage Temperature	−55 to +100°C
Lead Temperature (Soldering, 5 seconds)	260°C

Electrical and Optical Characteristics (25°C)

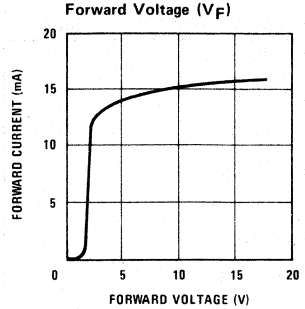
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Forward Current (I_F)	$2.4V \leq V_F \leq 18V$	10	15	20	mA
Light Intensity (I)	V_F = 5V	0.2	0.8		mcd
Reverse Breakdown Voltage (BV_R)	I_R = 100μA	18.0			V
Peak Wavelength (λ_{pk})	V_F = 10V		660		nm
Spectral Width	V_F = 10V		40		nm
Angle of Half Intensity	V_F = 10V		55		degrees
Minimum Operational Voltage	I_F = 10 mA		1.9	2.4	V

Typical Performance Characteristics (25°C)

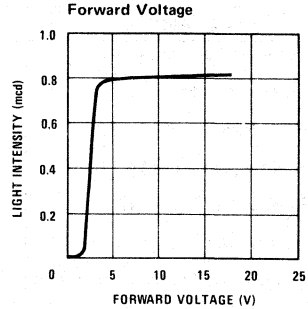
Reverse Current (I_R) vs Reverse Voltage (V_R)



Forward Current (I_F) vs Forward Voltage (V_F)

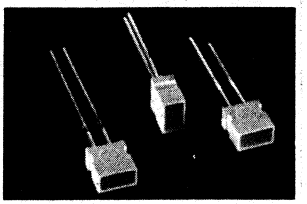


Light Intensity vs Forward Voltage



National Semiconductor

Functional Blocks
PRELIMINARY



NSL57124 Rectangular High Efficiency Red LED Lamp

General Description

The NSL57124 is a rectangularly-shaped solid state LED lamp in a plastic-encased epoxy package. The lamp emits high intensity red light from its top surface.

Features

- 0.225" x 0.125" lighted area
- End-stackable in either direction
- High brightness
- Solid state reliability
- Compact, rugged, lightweight
- No light leakage from unit or sides

Absolute Maximum Ratings

Forward Current @ 25°C	35 mA
Reverse Voltage	5.0V
Power Dissipation @ 25°C	105 mW
Derate Linearly 1.14 mW/°C from 25°C	
Peak Forward Current	1A
1 μs Pulse Width, 300 pps	
Operating and Storage Temperature Range	−55°C to +100°C
Lead Temperature (Soldering)	230°C for 5 sec.

Applications

- Legend backlighting
- Illuminated pushbutton
- Panel indicator
- Bargraph meter

Electrical and Optical Characteristics (25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage (V_F)	I_F = 20 mA		2.1	3.0	V
Luminous Intensity	I_F = 20 mA	1.0	4.0		mcd
Peak Wavelength	I_F = 20 mA		635		nm
Spectral Line Half Width	I_F = 20 mA		45		nm
Reverse Voltage (V_R)	I_R = 100 μA	5.0	25		V
Reverse Current (I_R)	V_R = 5.0V		0.020	100	μA
Angle of Half-Intensity off Axis	I_F = 20 mA		55		degrees
Capacitance	V = 0		45		pF

NSM3914, NSM3915, NSM3916 Series End-Stackable LED Bar Graph Array with Driver

General Description

The NSM3914, NSM3915, NSM3916 series are functional replacements for a variety of conventional meters. Each combines a 10-element red LED linear array and a monolithic integrated circuit display driver. The driver circuits, similar to the LM3914, LM3915, LM3916 series, light successive LEDs as the analog input voltage level increases past prescaled threshold points.

The NSM3914 provides a linear analog display, as internal threshold points are linearly scaled. A logarithmic display is provided by the NSM3915, as threshold points are set on 3 dB intervals. The NSM3916 is a variation of the logarithmic display; the VU meter function is provided by using threshold points at common VU levels.

The driver circuit contains a stable, adjustable voltage reference which precisely sets LED thresholds independently of supply voltage. Current drives to the LEDs are regulated and programmable, eliminating the need for many resistors. The entire display array can operate from supply voltages as low as 3V to as high as 24V. The internal voltage reference is also connected to an accurate 10-step voltage divider, supplying reference voltages for 10 individual comparators. These comparators switch as the signal voltage exceeds the established thresholds as described above. The typical overall inaccuracy (deviation from ideal) is typically within 1% for the NSM3914 and below 1 dB for the NSM3915 and NSM3916. A high impedance input buffer accepts signals down to ground, yet protects against signal inputs of 35V above or below ground. A single (mode) pin changes the display from a bar graph to a moving dot. Additional information regarding the internal voltage reference, LED current programming mode selection, and application hints are given in the LM3914, LM3915, LM3916 data sheets.

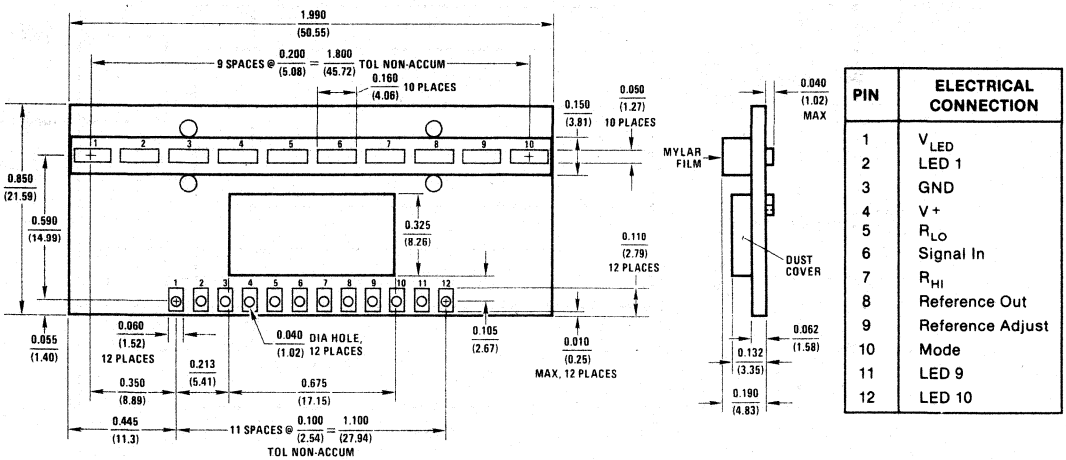
Features

- Packages are end-stackable for expanded displays
- Can be cascaded to 10 arrays (100 bar graph element)
- Linear, logarithmic, and VU meter functions performed
- Bar or dot display mode externally selectable by user
- LED current programmable from 2 mA to 30 mA
- Stable, internal voltage reference for full-scale analog inputs from 1.2V to 12V
- Inputs operate down to ground
- Signal input withstands 35V without damage or false outputs

Applications

- Power meter in stereo systems
- S meter in ham and CB radios
- VU meter in tape recorders
- Process control meters
- Replacement for edge meters

Physical Dimensions and Pin Connections inches (millimeters)



PIN	ELECTRICAL CONNECTION
1	V_{LED}
2	LED 1
3	GND
4	V+
5	R_{LO}
6	Signal In
7	R_{HI}
8	Reference Out
9	Reference Adjust
10	Mode
11	LED 9
12	LED 10

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NSM4000A LED Display with Driver

General Description

The NSM4000A is a 4-digit 0.3" height LED display with a serial data-in/parallel data-out LED driver designed to operate with minimal interface to the data source. Current drive to the LEDs is programmable by setting a reference current to a single pin.

- Enable
- TTL compatible
- Wide power supply operation
- Direct current drive (non-multiplexed)

Features

- Four 0.3" digits with right-hand decimal points
- Outputs available for two external LEDs
- LED current is programmable
- Serial data input

Applications

- COPs or microprocessor display
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block Diagram

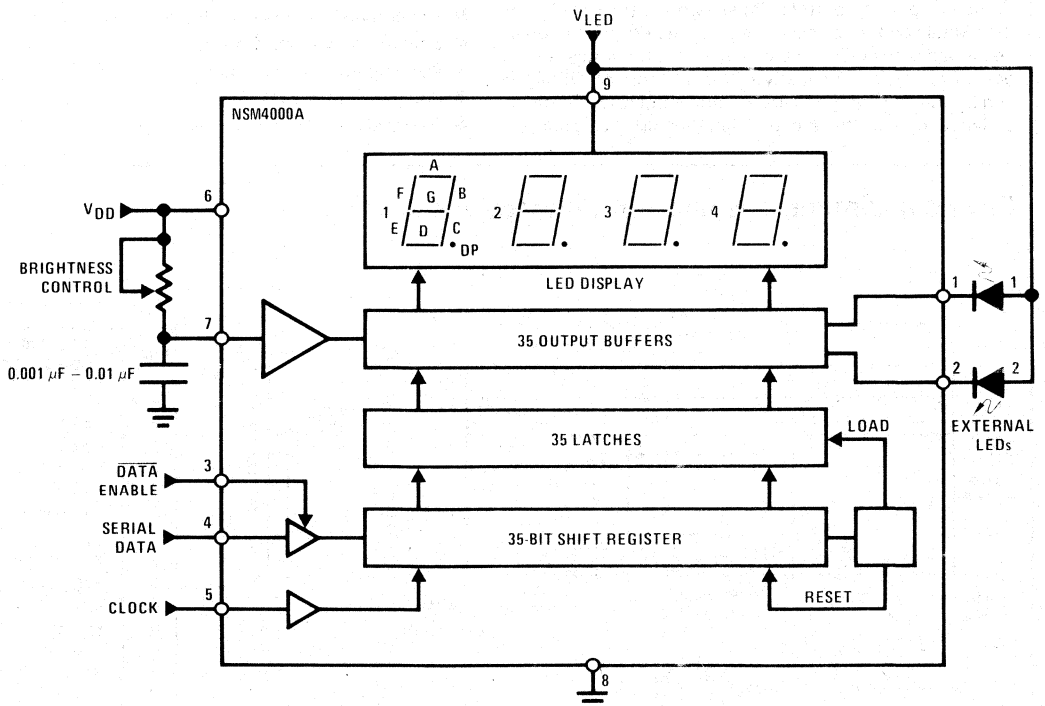

FIGURE 1

Section 10

Multiplexers

10

Section Contents

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AM3705/AM3705C 8-Channel MOS Analog Multiplexer

General Description

The AM3705/AM3705C is an eight-channel MOS analog multiplex switch. TTL compatible logic inputs that require no level shifting or input pull-up resistors and operation over a wide range of supply voltages is obtained by constructing the device with low threshold P-channel enhancement MOS technology. To simplify external logic requirements, a one-of-eight decoder and an output enable are included in the device.

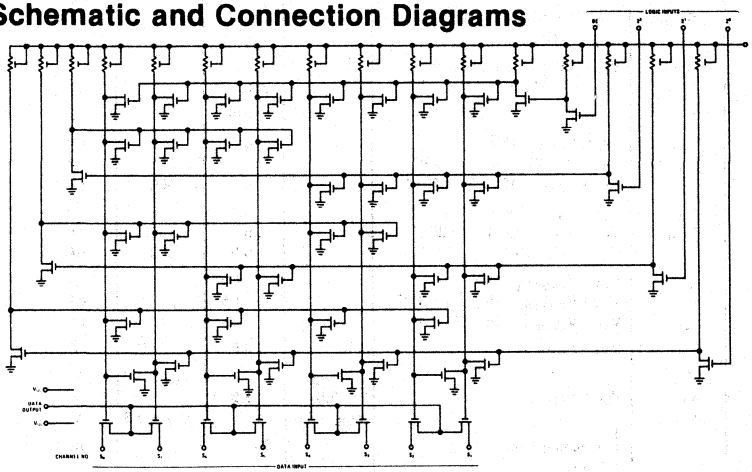
Important design features include:

- TTL/DTL compatible input logic levels
- Operation from standard +5V and −15V supplies
- Wide analog voltage range — ±5V
- One-of-eight decoder on chip
- Output enable control
- Low ON resistance — 150Ω
- Input gate protection
- Low leakage currents — 0.5 nA

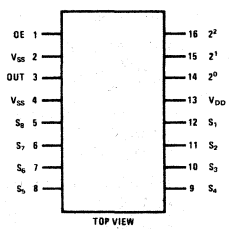
The AM3705/AM3705C is designed as a low cost analog multiplex switch to fulfill a wide variety of data acquisition and data distribution applications including cross-point switching, MUX front ends for A/D converters, process controllers, automatic test gear, programmable power supplies and other military or industrial instrumentation applications.

The AM3705 is specified for operation over the −55°C to +125°C military temperature range. The AM3705C is specified for operation over the −25°C to +85°C temperature range.

Schematic and Connection Diagrams



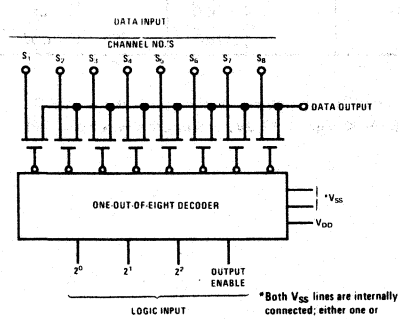
Dual-In-Line Package



Order Number AM3705D or AM3705CD
See NS Package D16A

Order Number AM3705F or AM3705CF
See NS Package F16A

Block Diagram (MIL-STD-806B)



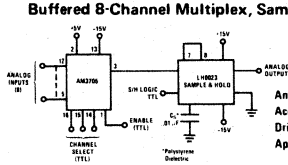
*Both V_{SS} lines are internally connected; either one or both may be used.

Truth Table

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

Typical Application

Buffered 8-Channel Multiplex, Sample and Hold



Analog Signal Range — 0.5V
Acquisition Time — 25 ns
Drift Rate — 0.5 mV/sec
Aperature Time — 250 ns

Absolute Maximum Ratings

Positive Voltage on Any Pin (Note 1)	+0.3V
Negative Voltage on Any Pin (Note 1)	−35V
Source to Drain Current	±30 mA
Logic Input Current	±0.1 mA
Power Dissipation (Note 2)	500 mW
Operating Temperature Range AM3705	−55°C to +125°C
AM3705C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 3)

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
ON Resistance	R_{ON}	$V_{IN} = V_{SS}$; $I_{OUT} = 100\ \mu A$		80	250	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\ \mu A$		160	400	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\ \mu A$				
AM3705		$T_A = +125°C$			400	Ω
AM3705C		$T_A = +70°C$			400	Ω
ON Resistance	R_{ON}	$V_{IN} = +5V$; $V_{DD} = -15V$; $I_{OUT} = 100\ \mu A$		100		Ω
ON Resistance	R_{ON}	$V_{IN} = 0V$, $V_{DD} = -15V$, $I_{OUT} = -100\ \mu A$		150		Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $V_{DD} = -15V$; $I_{OUT} = -100\ \mu A$		250		Ω
OFF Resistance	R_{OFF}			10^{10}		Ω
Output Leakage Current	I_{LO}	$V_{SS} - V_{OUT} = 15V$		0.5	10	nA
AM3705	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 125°C$		150	500	nA
AM3705C	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 70°C$		35	500	nA
Data Input Leakage Current	I_{LDI}	$V_{SS} - V_{IN} = 15V$		0.1	3.0	nA
AM3705	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 125°C$		25	500	nA
AM3705C	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 70°C$		0.5	500	nA
Logic Input Leakage Current	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$		.001	1	μA
AM3705	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 125°C$		.05	10	μA
AM3705C	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 70°C$		.05	10	μA
Logic Input LOW Level	V_{IL}	$V_{SS} = +5.0V$		0.5	1.0	V
Logic Input LOW Level	V_{IL}		V_{DD}		$V_{SS} - 4.0$	V
Logic Input HIGH Level	V_{IH}	$V_{SS} = +5.0V$	3.0	3.5		V
Logic Input HIGH Level	V_{IH}		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
Channel Switching Time-Positive	t^+	Switching Time Test Circuit		300		ns
Channel Switching Time-Negative	t^-	Switching Time Test Circuit		600		ns
Channel Separation		f = 1 kHz		62		dB
Output Capacitance	C_{db}	$V_{SS} - V_{OUT} = 0$; f = 1 MHz		35		pF
Data Input Capacitance	C_{sb}	$V_{SS} - V_{DIP} = 0$; f = 1 MHz		6.0		pF
Logic Input Capacitance	C_{cg}	$V_{SS} - V_{Logic\ In} = 0$; f = 1 MHz		6.0		pF
Power Dissipation	P_D	$V_{DD} = -31V$, $V_{SS} = 0V$		125	175	mW

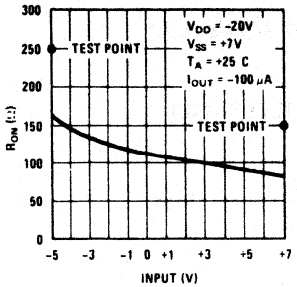
Note 1: All voltages referenced to V_{SS}.

Note 2: Ratings applies for ambient temperatures to +25°C, derate linearly at 3 mW/°C for ambient temperatures above +25°C.

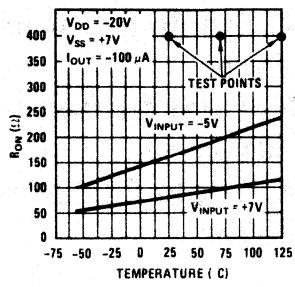
Note 3: Specifications apply for $T_A = 25°C$, $-24V \leq V_{DD} \leq -20V$, and $+5.0V \leq V_{SS} \leq +7.0V$; unless otherwise specified (all voltages are referenced to ground).

Typical Performance Characteristics

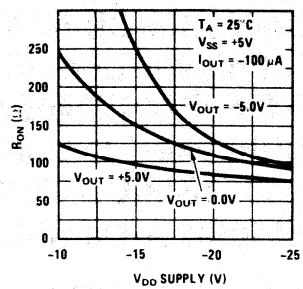
ON Resistance vs Analog Input Voltage



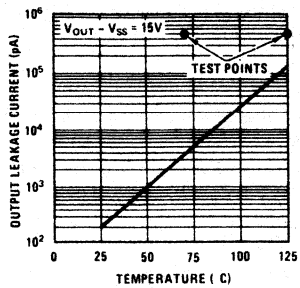
ON Resistance vs Ambient Temperature



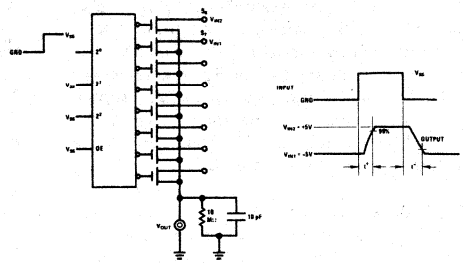
ON Resistance vs V_{DD} Supply Voltage



Output Leakage Current vs Ambient Temperature

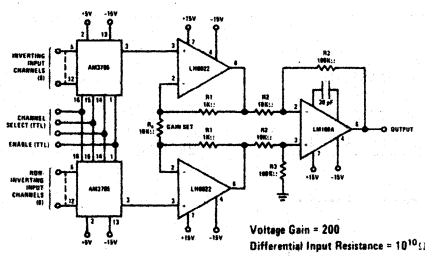


Switching Time Test Circuit



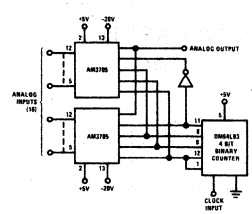
Typical Applications (Continued)

Differential Input MUX

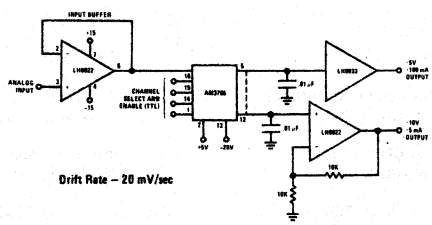


Voltage Gain = 200
Differential Input Resistance = 10^{10} Ω
CMRR = 100 dB
Input Current = 0.5 nA

16-Channel Commutator

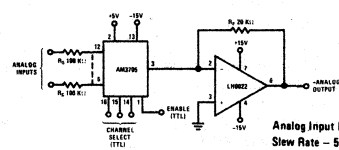


8-Channel Demultiplexer with Sample and Hold



Drift Rate – 20 mV/sec

Wide Input Range Analog Switch



Analog Input Range – 25V
Slew Rate – 5 V/μs

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CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to 15 Vp-p can be achieved by digital signal amplitudes of 3-15 V. For example, if V_{DD} = 5 V, V_{SS} = 0 V and V_{EE} = −5 V, analog signals from −5 V to +5 V can be controlled by digital inputs of 0-5 V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF."

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

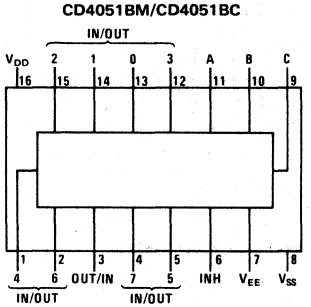
CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

Features

- Wide range of digital and analog signal levels: digital 3-15 V, analog to 15 Vp-p
- Low "ON" resistance: 80 Ω (typ) over entire 15 Vp-p signal-input range for $V_{DD} - V_{EE}$ = 15 V
- High "OFF" resistance: channel leakage of ±10 pA (typ) at $V_{DD} - V_{EE}$ = 10 V
- Logic level conversion for digital addressing signals of 3-15 V ($V_{DD} - V_{SS}$ = 3-15 V) to switch analog signals to 15 Vp-p ($V_{DD} - V_{EE}$ = 15 V)
- Matched switch characteristics: ΔR_{ON} = 5 Ω (typ) for $V_{DD} - V_{EE}$ = 15 V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ) at $V_{DD} - V_{SS} = V_{DD} - V_{EE}$ = 10 V
- Binary address decoding on chip

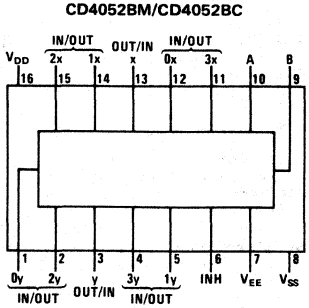
Connection Diagrams

CD4051BM/CD4051BC



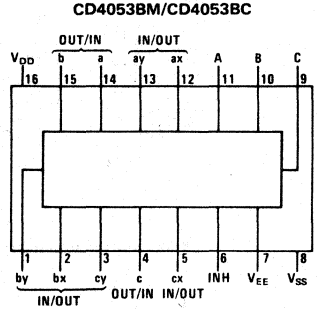
TOP VIEW

CD4052BM/CD4052BC



TOP VIEW

CD4053BM/CD4053BC



TOP VIEW

Order Number CD4051BMJ or CD4051BCJ
See NS Package J16A

Order Number CD4051BCN
See NS Package N16A

Order Number CD4051BMW
See NS Package W16A

Order Number CD4052BCJ or CD4052BMJ
See NS Package J16A

Order Number CD4052BCN
See NS Package N16A

Order Number CD4052BMW
See NS Package W16A

Order Number CD4053BCJ or CD4053BMJ
See NS Package J16A

Order Number CD4053BCN
See NS Package N16A

Order Number CD4053BMW
See NS Package W16A

Absolute Maximum Ratings

V_{DD}	DC Supply Voltage	−0.5 Vdc to +18 Vdc
V_{IN}	Input Voltage	−0.5 Vdc to V_{DD} + 0.5 Vdc
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

Recommended Operating Conditions

V_{DD}	DC Supply Voltage	+5 Vdc to +15 Vdc
V_{IN}	Input Voltage	0 V to V_{DD} Vdc
T_A	Operating Temperature Range	
	4051BM/4052BM/4053BM	−55°C to +125°C
	4051BC/4052BC/4053BC	−40°C to +85°C

DC Electrical Characteristics (Note 2)

	Parameter	Conditions		−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Units
I_{DD}	Quiescent Device Current	V_{DD} = 5 V			5			5		150	μA
		V_{DD} = 10 V			10			20		600	μA
		V_{DD} = 15 V			20			20		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \leq V_{IS} \leq V_{DD}$)	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5 V, V_{EE} = −2.5 V or V_{DD} = 5 V, V_{EE} = 0 V		2000		270	2500		3500	Ω
			V_{DD} = 5 V, V_{EE} = −5 V or V_{DD} = 10 V, V_{EE} = 0 V		310		120	400		580	Ω
			V_{DD} = 7.5 V, V_{EE} = −7.5 V or V_{DD} = 15 V, V_{EE} = 0 V		220		80	280		400	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5 V, V_{EE} = −2.5 V or V_{DD} = 5 V, V_{EE} = 0 V				10				Ω
			V_{DD} = 5 V, V_{EE} = −5 V or V_{DD} = 10 V, V_{EE} = 0 V				10				Ω
			V_{DD} = 7.5 V, V_{EE} = −7.5 V or V_{DD} = 15 V, V_{EE} = 0 V				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	V_{DD} = 7.5 V, V_{EE} = −7.5 V O/I = ±7.5 V, I/O = 0 V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5 V V_{DD} = 7.5 V, V_{EE} = −7.5 V, O/I = 0 V, I/O = ±7.5 V	CD4051 CD4052 CD4053		±200 ±200 ±200		±0.08 ±0.04 ±0.02	±200 ±200 ±200		±2000 ±2000 ±2000	nA nA nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	V_{EE} = V_{SS} R_L = 1 kΩ to V_{SS} I_{IS} < 2 μA on all OFF channels V_{IS} = V_{DD} thru 1 kΩ									
		V_{DD} = 5 V			1.5			1.5		1.5	V
		V_{DD} = 10 V			3.0			3.0		3.0	V
		V_{DD} = 15 V			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5		3.5		3.5			3.5		V
		V_{DD} = 10		7		7			7		V
		V_{DD} = 15		11		11			11		V
I_{IN}	Input Current	V_{DD} = 15 V, V_{EE} = 0 V V_{IN} = 0 V			−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15 V, V_{EE} = 0 V V_{IN} = 15 V			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics (Continued) (Note 2)

	Parameter	Conditions		−40°C		+25°C		+85°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V			20			20		150	μA
		V_{DD} = 10V			40			40		300	μA
		V_{DD} = 15V			80			80		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \leq V_{IS} \leq V_{DD}$)	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V		2100		270	2500		3200	Ω
			V_{DD} = 5V, V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V		330		120	400		520	Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V		230		80	280		360	Ω
ΔR_{ON}	Δ "ON" Resistance Between Any Two Channels	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V				10				Ω
			V_{DD} = 5V V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V				10				Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	V_{DD} = 7.5V, V_{EE} = −7.5V O/I = ±7.5V, I/O = 0V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V	CD4051		±200		±0.08	±200		±2000	nA
		V_{DD} = 7.5V, V_{EE} = −7.5V, O/I = 0V	CD4052		±200		±0.04	±200		±2000	nA
		I/O = ±7.5V	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	V_{EE} = V_{SS} R_L = 1 kΩ to V_{SS} I_{IS} < 2μA on all OFF Channels V_{IS} = V_{DD} thru 1kΩ									
		V_{DD} = 5V			1.5			1.5		1.5	V
		V_{DD} = 10V			3.0			3.0		3.0	V
		V_{DD} = 15V			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5		3.5		3.5			3.5		V
		V_{DD} = 10		7		7			7		V
		V_{DD} = 15		11		11			11		V
I_{IN}	Input Current	V_{DD} = 15V, V_{EE} = 0V V_{IN} = 0V			−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{EE} = 0V V_{IN} = 15V			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

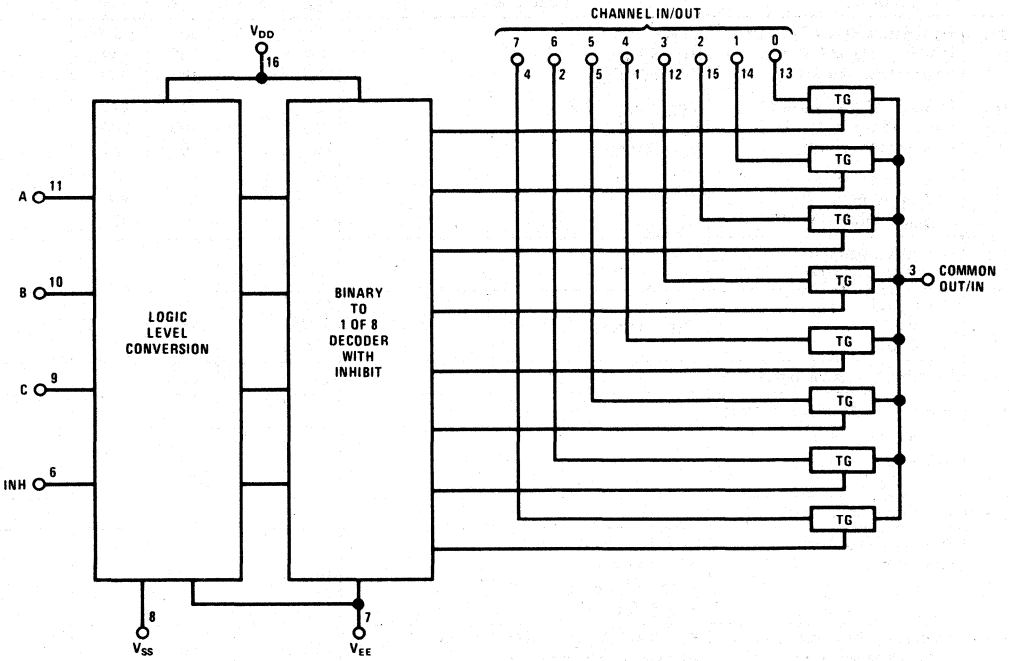
AC Electrical Characteristics

$T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

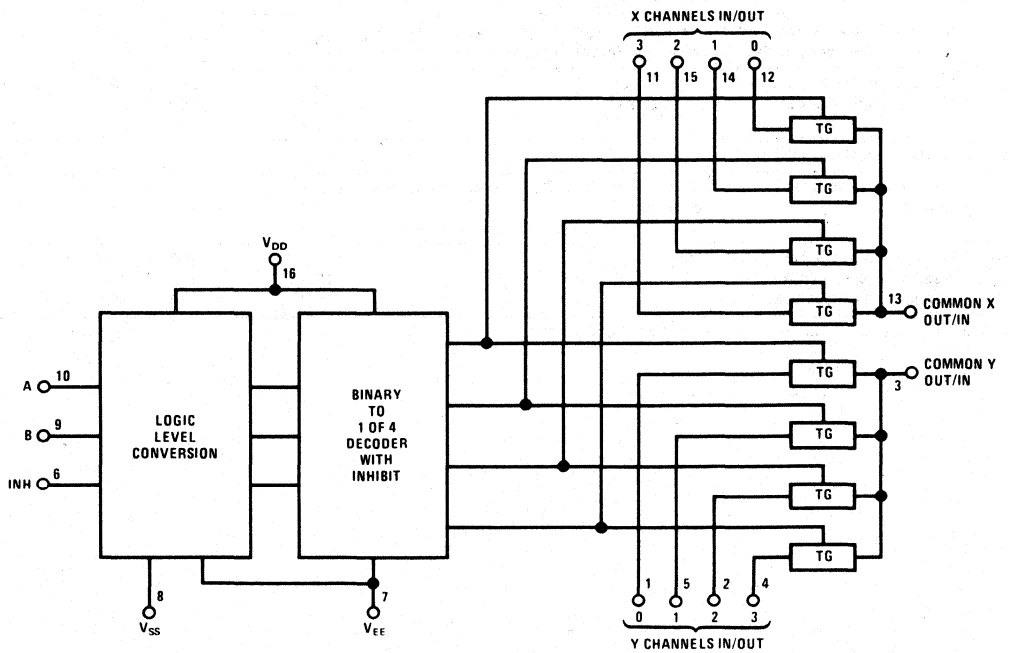
	Parameter	Conditions	V_{pp}	Min	Typ	Max	Units
t_{PZH}, t_{PZL}	Propagation Delay Time from Inhibit to Signal Output (channel turning on)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50$ pF	5V 10V 15V		600 225 160	1200 450 320	ns ns ns
t_{PHZ} t_{PLZ}	Propagation Delay Time from Inhibit to Signal Output (channel turning off)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50$ pF	5V 10V 15V		210 100 75	420 200 150	ns ns ns
C_{IN}	Input Capacitance Control Input Signal Input (IN/OUT)				 5 10	 7.5 15	 pF pF
C_{OUT}	Output Capacitance (common OUT/IN)						
	CD4051 CD4052 CD4053	$V_{EE} = V_{SS} = 0V$	10V 10V 10V		30 15 8		pF pF pF
C_{IOS}	Feedthrough Capacitance				0.2		pF
C_{PD}	Power Dissipation Capacitance						
	CD4051 CD4052 CD4053				110 140 70		pF pF pF
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response (Distortion)	$R_L = 10\ k\Omega$ $f_{IS} = 1$ kHz $V_{IS} = 5\ V_{p-p}$ $V_{EE} = V_{SI} = 0V$	10V		0.04		%
	Frequency Response, Channel "ON" (Sine Wave Input)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20\log_{10} V_{OS}/V_{IS} = -3$ dB	10V		40		MHz
	Feedthrough, Channel "OFF"	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20\log_{10} V_{OS}/V_{IS} = -40$ dB	10V		10		MHz
	Crosstalk Between Any Two Channels (frequency at 40 dB)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$ $20\log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3)	10V		3		MHz
t_{PHL}, t_{PLH}	Propagation Delay Signal Input to Signal Output	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		25 15 10	55 35 25	ns ns ns
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal Crosstalk	$V_{EE} = V_{SS} = 0V$, $R_L = 10\ k\Omega$ at both ends of channel. Input Square Wave Amplitude = 10V	10V		65		mV (peak)
t_{PHL}, t_{PLH}	Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF")	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		500 180 120	1000 360 240	ns ns ns

Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF".

Block Diagrams

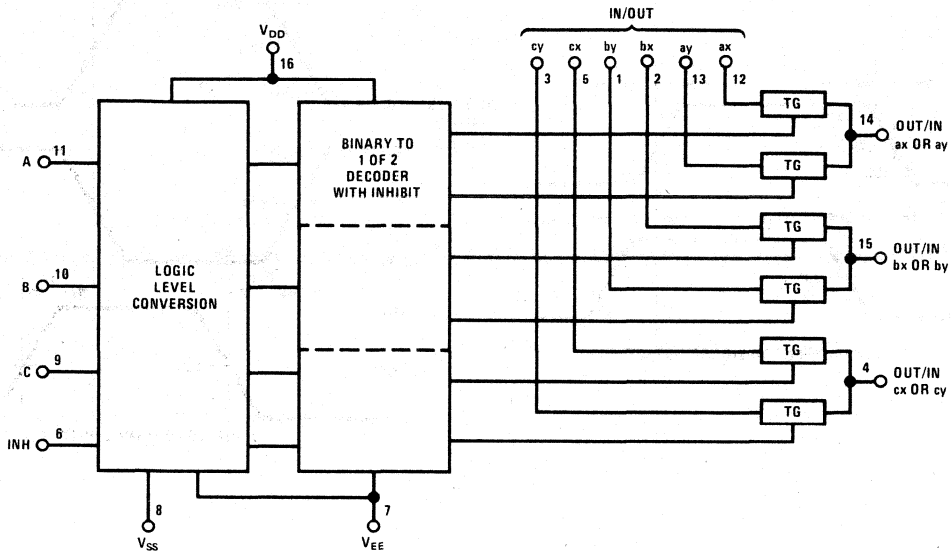


CD4051BM/CD4051BC



CD4052BM/CD4052BC

Block Diagrams (Continued)

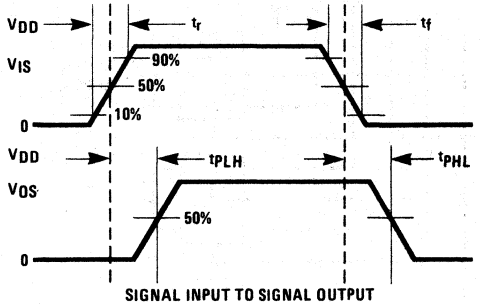


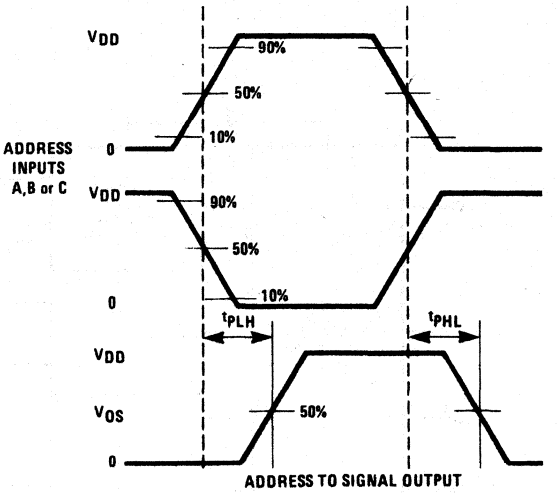
CD4053BM/CD4053BC

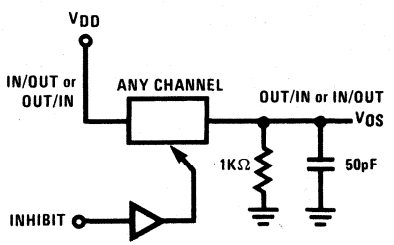
INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

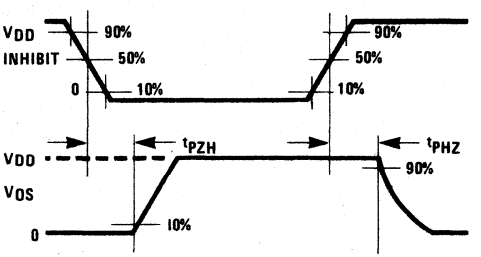
* Don't Care condition.

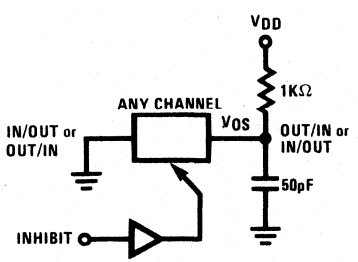
Switching Time Waveforms

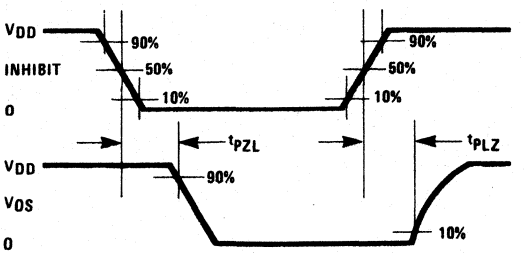










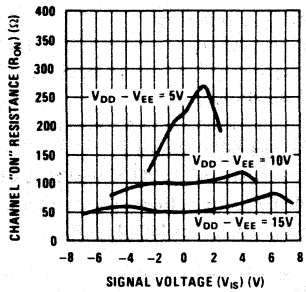


Special Considerations

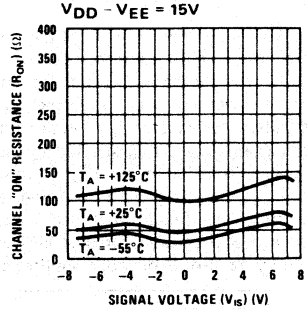
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6 V at $T_A \leq 25°C$, or 0.4 V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

Typical Performance Characteristics

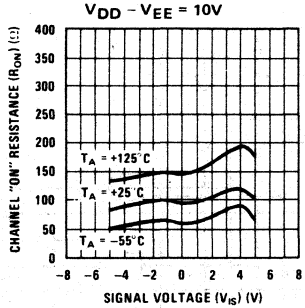
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



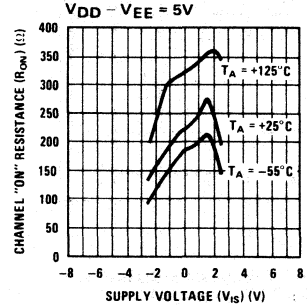
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



National Semiconductor

CD4529BM/CD4529BC Dual 4-Channel or Single 8-Channel Analog Data Selector

General Description

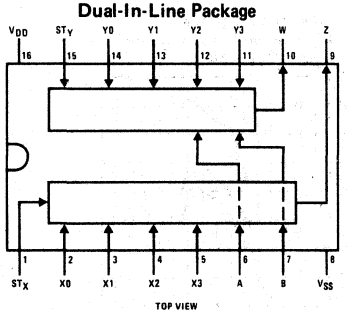
The CD4529B is a dual 4-channel or a single 8-channel analog data selector, implemented with complementary MOS (CMOS) circuits constructed with N and P-channel enhancement mode transistors. Dual 4-channel or 8-channel mode operation is selected by proper input coding, with outputs Z and W tied together for the single 8-bit mode. The device is suitable for digital as well as analog applications, including various 1-of-4 and 1-of-8 data selector functions. Since the device is analog and bidirectional, it can also be used for dual binary to 1-of-4 or single binary to 1-of-8 decoder applications.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} typ
- Low quiescent power dissipation 0.005 μW/package typical @ 5 V_{DC}
- 10 MHz frequency operation (typical)
- Data paths are bidirectional
- Linear ON resistance (120Ω typical @ 15V)
- TRI-STATE® outputs (high impedance disable strobe)
- Plug-in replacement for MC14529B

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number CD4529BCJ or CD4529BMJ
See NS Package J16A

Order Number CD4529BCN
See NS Package N16A

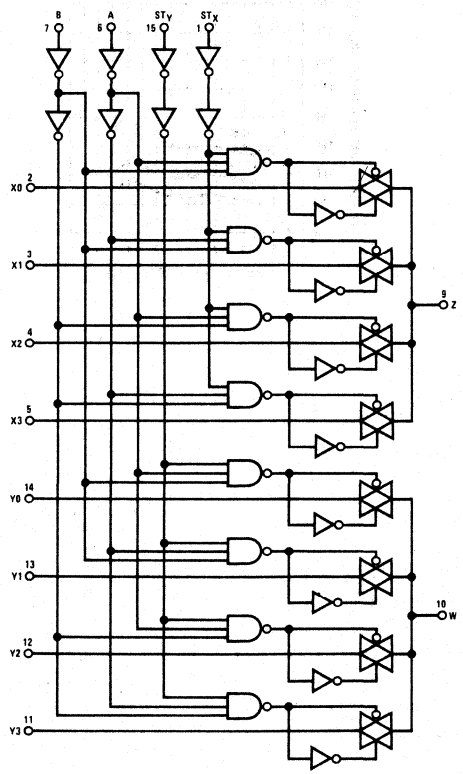
Order Number CD4529BMW
See NS Package W16A

Truth Table

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X	High Impedance (TRI-STATE®)		

X = Don't care

Logic Diagram



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4529BM	−55°C to +125°C
CD4529BC	−40°C to +85°C

DC Electrical Characteristics CD4529BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.001	1.0		60	μA
		V_{DD} = 10V		1.0		0.002	1.0		60	μA
		V_{DD} = 15V		2.0		0.003	2.0		120	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		400		165	480		640	Ω
		V_{IN} = −5V		400		100	480		640	Ω
		V_{IN} = ±0.25V		400		155	480		640	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		240		135	270		400	Ω
		V_{IN} = −7.5V		240		75	270		400	Ω
		V_{IN} = ±0.25V		240		100	270		400	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		400		165	480		640	Ω
		V_{IN} = 0.25V		400		100	480		640	Ω
		V_{IN} = 5.6V		400		160	480		640	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		400	Ω
		V_{IN} = 0.25V		250		75	270		400	Ω
		V_{IN} = 9.3V		250		110	270		400	Ω
I_{OFF}	Input to Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V, V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −5V, V_{DD} = 5V, V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±2500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±2500	nA

DC Electrical Characteristics CD4529BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.001	5.0		70	μA
		V_{DD} = 10V		5.0		0.002	5.0		70	μA
		V_{DD} = 15V		10.0		0.003	10.0		140	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.00		4.95		V
		V_{DD} = 10V	9.95		9.95	10.00		9.95		V
		V_{DD} = 15V	14.95		14.95	15.00		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		410		165	480		560	Ω
		V_{IN} = −5V		410		100	480		560	Ω
		V_{IN} = ±0.25V		410		155	480		560	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		250		135	270		350	Ω
		V_{IN} = −7.5V		250		75	270		350	Ω
		V_{IN} = ±0.25V		250		100	270		350	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		410		165	480		560	Ω
		V_{IN} = 0.25V		410		100	480		560	Ω
		V_{IN} = 5.6V		410		160	480		560	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		350	Ω
		V_{IN} = 0.25V		250		75	270		350	Ω
		V_{IN} = 9.3V		250		110	270		350	Ω
I_{OFF}	Input-Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V								
		V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±500	nA
		V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V								
		V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±1000	nA
		V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±1000	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Switch OFF is defined as $|I_O| \leq 10\ \mu A$, switch ON as defined by R_{ON} specification.

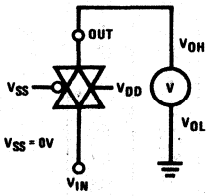
AC Electrical Characteristics CD4529BM/CD4529BC

$T_A = 25°C$, $R_L = 1\ k\Omega$, $t_r = t_f = 20$ ns, unless otherwise specified.

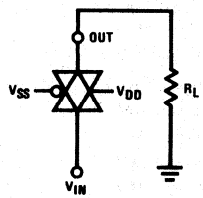
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	V_{IN} to V_{OUT} Propagation Delay	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		10	20	ns
		$V_{DD} = 15V$		8	15	ns
t_{PLH}, t_{PHL}	Control to Output Propagation Delay	$V_{IN} = V_{DD}$ or V_{SS}, $C_L = 50$ pF, $V_{IN} \leq 10V$				
		$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		50	120	ns
f_{MAX}	Maximum Control Input Pulse Frequency	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		5		MHz
		$V_{DD} = 10V$		10		MHz
		$V_{DD} = 15V$		12		MHz
	Crosstalk, Control to Output	$R_{OUT} = 10\ k\Omega$, $C_L = 50$ pF, $V_{SS} = 0$				
		$V_{DD} = 5V$		5.0		mV
		$V_{DD} = 10V$		5.0		mV
		$V_{DD} = 15V$		5.0		mV
	Noise Voltage	$f = 100$ Hz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		24		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		25		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		30		$nV/\sqrt{cycle}$
		$f = 100$ kHz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		15		$nV/\sqrt{cycle}$
	Sine Wave (Distortion)	$V_{IN} = 1.77$Vrms Centered at 0V, $R_L = 10\ k\Omega$, $f = 1$ kHz, $V_{SS} = -5V$, $V_{DD} = 5V$		0.36		%
I_{LOSS}	Insertion Loss, $I_{LOSS} = 20\ Log_{10} \frac{V_{OUT}}{V_{IN}}$	$V_{IN} = 1.77$Vrms Centered at 0V, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$		2.0		dB
		$R_L = 10\ k\Omega$		0.8		dB
		$R_L = 100\ k\Omega$		0.25		dB
		$R_L = 1\ M\Omega$		0.01		dB
BW	Bandwidth, −3 dB	$V_{IN} = 1.77$Vrms Centered at 0 Vdc, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	35			MHz
		$R_L = 10\ k\Omega$	28			MHz
		$R_L = 100\ k\Omega$	27			MHz
		$R_L = 1\ M\Omega$	26			MHz
	Feedthrough and Crosstalk, $20\ Log_{10} \frac{V_{OUT}}{V_{IN}} = -50$ dB	$V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	850			kHz
		$R_L = 10\ k\Omega$	100			kHz
		$R_L = 100\ k\Omega$	12			kHz
		$R_L = 1\ M\Omega$	1.5			kHz

Test Circuits and Switching Time Waveforms

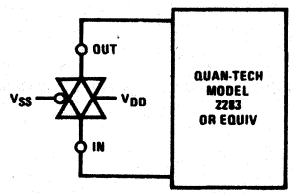
Output Voltage



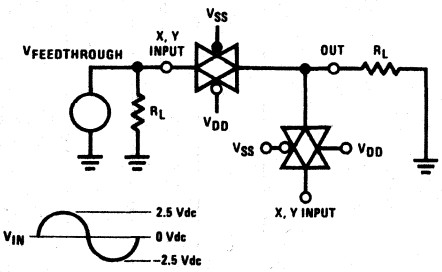
R_{ON} Characteristics



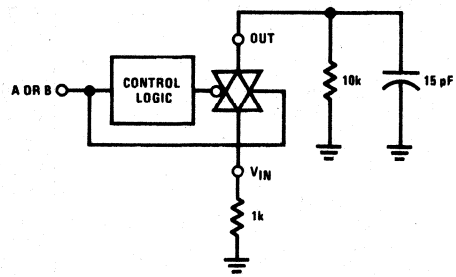
Noise Voltage



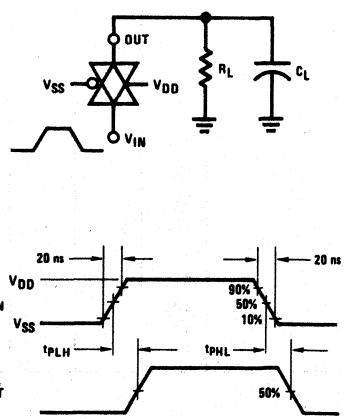
Frequency Response



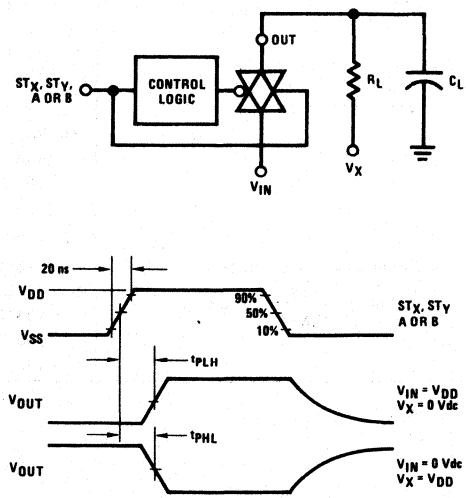
Crosstalk



Propagation Delay

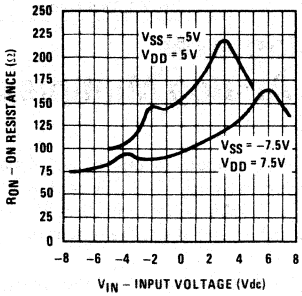


Turn-ON Delay Time

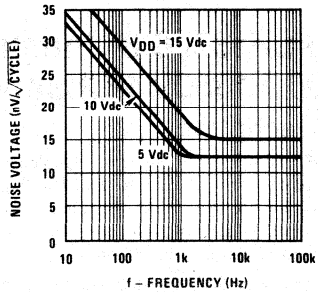


Typical Performance Characteristics

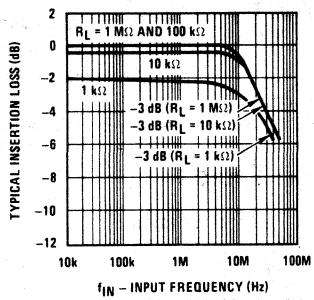
Typical R_{ON} vs V_{IN}



Typical Noise Characteristics

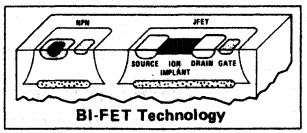


Typical Insertion Loss/ Bandwidth Characteristics



National Semiconductor

Multiplexers



LF11508/LF13508 8-Channel Analog Multiplexer
LF11509/LF13509 4-Channel Differential Analog Multiplexer

General Description

The LF11508/LF13508 is an 8-channel analog multiplexer which connects the output to 1 of the 8 analog inputs depending on the state of a 3-bit binary address. An enable control allows disconnecting the output, thereby providing a package select function.

This device is fabricated with National's BI-FET technology which provides ion-implanted JFETs for the analog switch on the same chip as the bipolar decode and switch drive circuitry. This technology makes possible low constant "ON" resistance with analog input voltage variations. This device does not suffer from latch-up problems or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action.

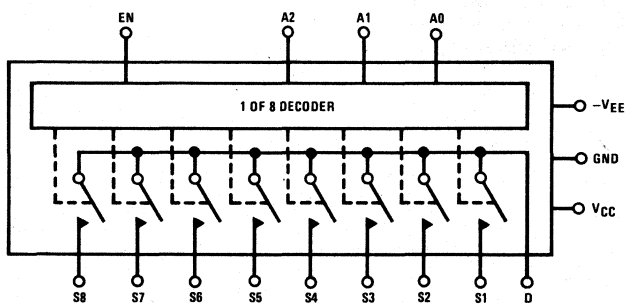
The LF11509/LF13509 is a 4-channel differential analog multiplexer. A 2-bit binary address will connect a pair of independent analog inputs to one of any 4 pairs of independent analog outputs. The device has all the features of the LF11508 series and should be used whenever differential analog inputs are required.

Features

- JFET switches rather than CMOS
- No static discharge blow-out problem
- No SCR latch-up problems
- Analog signal range 11V, −15V
- Constant "ON" resistance for analog signals between −11V and 11V
- "ON" resistance 380 Ω typ
- Digital inputs compatible with TTL and CMOS
- Output enable control
- Break-before-make action: t_{OFF} = 0.2 μs; t_{ON} = 2 μs typ
- Lower leakage devices available

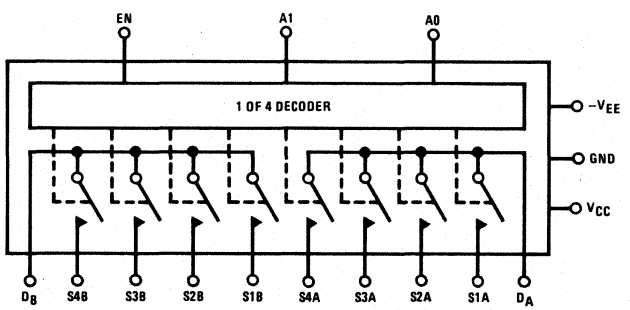
Functional Diagrams and Truth Tables

LF11508/LF13508



EN	A2	A1	A0	SWITCH ON
H	L	L	L	S1
H	L	L	H	S2
H	L	H	L	S3
H	L	H	H	S4
H	H	L	L	S5
H	H	L	H	S6
H	H	H	L	S7
H	H	H	H	S8
L	X	X	X	NONE

LF11509/LF13509



EN	A1	A0	SWITCH PAIR ON
L	X	X	None
H	L	L	S1
H	L	H	S2
H	H	L	S3
H	H	H	S4

Absolute Maximum Ratings

	LF11508, LF11509	LF13508, LF13509
Positive Supply − Negative Supply ($V_{CC} - V_{EE}$)	36V	36V
Positive Analog Input Voltage (Note 1)	V_{CC}	V_{CC}
Negative Analog Input Voltage (Note 1)	$-V_{EE}$	$-V_{EE}$
Positive Digital Input Voltage	V_{CC}	V_{CC}
Negative Digital Input Voltage	−5V	−5V
Analog Switch Current	$\|I_S\| < 10$ mA	$\|I_S\| < 10$ mA
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)		
Molded DIP (N) P_D	–	500 mW
θ_{jA}	–	150°C/W
Cavity DIP (D) P_D	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C

Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LF11508, LF11509			LF13508, LF13509			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
R_{ON}	"ON" Resistance	V_{OUT} = 0V, I_S = 100 μA	T_A = 25°C		380	500		380	650	Ω
					600	750		500	850	Ω
ΔR_{ON}	ΔR_{ON} with Analog Voltage Swing	$-10V \leq V_{OUT} \leq +10V$, I_S = 100 μA	T_A = 25°C		0.01	1		0.01	1	%
R_{ON} Match	R_{ON} Match Between Switches	V_{OUT} = 0V, I_S = 100 μA	T_A = 25°C		20	100		20	150	Ω
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF", V_S = 11, V_D = −11, (Note 4)	T_A = 25°C			1			5	nA
					10	50		0.09	50	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF", V_S = 11, V_D = −11, (Note 4)	T_A = 25°C			10			20	nA
					25	500		0.6	500	nA
$I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON" V_D = 11V, (Note 4)	T_A = 25°C			10			20	nA
					35	500		1	500	nA
V_{INH}	Digital "1" Input Voltage			2.0			2.0			V
V_{INL}	Digital "0" Input Voltage					0.7			0.7	V
I_{INL}	Digital "0" Input Current	V_{IN} = 0.7V	T_A = 25°C		1.5	20		1.5	30	μA
						40			40	μA
$I_{INL(EN)}$	Digital "0" Enable Current	V_{EN} = 0.7V	T_A = 25°C		1.2	20		1.2	30	μA
						40			40	μA
t_{TRAN}	Switching Time of Multiplexer	*(Figure 1)*, (Note 5)	T_A = 25°C		2.0	3		1.8		μs
t_{OPEN}	Break-Before-Make	*(Figure 3)*	T_A = 25°C		1.6			1.6		μs
$t_{ON(EN)}$	Enable Delay "ON"	*(Figure 2)*	T_A = 25°C		1.6			1.6		μs
$t_{OFF(EN)}$	Enable Delay "OFF"	*(Figure 2)*	T_A = 25°C		0.2			0.2		μs
$V_{ISO(OFF)}$	"OFF" Isolation	(Note 6)	T_A = 25°C		−66			−66		dB
V_{CT}	Crosstalk	LF11509 Series, (Note 6)	T_A = 25°C		−66			−66		dB
$C_{S(OFF)}$	Source Capacitance ("OFF")	Switch "OFF", V_{OUT} = 0V, V_S = 0V	T_A = 25°C		2.2			2.2		pF
$C_{D(OFF)}$	Drain Capacitance ("OFF")	Switch "OFF", V_{OUT} = 0V, V_S = 0V	T_A = 25°C		11.4			11.4		pF
I_{CC}	Positive Supply Current	All Digital Inputs Grounded	T_A = 25°C		7.4	10		7.4	12	mA
					9.2	13		7.9	15	mA
I_{EE}	Negative Supply Current	All Digital Inputs Grounded	T_A = 25°C		2.7	4.5		2.7	5	mA
					2.9	5.5		2.8	6	mA

Notes

Note 1: If the analog input voltage exceeds this limit, the input current should be limited to less than 10 mA.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{DMAX}, whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

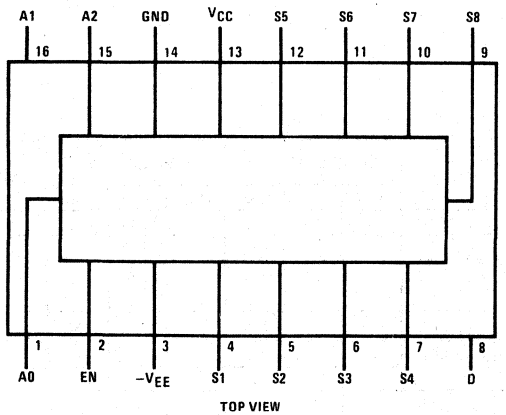
Note 4: Conditions applied to leakage tests insure worse case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".

Note 5: Lots are sample tested to this parameter. The measurement conditions of *Figure 1* insure worse case transition time.

Note 6: "OFF" isolation is measured with all switches "OFF" and driving a source. Crosstalk is measured with a pair of switches "ON", driving channel A and measuring channel B. $R_L = 200$, $C_L = 7$ pF, $V_S = 3$ Vrms, f = 500 kHz.

Connection Diagrams

LF11508/LF13508
Dual-In-Line Package

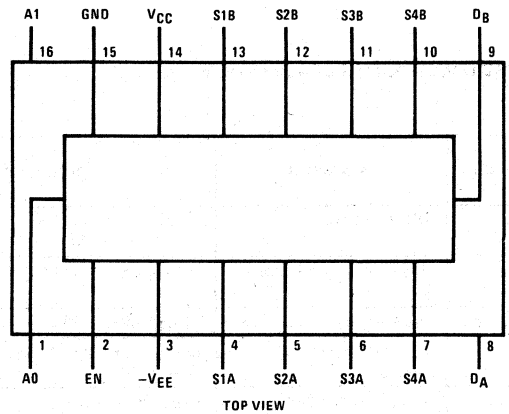


TOP VIEW

Order Number LF11508D or LF13508D
See NS Package D16C

Order Number LF13508N
See NS Package N16A

LF11509/LF13509
Dual-In-Line Package

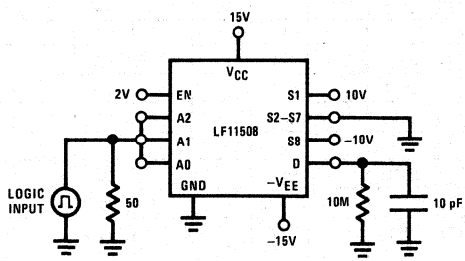


TOP VIEW

Order Number LF11509D or LF13509D
See NS Package D16C

Order Number LF13509N
See NS Package N16A

AC Test Circuits and Switching Time Waveforms



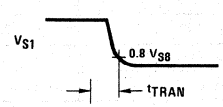
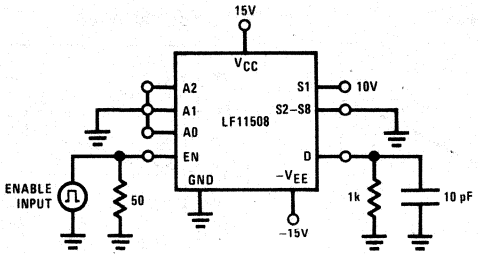


FIGURE 1. Transition Time

AC Test Circuit and Switching Time Waveforms (Continued)



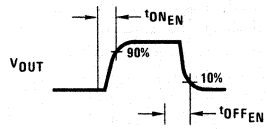
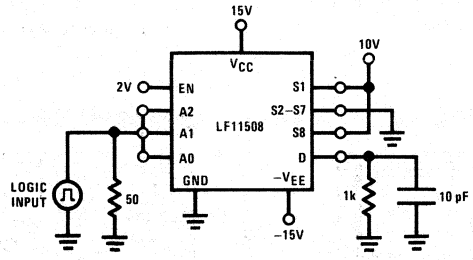


FIGURE 2. Enable Times



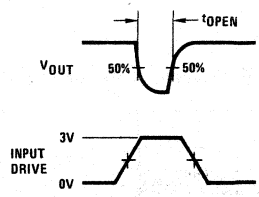
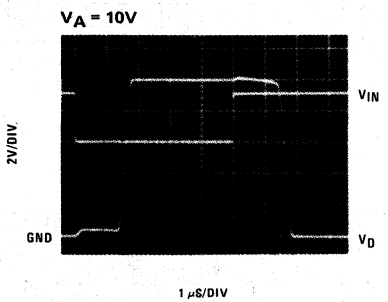
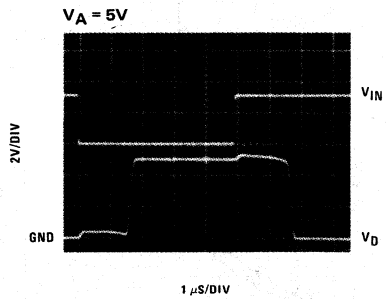
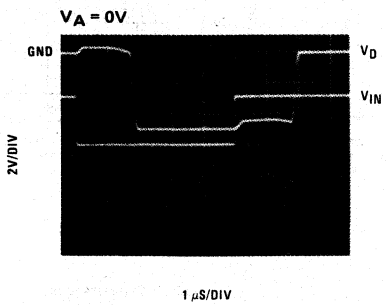


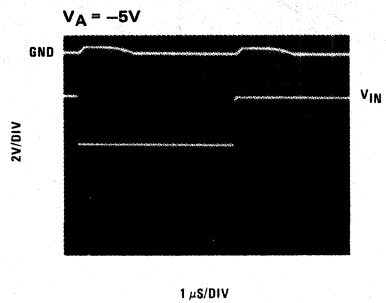
FIGURE 3. Break-Before-Make

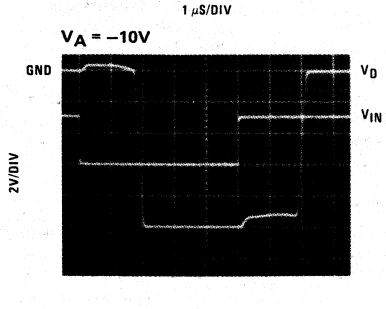
Transition Times and Transients

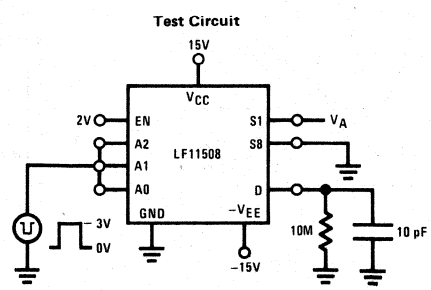






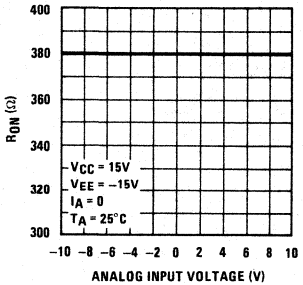




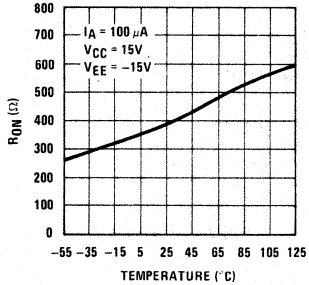


Typical Performance Characteristics

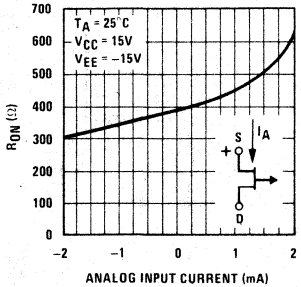
"ON" Resistance



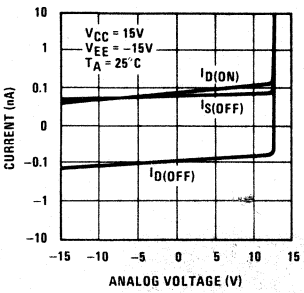
"ON" Resistance



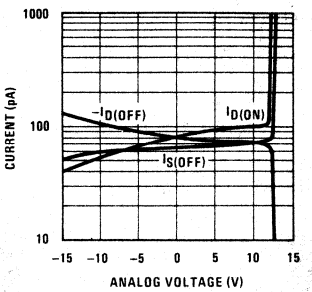
"ON" Resistance



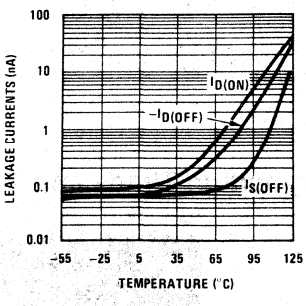
Switch Leakage Currents



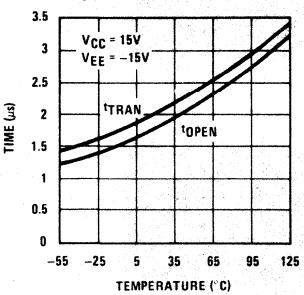
Switch Leakage Currents



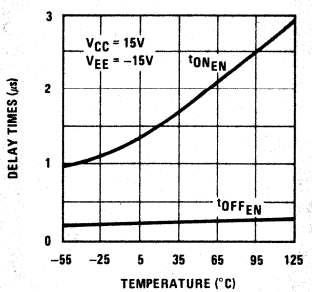
Switch Leakage Currents



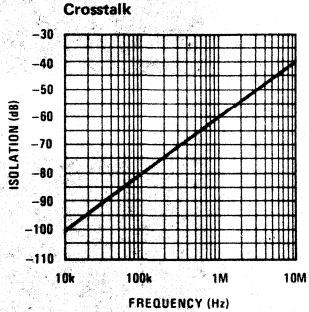
Switching Times (Figures 1 and 3)



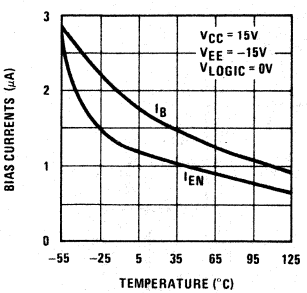
Enable Delay Times (Figure 2)



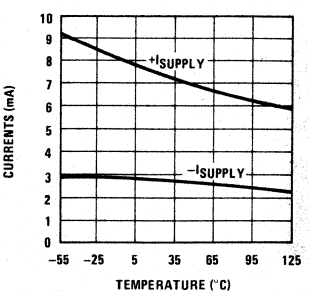
"OFF" Isolation and Crosstalk



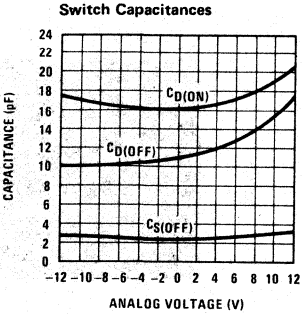
Bias Currents



Supply Currents



Switch Capacitances



Application Hints

The LF11508 series is an 8-channel analog multiplexer which allows the connection of a single load to 1 of 8 different analog inputs. These multiplexers incorporate JFETs in a switch configuration which insures a constant "ON" resistance over the analog voltage range of the device. Four TTL compatible inputs are provided; a 3-bit binary decode to select a particular channel and an enable input used as a package select. The switches operate with a break-before-make action preventing the temporary connection of 2 analog inputs during switching. Because these multiplexers are fabricated with the BI-FET process rather than CMOS, they do not require special handling.

The LF11509 series is a 4-channel differential multiplexer which allows two loads to be connected to 1 of 4 different pairs of analog inputs. The LF11509 series also has all the features of the LF11508.

ANALOG VOLTAGE AND CURRENT

The "ON" resistance, R_{ON}, of the analog switches is constant over a wide input range from positive (V_{CC}) supply to negative ($-V_{EE}$) supply.

The analog input should not exceed either positive or negative supply without limiting the current to less than 10 mA; otherwise the multiplexer may get damaged. For proper operation, however, the positive analog voltage should be kept equal to or less than $V_{CC} - 4V$ as this will increase the switch leakage in both "ON" and "OFF" state and it may also cause a false turn "ON" of a normally "OFF" switch. This limit applies over the full temperature range.

The maximum allowable switch "ON" voltage (the drop across the switch in the "ON" condition) is ±0.4V over temperature. If this number is to exceed the input current should be limited to 10 mA.

The "ON" resistance of the multiplexing switches varies slightly with analog current because they are JFETs running at 0V gate to source. The JFET characteristics shown in *Figure 4* indicates how R_{ON} tends to vary with current. A lower R_{ON} is possible when the source voltage is negative with respect to the drain voltage because the JFET becomes enhanced. Caution should be used when operating in this mode as this may forward-bias an internal transistor and cause high currents to flow in the switches. Thus, the drain voltage should never be greater than 0.4V positive with respect to the source voltage without limiting the drain current to less than 10 mA.

LEAKAGE CURRENTS

Leakage currents will remain within the specified value as long as the drain and source remain within the specified analog voltage range. As the switch terminals exceed the positive analog voltage range "ON" and "OFF" leakage currents increase. The "ON" leakage increases due to an internal clamp required by the switch structure. The "OFF" leakage increases because the gate to source reverse bias has been decreased to the point where the switch becomes active. Leakage currents vary slightly with analog voltage and will approximately double for every 10°C rise in temperature.

SWITCHING TIMES AND TRANSIENTS

These multiplexers operate with a break-before-make switch action. The turn off time is much faster than the turn on time to guarantee this feature over the full range of analog input voltage and temperature. Switching transients are introduced when a switch is turned "OFF". The amplitude of these transients may be reduced by increasing the load capacitance or decreasing the load resistance. The actual charge transfer in the transient may be reduced by operating on reduced power supplies. Examples of switching times and transients are shown in the typical characteristic curves. The enable function switching times are specified separately from switch-to-switch transition times and may be thought of as package-to-package transition times.

LOGIC INPUTS AND ENABLE INPUT

Switch selection in the LF11508 series is accomplished by using a 3-bit binary decode while the LF11509 series uses a 2-bit decode. These binary logic inputs are compatible with both TTL and CMOS logic voltage levels. The maximum positive voltage applied to these inputs may exceed V_{CC} but should not exceed $-V_{EE} + 36V$. The maximum negative voltage should not be less than 4V below ground as this will cause an internal device to zener and all the switches will turn "ON".

As shown in the schematic diagram, the logic low bias current will flow until the PNP input is raised above the 3 diode reference (≈ 2.1V). Above this voltage the input device becomes reverse biased and the input current drops to the leakage of the reverse biased junction (< 0.1 μA).

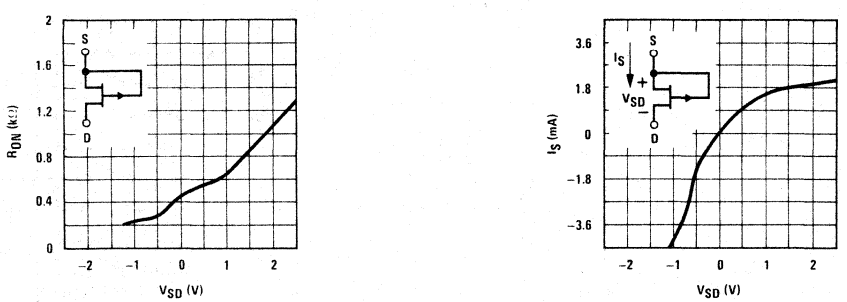


FIGURE 4. JFET Characteristics

Typical Applications

DATA ACQUISITION SYSTEM

A SIMPLIFIED SYSTEM DISCUSSION

Analog multiplexers (MUX) are usually used for multichannel Data Acquisition Units (DAU). *Figure 5* shows a system in which 8 different analog inputs are sampled and converted into digital words for further processing. The sample and hold circuit is optional, depending on input speed requirements and on A/D converter speed.

Parameters characterizing the system are:

System Channels: The number of multiplexer channels.

Accuracy: The conversion accuracy of each individual sample with the system operating at the throughput rate.

Speed or Throughput Rate: Number of samples/second/channel the system can handle.

For a discussion on system structure, addressing mode and processor interfacing, see application note AN-159.

A. ACCURACY CONSIDERATIONS

1. Multiplexer's Influence on System Accuracy *(Figure 6).*

   a. The error, (E), caused by the finite "ON" resistance, R_{ON}, of the multiplexing switches is given by:

   $$E(\%) = \frac{100}{1 + R_{IN}/(R_{ON} + R_S + \Delta R_{ON})}$$ where:

   R_{IN} = following stage input impedance

   ΔR_{ON} = "ON" resistance modulation which is negligible for JFET switches like the LF11508

   Example: Let R_{ON} = 450 Ω, ΔR_{ON} = 0, R_S = 0, T_A = 25°C and allowable E = 0.01% which is equivalent to 1/2 LSB in a 12-bit system:

   $$R_{IN}\Big|_{min} = \frac{R_{ON}\,(100-E)}{E} = 4.5\ M\Omega$$

   Note that if temperature effects are included, some gain (or full scale) drift will occur; but effects on linearity are small.

   b. Multiplexer settling time (t_s):

   $t_{s(ON)}$: is the time required for the MUX output to settle within a predetermined accuracy, as shown in Table I.

   C_S *(Figure 6):* MUX output capacitance + following stage input capacitance + any stray capacitance at this node.

TABLE I.

ERROR %	BITS	$t_{s(ON)}$ TO 1/2 LSB
0.2	8	6.2t
0.05	10	7.6t
0.01	12	9t
0.0008	16	11.8t

$t = C_S\,(R_{ON} + R_S) \| R_{IN}$

$t_{s(OFF)}$: is the time it takes to discharge C_S within a tolerable error. The "OFF" settling time should be taken into account for bipolar inputs where its effects will appear as a worse case doubling of the $t_{s(ON)}$.

2. Sample and Hold Influence on System Accuracy

   The sample and hold, if used, also introduces errors into the system accuracy due to:

   - Offset voltage of sample and hold
   - Droop rate in the Hold mode
   - T_A: Aperture time or time delay between the time of a digital Hold command and the actual Hold occurance
   - Taq: Acquisition time or time it takes to acquire an analog input and settle within a predetermined error band
   - Hold step: Error created during the Sample to Hold mode caused by an undesirable charge injected into the Hold capacitor C_h.

   For more details on sample and hold errors, see the LF198/LF298/LF398 data sheet.

3. A/D Converter Influence on System Accuracy
   The "accuracy" of the A/D converter is the best possible system accuracy. In most data acquisition systems, the A/D converter is the most expensive single component, so its error will often dominate system error. Care should be taken that MUX, S/H and input source errors do not exceed system error requirements when *added* to A/D errors. For instance, if an 8-bit accuracy system is desired and an 8-bit A/D converter is used, the accuracy of the MUX and S/H should be far better than 8 bits.

For details on A/D converter specifications, see AN-156.

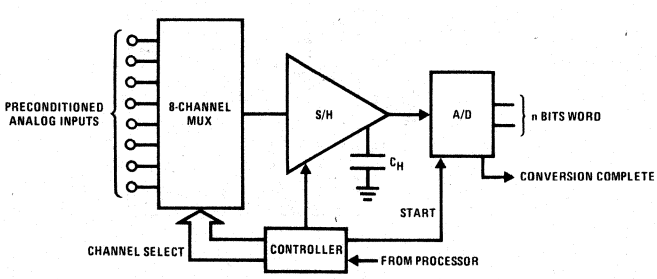


FIGURE 5. Random-Addressed, Multiplexed DAU

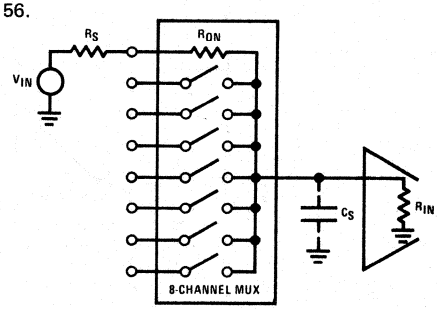


FIGURE 6. 8-Channel MUX

Typical Applications (Continued)

B. SPEED CONSIDERATIONS

In the system of *Figure 5* with the S/H omitted, if n-bit accuracy is desired, the change of the analog input voltage should be less than ±1/2 LSB over the A/D conversion time T_C. In other words, the analog input slew rate, (rate of change of input voltage), will cause a slew-induced error and its magnitude, with respect to the total system error, will depend on the particular application.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{\pm 1/2\ LSB}{T_C} = \frac{V_{FS}}{2^n \times T_C}$$

where V_{FS} is the full scale voltage of the A/D. Note that slew induced errors are not affected by the MUX switch time since we can let the unit settle before starting conversion.

Example: Let T_C = 40 μs (MM4357), V_{FS} = 10V and n = 8.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{1\ mV}{\mu s}$$

which is a very small number. A 10 Vp-p sine wave of a frequency greater than 32 Hz will have higher slew rate than this. The maximum throughput rate of the above 8-channel system would be calculated using both the A/D conversion time and the sum of MUX switch "ON" time and settling time, i.e.:

$$\text{Th. R}\Big|_{max} = \frac{1}{8\ (T_C + T_{MUX})} = 3\text{k samples/sec/channel}$$

$$T_{MUX} = T_{ON} + T_{S(ON)}$$

Also notice that Nyquist sampling criteria would allow each channel to have a signal bandwidth of 1.5 kHz max, while the slew limit dictates a maximum frequency of 32 Hz. If the input signal has a peak-to-peak voltage less than 10V, the allowable maximum input frequency can be calculated by:

$$f_{MAX} = \frac{(\text{Slew Rate})_{max}}{\pi\ V_{p\text{-}p}}$$

On the other hand, if the input voltage is not band-limited a low pass filter with an attenuation of 30 dB or better at 1.5 kHz, should be connected in front of the MUX.

1. Improving System Speed with a Sample and Hold

The system speed can be improved by using the S/H shown in *Figure 5*. This allows a much greater rate of change of V_{IN}.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{V_{FS}}{2^n \times T_A}$$

where T_A is the aperture time of the S/H. This represents an input slew rate improvement by a factor: T_C/T_A. Here again, the slew rate error is not affected by the acquisition time of the Sample and Hold since conversion will start after the S/H has settled. *An important thing to notice is that the sample and hold errors will add to the total system error budget; therefore, the inequality of the $\Delta V_{IN}/\Delta t$ expression should become more stringent.*

Example: T_C = 40 μs, T_A=0.5 μs, n = 8: T_C/T_A = 80

So the use of a S/H allows a speed improvement by nearly two orders of magnitude.

The maximum throughput rate can be calculated by:

$$\text{Th. R}\Big|_{max} = \frac{1}{8\ (T_A + T_{aq} + T_C)}$$

Notice that T_{MUX} does not affect the $\Delta V_{IN}/\Delta t$ expression *nor the throughput rate* of the system since it may be switched and settled while the Sample and Hold is in the Hold mode. This is true, provided that: $T_{MUX} < T_A + T_C$.

C. SYSTEM EXAMPLE *(Figure 7)*

The LF398 S/H with a 1000 pF hold capacitor, has an acquisition time of 4 μs to 0.1% (1/4 LSB error for 8 bits) and an aperture time of less than 200 μs. On the other hand, after the hold command, the output will settle to ±0.05 mV in 1 μs. This, together with the acquisition time, introduces approximately a ±1/4 LSB error. Allowing another 1/4 LSB error for hold step and gain non-linearity, the maximum slew error ($\Delta V_{IN}/\Delta t$) should not exceed 1/4 LSB or:

$$\frac{\Delta V_{IN}}{\Delta t} \leq \frac{1}{4} \times \frac{1}{256} \times \frac{1}{T_A} \approx 5\ mV/\mu s$$

(which is the maximum slew rate of a 5 V peak sine wave. Also notice that, due to the above input slew restrictions, the analog delay caused by the finite BW of the S/H and the digital delay caused by the response time of the controller will be negligible. The maximum throughput rate of the system is:

$$\text{Th. R}\Big|_{max} = \frac{1}{8\ (5 + 40)\ 10^{-6}} = 2800\ \text{samples/sec/ch.}$$

If the system speed requirements are relaxed, but the A/D converter is still too slow, then an inexpensive S/H can be built by using just a capacitor and a low cost FET input op amp as shown in *Figure 8.*

Typical Applications (Continued)

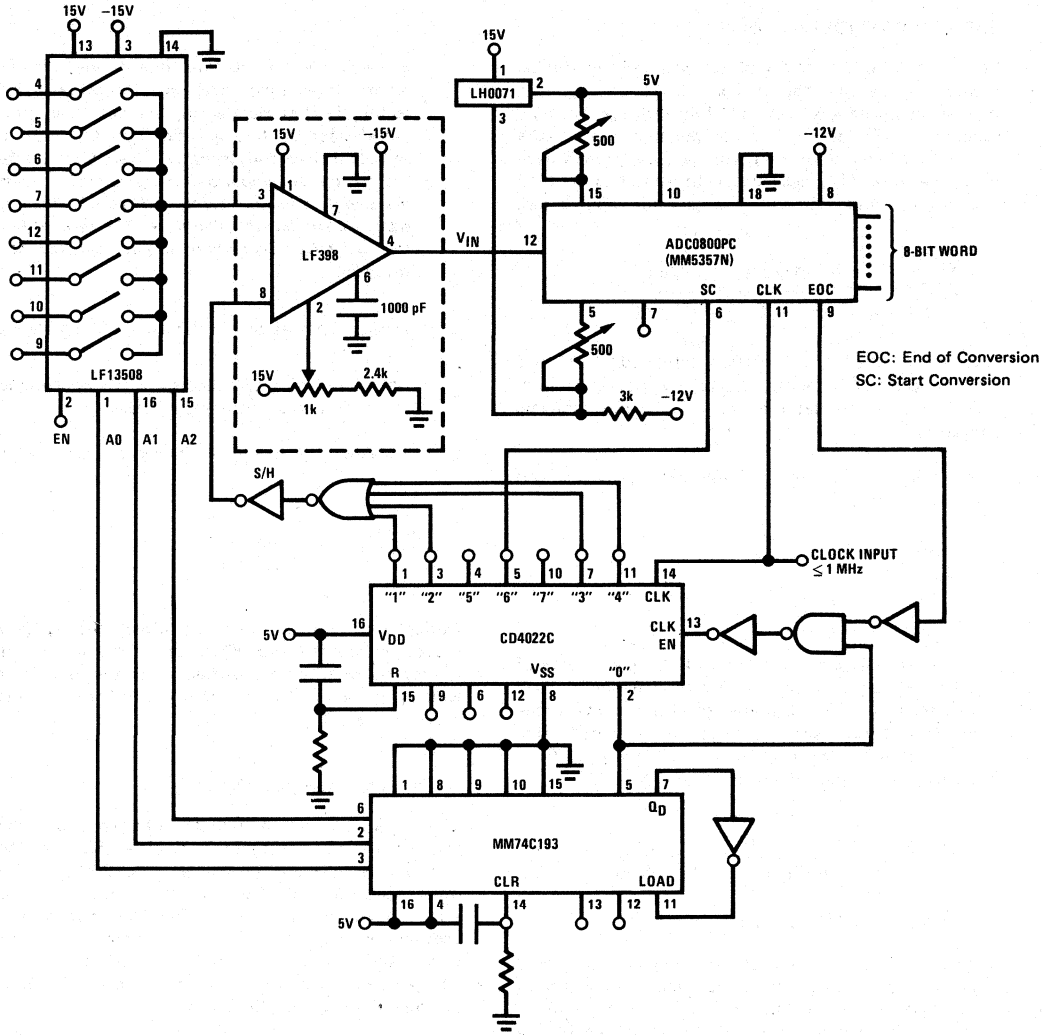


FIGURE 7a. Sequentially Multiplexed DAU with Sample and Hold

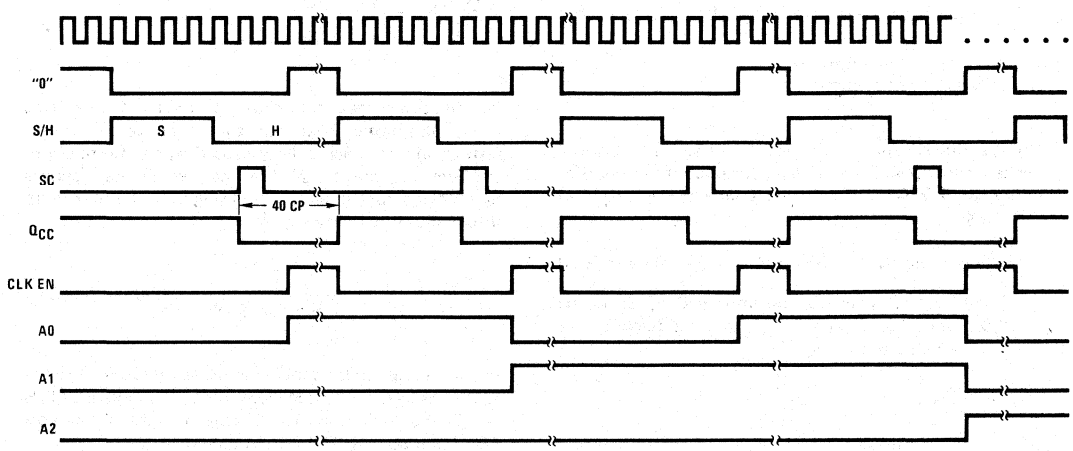


FIGURE 7b. Timing Diagram

Typical Applications (Continued)

D. DOUBLING THE SYSTEM CHANNEL CAPABILITY

This is done in two different ways. First, we can use second level multiplexing with speed benefits, as shown in *Figure 9*. A fast 2-channel multiplexer, made by the dual analog switch AM182, accepts the outputs of each 8-channel MUX, LF13508, and then feeds them sequentially into an 8-bit successive approximation A/D converter. With this technique, the throughput rate of the system can again be made independent of the the LF13508 speed. Looking at the timing diagram, when the A/D converter converts the analog value of an upper multiplexer channel, we switch channels in the lower multiplexer for the next conversion. This can be done provided that:

$$T_{MUX} \leq T_C + 1\ CP$$

The LF356 connected as unity gain buffers are used because of the low input impedance of the A/D; they are connected between multiplexers for speed optimization. With a maximum clock frequency of 4.5 MHz:

$$\text{Th. } R = \frac{10^6}{16 \times 2} = 31.25\text{k samples/sec/channel}$$

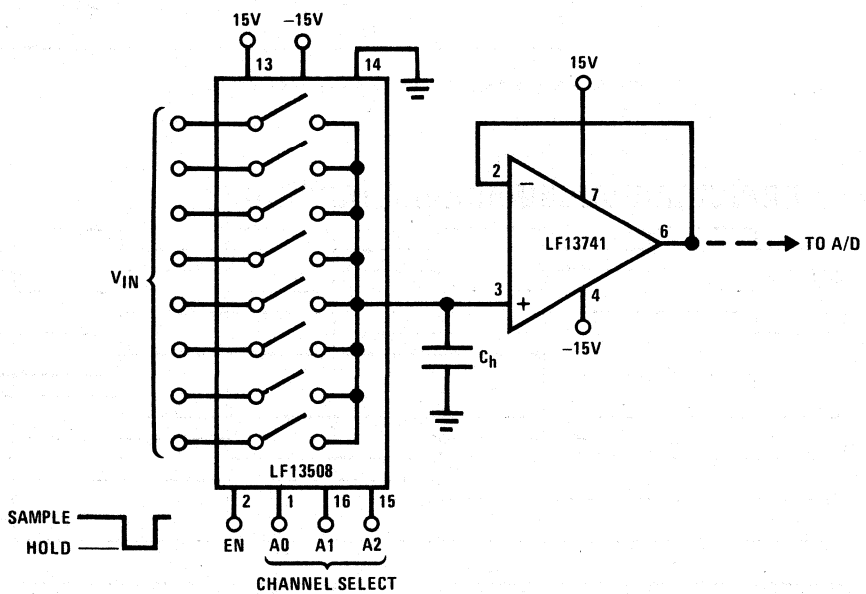
and

$$\left|\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{10}{256} \times \frac{1}{2\ \mu s} = 19.5\ mV/\mu s \text{ for } 10V_{FS}$$

An alternate way to increase the system channel is shown in *Figure 10*, where the enable pins are used to disable one MUX while the other is sampling. With this method, many 8-channel multiplexers can be connected, but the parasitic capacitance at the common output node will keep increasing and will eventually degrade the settling time, $t_{s(ON)}$. Also, the MUX speed will now affect the system throughput. If, for instance, this method was used instead of second level multiplexing, the system of *Figure 9* will lose half of its speed. If, however, speed is not the prime system requirement, the approach of *Figure 10* is more cost effective.

E. DIFFERENTIAL INPUT SYSTEMS

Systems operating in industrial environments may require an instrumentation amplifier to separate the desired analog signal from any common-mode signal present. The LF11509 was designed to provide 4 pairs of differential input signals to the input of an instrumentation amplifier for further process. A 4-channel preconditioning circuit is shown in *Figure 11* and a complete system is shown in *Figure 12*.



- The acquisition time, T_A, of the Sample and Hold depends upon: R_{ON}, I_{DSS} of switches, Z_{OUT} of switches
- $I_{DSS} \cong 1.5$ mA, $Z_{OUT} = 40\ k\Omega$
- $V_{IN} = 10V$, $C_h = 1000$ pF, $T_A = 20\ \mu s$ to 0.1%
- Error created by charge injection during Hold mode: $\Delta V_E \simeq 10\ pF\ (14.5V - V_{IN})/C_h$

FIGURE 8. Inexpensive Sample and Hold

Typical Applications (Continued)

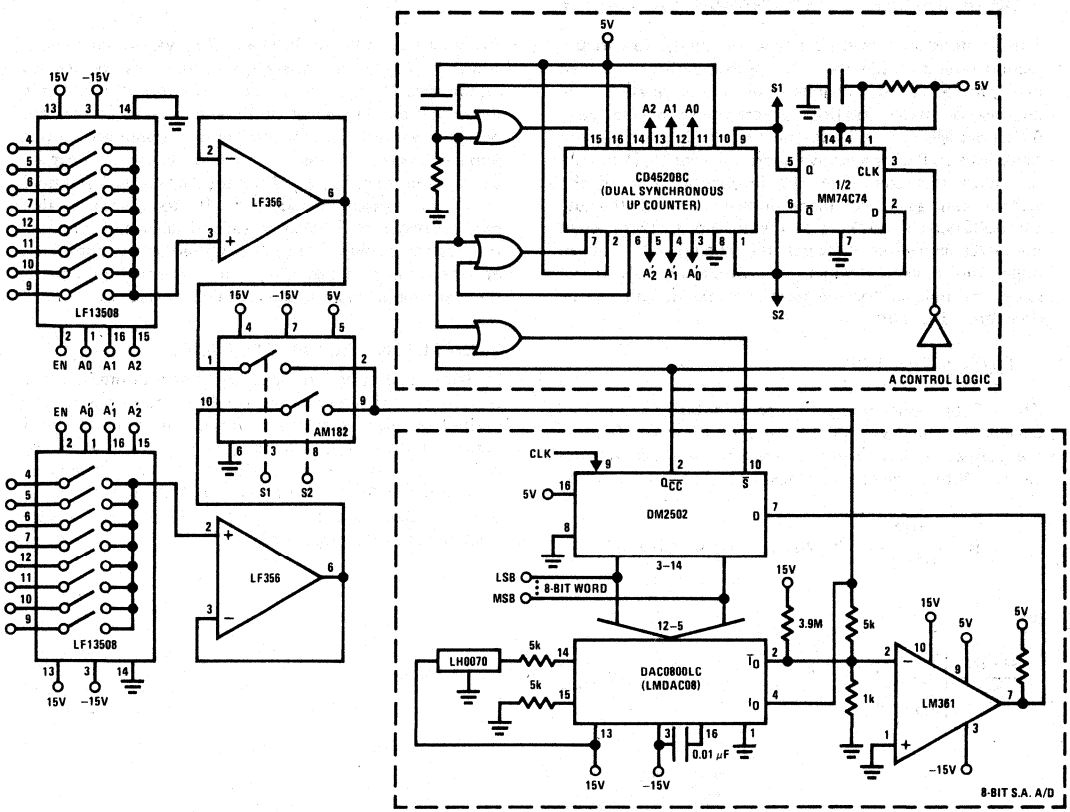


FIGURE 9a. A Fast 16-Channel DAU with Second Level Multiplexing

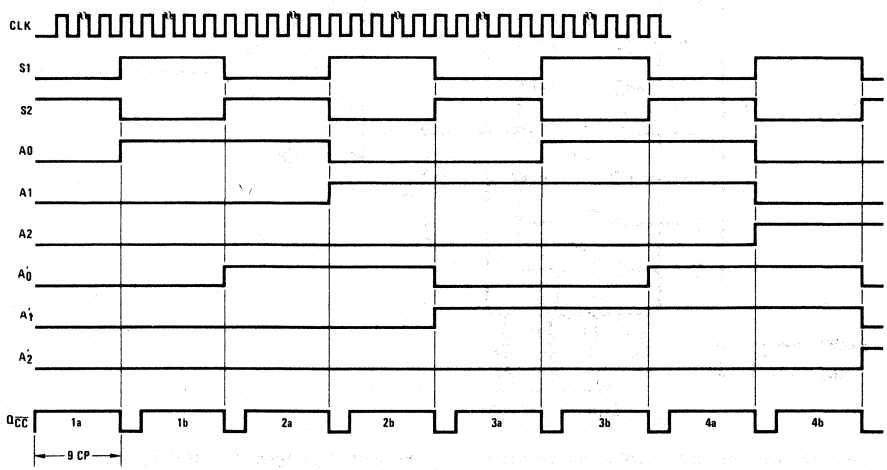


FIGURE 9b. Timing Diagram

Typical Applications (Continued)

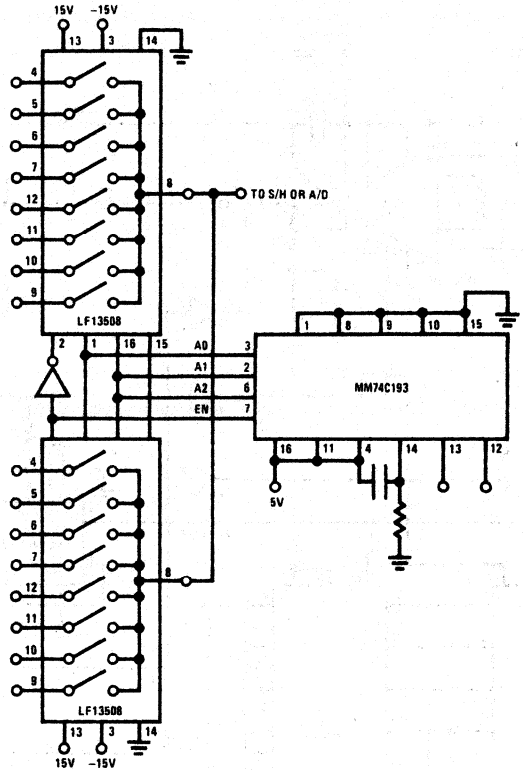
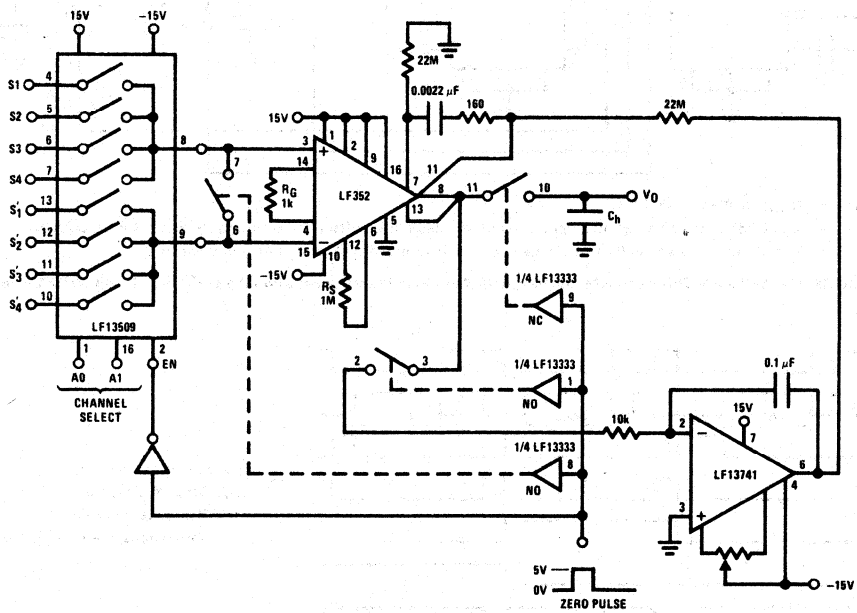


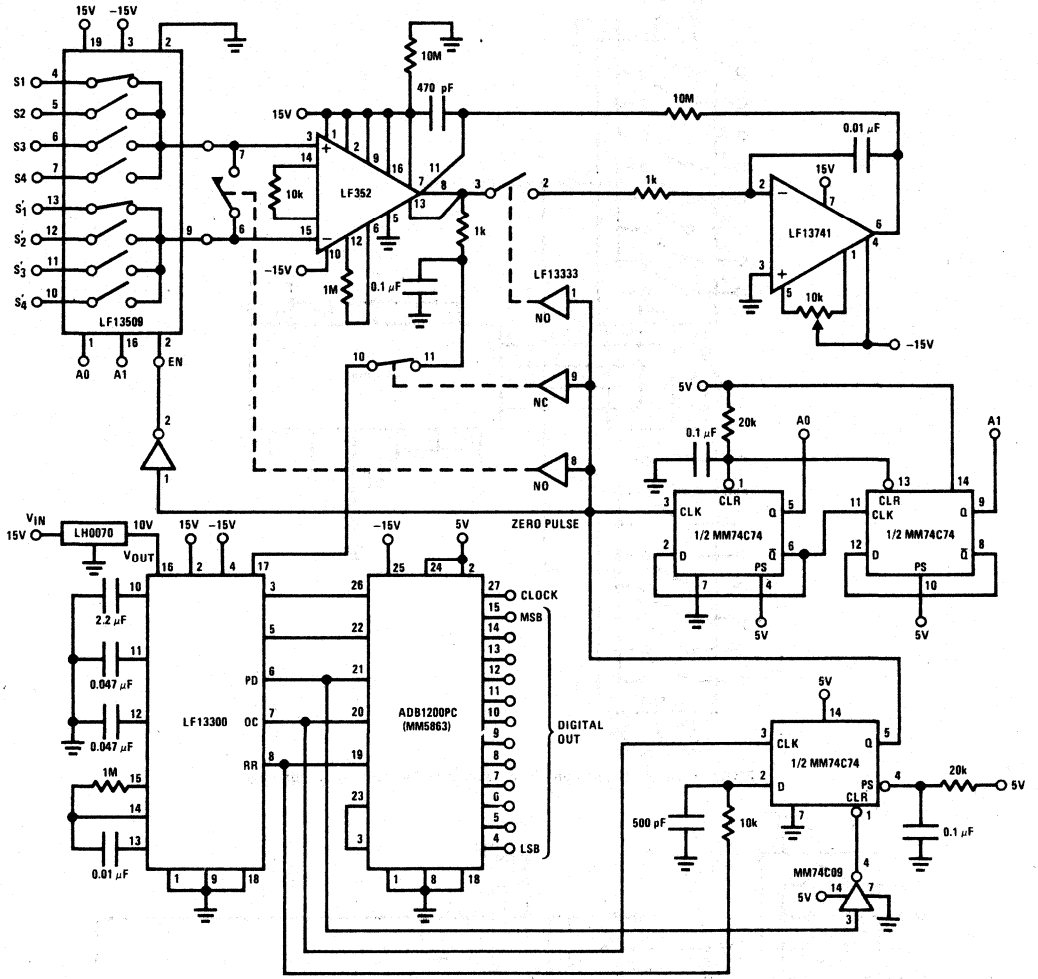
FIGURE 10. A 16-Channel Multiplexer with Sequential Multiplexing



- Differential multiplexer disabled during auto zeroing
- Minimum zeroing pulse width will depend upon the integrator R1C
- This scheme provides input offset adjust especially useful with high gain connections. The device, LF352, provides pins for output offset adjust. For more details, see LF352 data sheet.

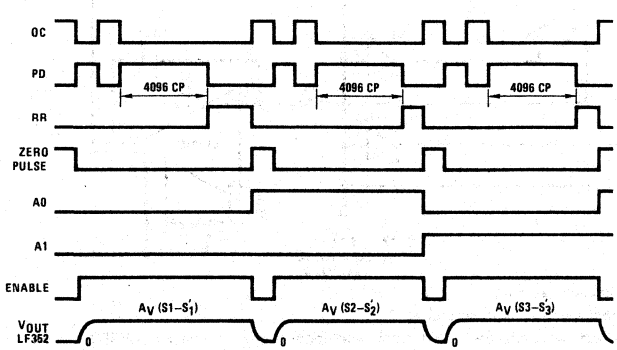
FIGURE 11. 4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier

Typical Applications (Continued)



- f_{CLOCK} max = 200 kHz
- The LF352 instrumentation amplifier is auto zeroed during offset correction cycle of the LF13300 A/D
- The system accuracy will mostly depend on the instrumentation amplifier gain linearity

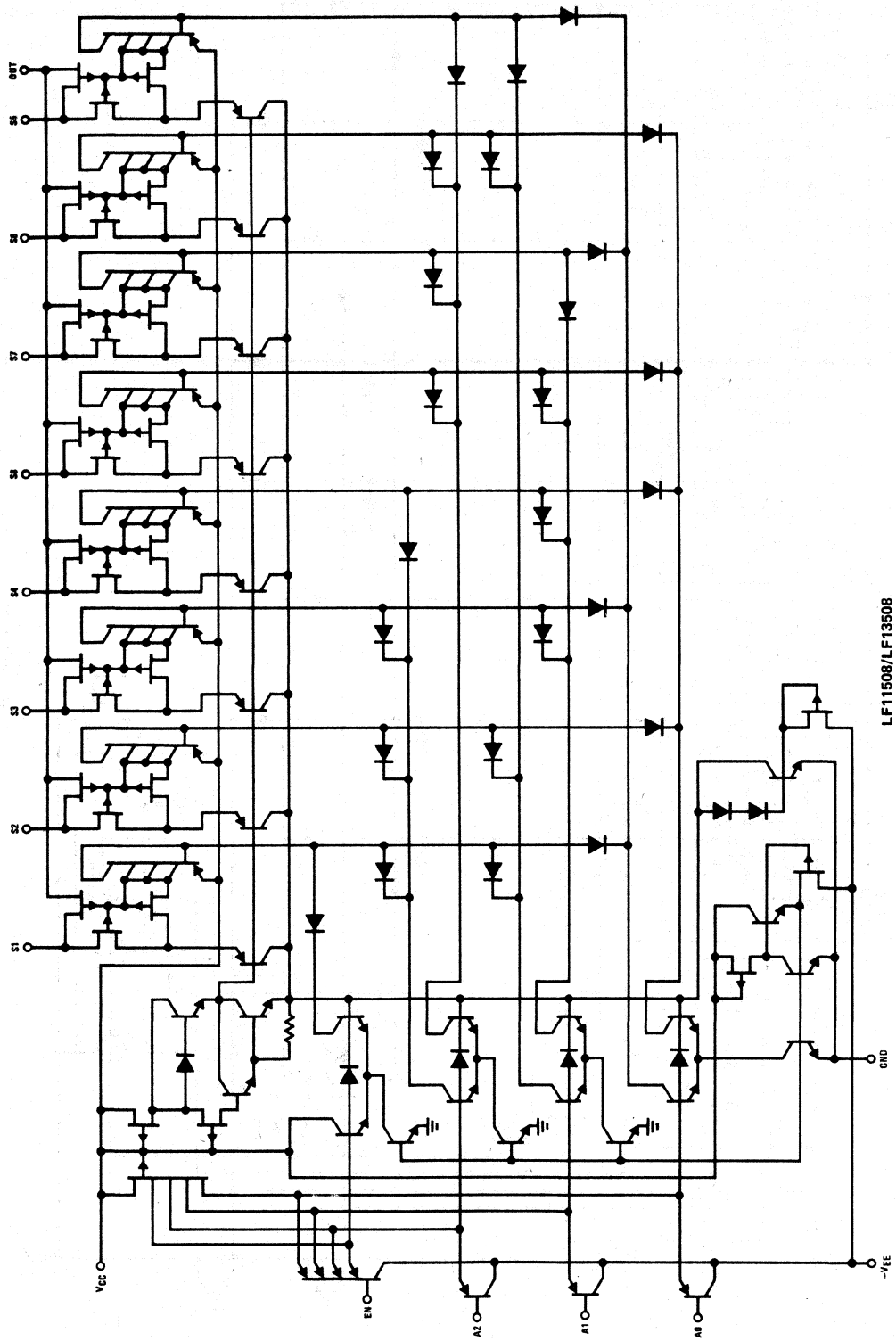
FIGURE 12a. 4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier and 12-Bit A/D Converter



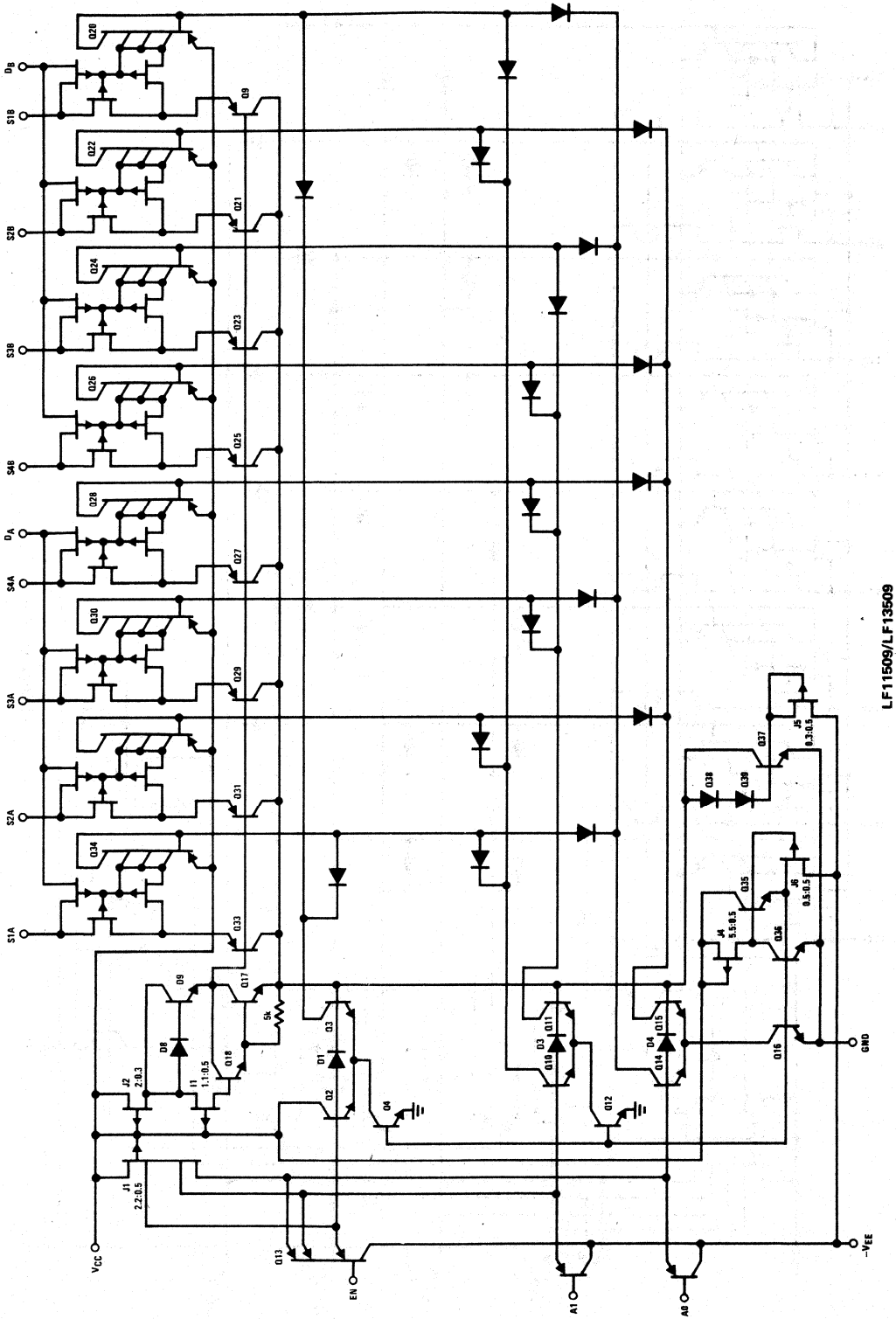
PD: Polarity Detection
OC: Offset Correction
RR: Ramp Reference
For more details, see LF13300 data sheet

FIGURE 12b. System Timing Diagram for Differential MUX

Schematic Diagrams



Schematic Diagrams (Continued)



Section 11

Sample and Hold

11

Section Contents

National Semiconductor

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample and Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample and hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

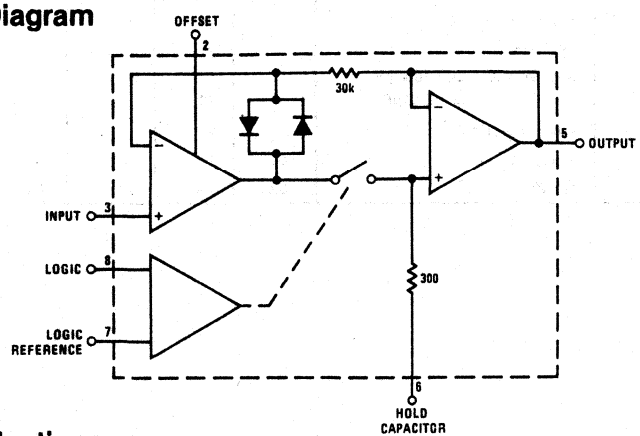
Features

- Operates from ±5V to ±18V supplies
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

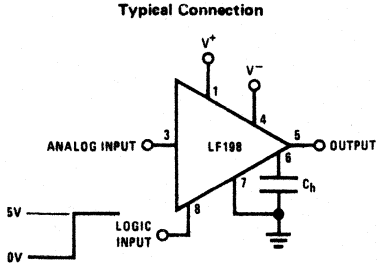
An "A" version is available with tightened electrical specifications.

Functional Diagram

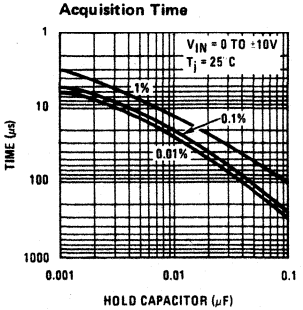


Typical Applications

Typical Connection



Acquisition Time



Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 1)	500 mW
Operating Ambient Temperature Range	
LF198/LF198A	−55°C to +125°C
LF298	−25°C to +85°C
LF398/LF398A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 2)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LF198/LF298			LF398			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4			4		μs
	$C_h = 0.01\mu F$		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Electrical Characteristics (Continued) (Note 3)

PARAMETER	CONDITIONS	LF198A			LF398A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	1		2	2	mV
	Full Temperature Range			2			3	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	25	nA
	Full Temperature Range			75			50	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.005	%
	Full Temperature Range			0.01			0.01	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		86	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	1		0.5	1	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4	6		4	6	μs
	$C_h = 0.01\mu F$		20	25		20	25	μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198/LF198A is 150°C, for the LF298, 115°C, and for the LF398/LF398A, 100°C. When operating at elevated ambient temperature, the power dissipation must be derated based on a thermal resistance (Θ_{jA}) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10\ k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

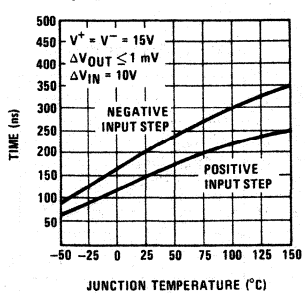
Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters guaranteed over a supply voltage range of ±5 to ±18V.

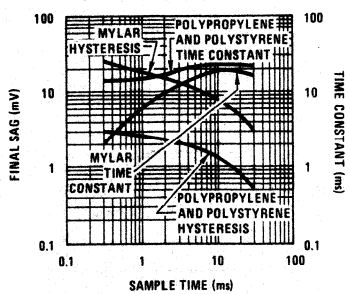
Typical Performance Characteristics

Aperture Time*

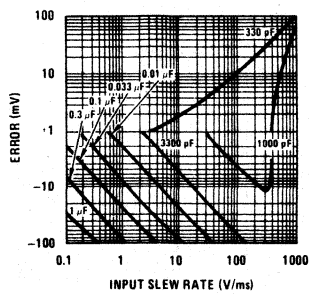


*See Definition of Terms

Capacitor Hysteresis

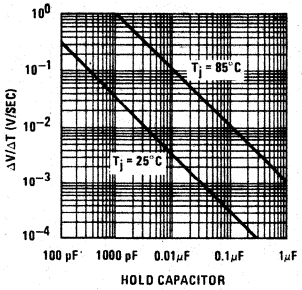


Dynamic Sampling Error

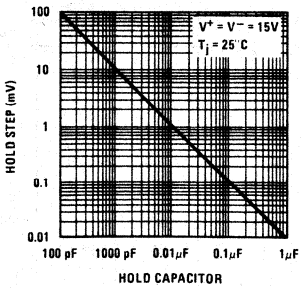


Typical Performance Characteristics (Continued)

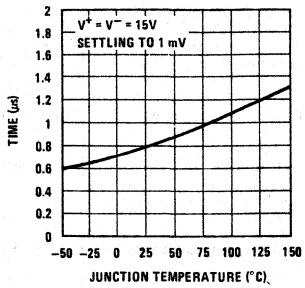
Output Droop Rate



Hold Step

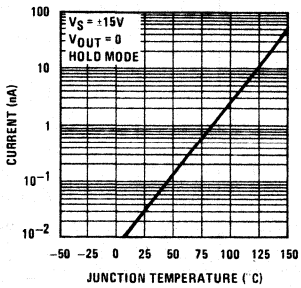


"Hold" Settling Time*

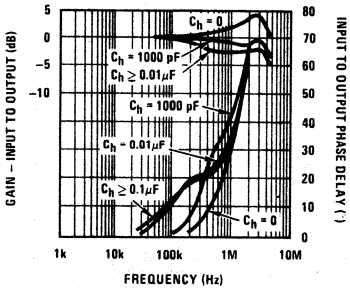


*See definition

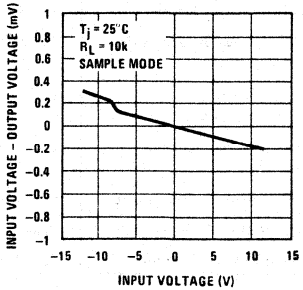
Leakage Current into Hold Capacitor



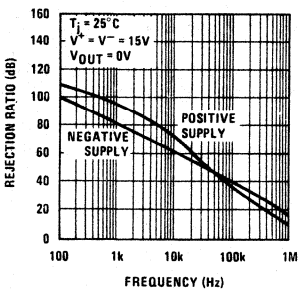
Phase and Gain (Input to Output, Small Signal)



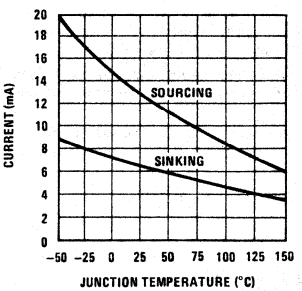
Gain Error



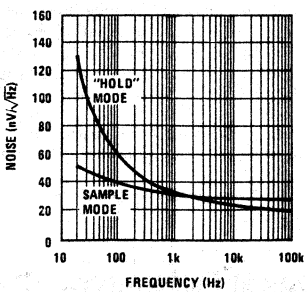
Power Supply Rejection



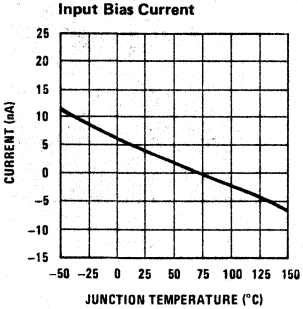
Output Short Circuit Current



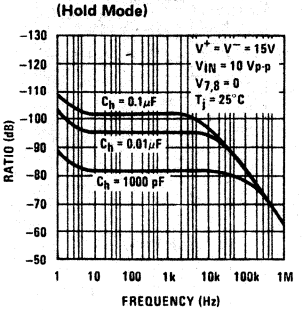
Output Noise



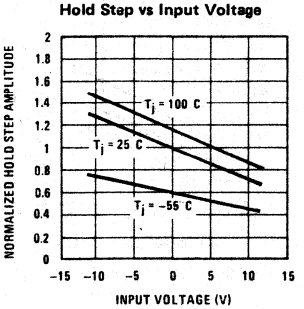
Input Bias Current



Feedthrough Rejection Ratio (Hold Mode)



Hold Step vs Input Voltage



Application Hints

Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with $> 1\%$ hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. "NPO" or "COG" capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see the curve labeled dielectric absorption error vs sample time. The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10–50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01μF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

Logic Rise Time

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/μs.

Sampling Dynamic Signals

Sample error due to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1μs)(0.6V/μs) = 60 mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs)(0.6 V/μs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

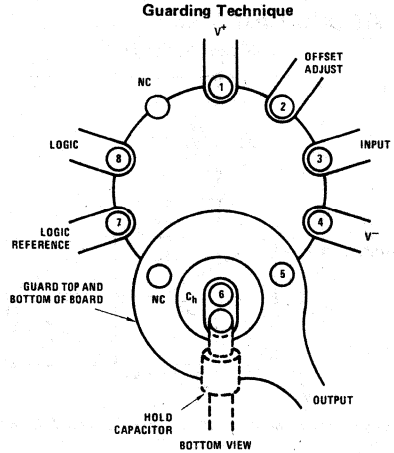
A curve labeled Aperture Time has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, Hold Settling Time indicates the time required for the output to settle to 1 mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

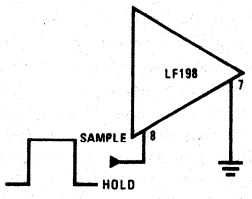
Guarding Technique



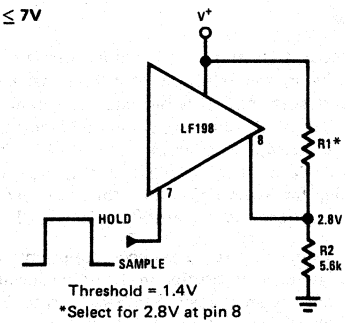
Use 10-pin layout. Guard around C_h is tied to output.

Logic Input Configurations

TTL & CMOS
$3V \leq V_L$ (Hi State) $\leq 7V$

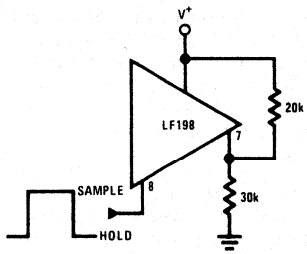


Threshold = 1.4V

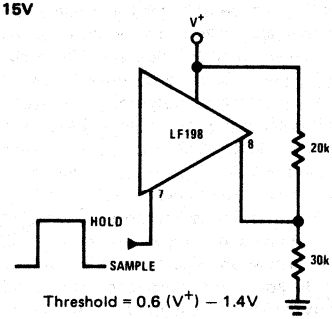


Threshold = 1.4V
*Select for 2.8V at pin 8

CMOS
$7V \leq V_L$ (Hi State) $\leq 15V$

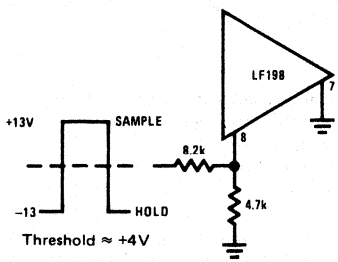


Threshold = 0.6 (V^+) + 1.4V

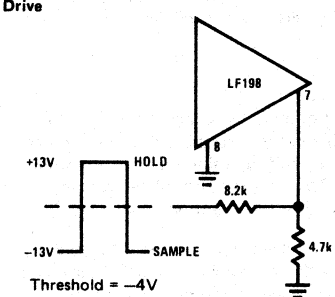


Threshold = 0.6 (V^+) − 1.4V

Op Amp Drive



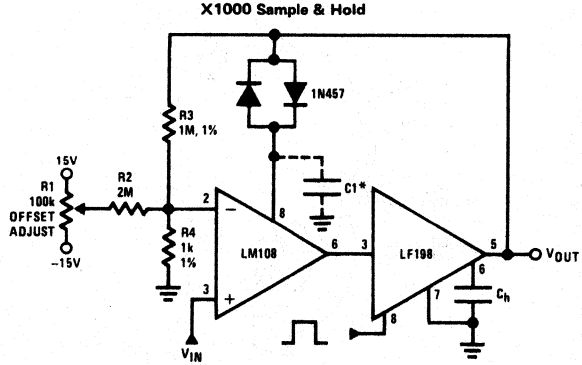
Threshold ≈ +4V



Threshold = −4V

Typical Applications (Continued)

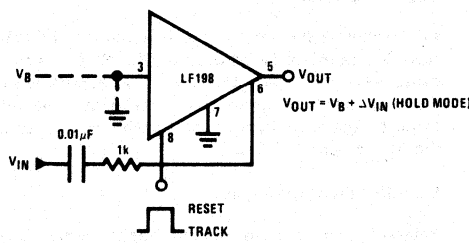
X1000 Sample & Hold



*For lower gains, the LM108 must be frequency compensated

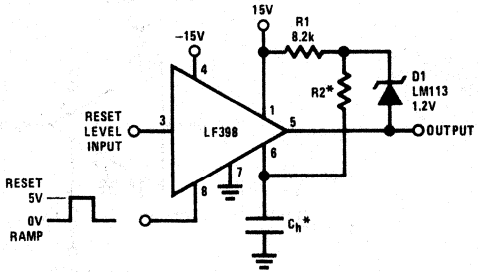
Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit
(Output Follows Input in Hold Mode)



Typical Applications (Continued)

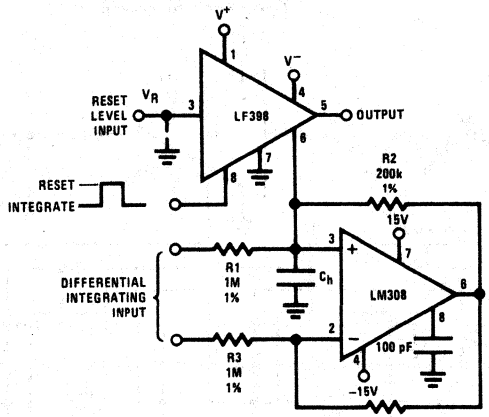
Ramp Generator with Variable Reset Level



*Select for ramp rate $R \geq 10k$

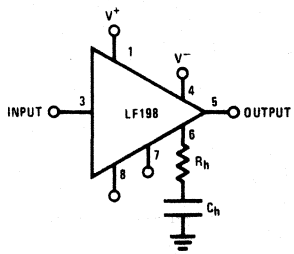
$$\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)(C_h)}$$

Integrator with Programmable Reset Level



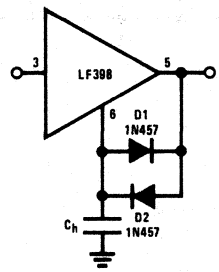
$$V_{OUT}\ (\text{Hold Mode}) = \left[\frac{1}{(R1)(C_h)}\int_0^t V_{IN}\,dt\right] + \left[V_R\right]$$

Output Holds at Average of Sampled Input

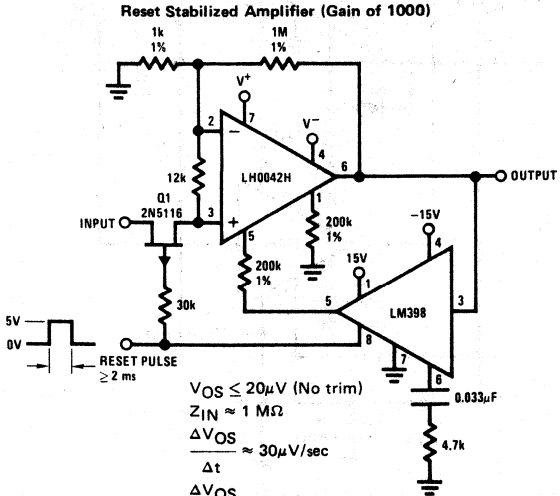


$$\text{Select } (R_h)(C_h) >> \frac{1}{2\pi f_{IN}\ (\text{Min})}$$

Increased Slew Current



Reset Stabilized Amplifier (Gain of 1000)



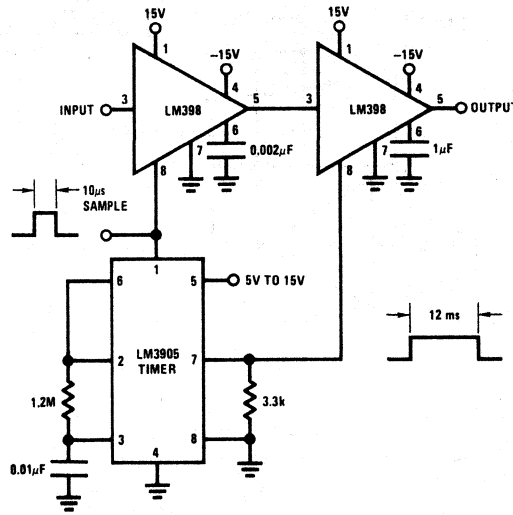
$V_{OS} \leq 20\mu V$ (No trim)

$Z_{IN} \approx 1\ M\Omega$

$$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/\text{sec}$$

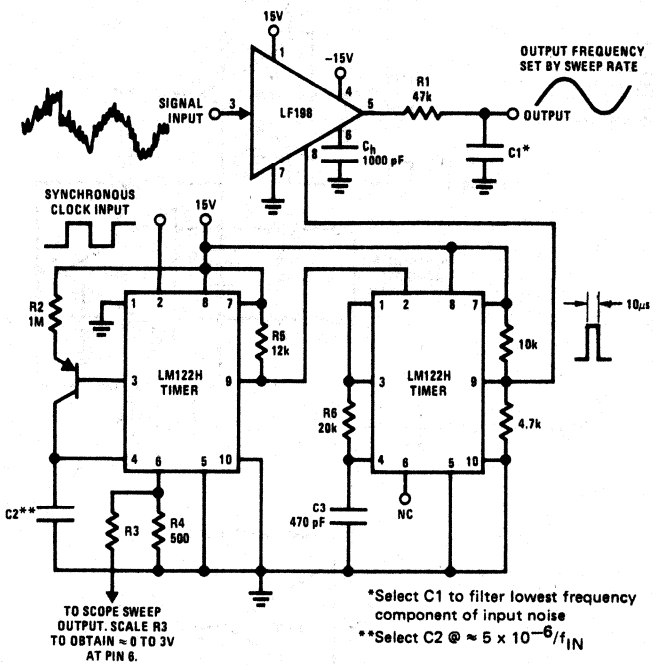
$$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/°C$$

Fast Acquisition, Low Droop Sample & Hold



Typical Applications (Continued)

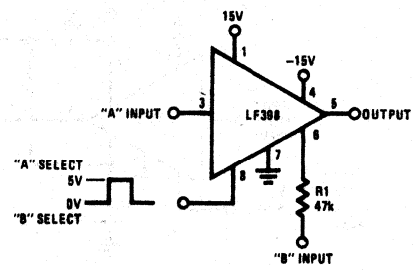
Synchronous Correlator for Recovering Signals Below Noise Level



*Select C1 to filter lowest frequency component of input noise

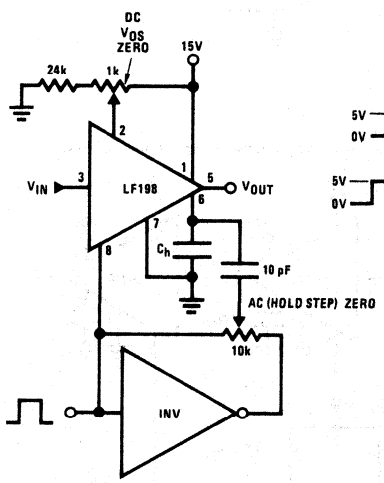
**Select C2 @ $\approx 5 \times 10^{-6}/f_{IN}$

2-Channel Switch

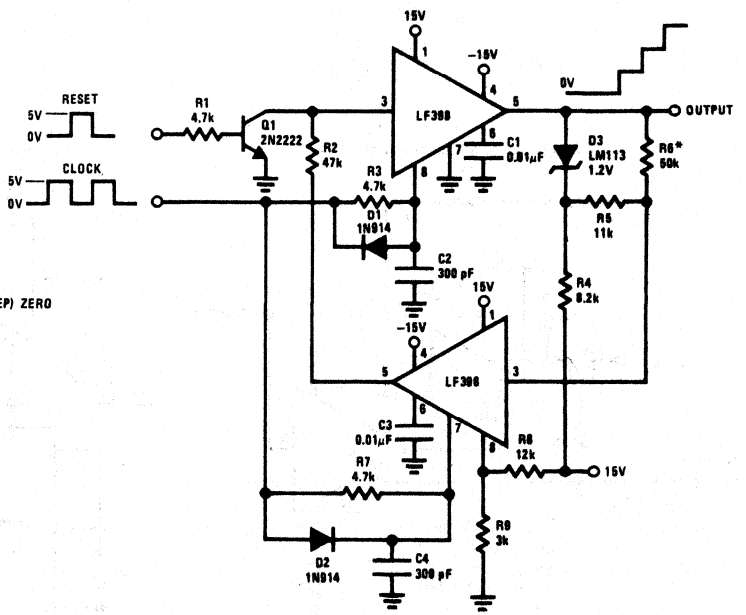


	A	B
Gain	1 ±0.02%	1 ±0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≃1 MHz	≈400 kHz
Crosstalk @ 1 kHz	−90 dB	−90 dB
Offset	≤ 6 mV	≤ 75 mV

DC & AC Zeroing



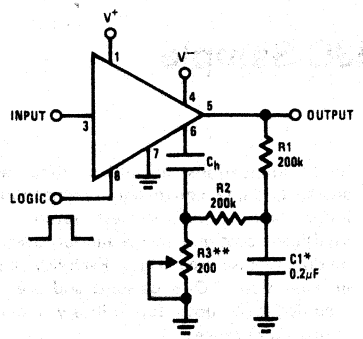
Staircase Generator



*Select for step height
50k → ≃ 1V Step

Typical Applications (Continued)

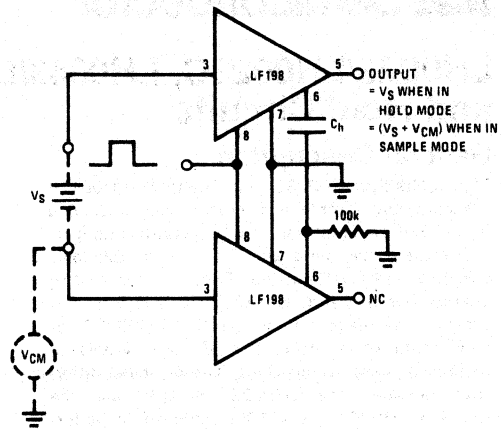
Capacitor Hysteresis Compensation



*Select for time constant C1 = $\frac{T}{100k}$

**Adjust for amplitude

Differential Hold



Definition of Terms

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

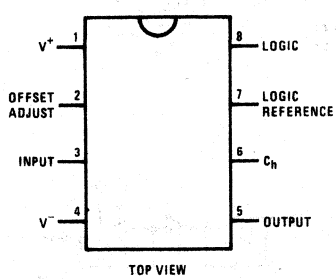
Hold Settling Time: The time required for the output to settle within 1 mV of final value after the "hold" logic command.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

Connection Diagrams

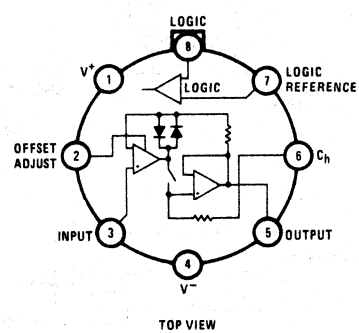
Dual-In-Line Package



TOP VIEW

Order Number LF398N or LF398AN
See NS Package N08A

Metal Can Package



TOP VIEW

Order Number LF198H, LF298H, LF398H, LF198AH or LF398AH
See NS Package H08C

National Semiconductor

LH0023/LH0023C, LH0043/LH0043C Sample and Hold Circuits

General Description

The LH0023/LH0023C and LH0043/LH0043C are complete sample and hold circuits including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. They are designed to operate from standard ±15V DC supplies, but provision is made on the LH0023/LH0023C for connection of a separate +5V logic supply in minimum noise applications. The principal difference between the LH0023/LH0023C and the LH0043/LH0043C is a 10:1 trade-off in performance on sample accuracy vs sample acquisition time. Devices are pin compatible except that TTL logic is inverted between the two types.

The LH0023/LH0023C and LH0043/LH0043C are ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. They offer significant cost and size reduction over equivalent module or discrete designs. Each device is available in a hermetic TO-8 package and are completely specified over both full military and instrument temperature ranges.

The LH0023 and LH0043 are specified for operation over the -55°C to +125°C military temperature range. The LH0023C and LH0043C are specified for operation over the -25°C to +85°C temperature range.

Features

LH0023/LH0023C

- Sample accuracy—0.01% max
- Hold drift rate—0.5 mV/sec typ
- Sample acquisition time—100 μs max for 20V
- Aperture time—150 ns typ
- Wide analog range—±10V min
- Logic input—TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

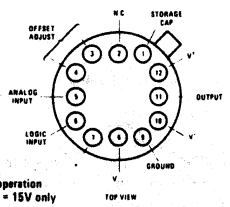
Features

LH0043/LH0043C

- Sample acquisition time—15 μs max for 20V
  4 μs typ for 5V
- Aperture time—20 nS typ
- Hold drift rate—1 mV/sec typ
- Sample accuracy—0.1% max
- Wide analog range—±10V min
- Logic input—TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

Block and Connection Diagrams

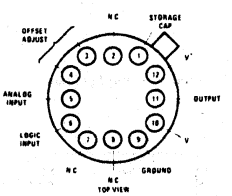
LH0023/LH0023C

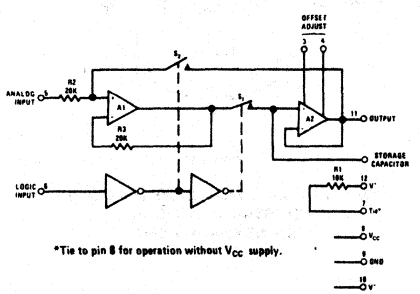


*Tie for operation with V^+ = 15V only

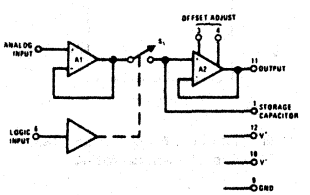
Order Number LH0023G or LH0023CG or LH0043G or LH0043CG
See Package H12B

LH0043/LH0043C





*Tie to pin 8 for operation without V_{CC} supply.



Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)		±20V
Logic Supply Voltage (V_{CC})	LH0023, LH0023C	+7.0V
Logic Input Voltage (V_6)		+5.5V
Analog Input Voltage (V_5)		±15V
Power Dissipation		See graph
Output Short Circuit Duration		Continuous
Operating Temperature Range	LH0023, LH0043	−55°C to +125°C
	LH0023C, LH0043C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Soldering (10 sec)		300°C

Electrical Characteristics LH0023/LH0023C (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0023			LH0023C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Sample (Logic "1") Input Voltage	V_{CC} = 4.5V	2.0			2.0			V
Sample (Logic "1") Input Current	V_6 = 2.4V, V_{CC} = 5.5V			5.0			5.0	μA
Hold (Logic "0") Input Voltage	V_{CC} = 4.5V			0.8			0.8	V
Hold (Logic "0") Input Current	V_6 = 0.4V, V_{CC} = 5.5V			0.5			0.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current – I_{10}	V_5 = 0V, V_6 = 2V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_{12}	V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_8	V_8 = 5.0V, V_5 = 0		1.0	1.6		1.0	1.6	mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.002	0.01		0.002	0.02	%
DC Input Resistance	Sample Mode	500	1000		300	1000		kΩ
	Hold Mode	20	25		20	25		kΩ
Input Current – I_5	Sample Mode		0.2	1.0		0.3	1.5	μA
Input Capacitance			3.0			3.0		pF
Leakage Current – pin 1	V_5 = ±10V; V_{11} = ±10V, T_A = 25°C		10.0	200		20.0	500	pA
	V_5 = ±10V; V_{11} = ±10V			2.5			2	nA
Drift Rate	V_{OUT} = ±5V, C_S = 0.01 μF, T_A = 25°C		0.5			0.5		mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_A = 25°C		1.0	20		2.0	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF			0.25			0.2	mV/ms
Aperture Time			150			150		ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.01 μF		50	100		50	100	μs
Output Amplifier Slew Rate		1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	$R_S \leq$ 10k, V_5 = 0V, V_6 = 0V			±20			±20	mV
Analog Voltage Output Range	$R_L \geq$ 1k, T_A = 25°C	±10	±11		±10	±11		V
	$R_L \geq$ 2k	±10	±12		±10	±12		V

Note 1: Unless otherwise noted, these specifications apply for V^+ = +15V, V_{CC} = +5V, V^- = −15V, pin 9 grounded, a 0.01μF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0023, and 25°C to +85°C for the LH0023C. All typical values are for T_A = 25°C.

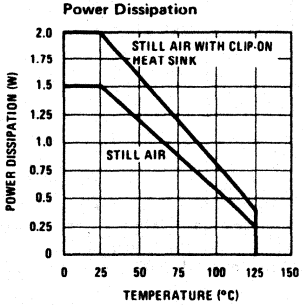
Electrical Characteristics LH0043/LH0043C: (Note 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0043			LH0043C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Hold (Logic "1") Input Voltage		2.0			2.0			V
Hold (Logic "1") Input Current	V_6 = 2.4V			5.0			5.0	μA
Sample (Logic "0") Input Voltage				0.8			0.8	V
Sample (Logic "0") Input Current	V_6 = 0.4V			1.5			1.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	V_5 = 0V, V_6 = 2V, V_{11} = 0V V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		20 14	22 18		20 14	22 18	mA mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.02	0.1		0.02	0.3	%
DC Input Resistance	T_C = 25°C	10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Current – I_5			1.0	5.0		2.0	10.0	nA
Input Capacitance			1.5			1.5		pF
Leakage Current–pin 1	V_5 = ±10V; V_{11} = ±10, T_C = 25°C		10	25		20	50	pA
	V_5 = ±10V; V_{11} = ±10V		10	25		2	5	nA
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF, T_C = 25°C		10	25		20	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF		10	25		2	5	mV/ms
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_C = 25°C		1	2.5		2	5	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF		1	2.5		0.2	0.5	mV/ms
Aperture Time			20	60		20	60	ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.001 μF ΔV_{OUT} = 20V, C_S = 0.01 μF ΔV_{OUT} = 5V, C_S = 0.001 μF		10 30 4	15 50		10 30 4	15 50	μs μs μs
Output Amplifier Slew Rate	V_{OUT} = 5V, C_S = 0.001 μF	1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	R_S < 10k, V_5 = 0V, V_6 = 0V			±40			±40	mV
Analog Voltage Output Range	$R_L \geq$ 1k, T_A = 25°C $R_L \geq$ 2k	±10 ±10	±11 ±12		±10 ±10	±11 ±12		V V

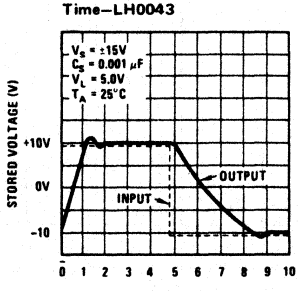
Note 2: Unless otherwise noted, these specifications apply for V^+ = +15V, V^- = −15V, pin 9 grounded, a 5000 pF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0043, and −25°C to +85°C for the LH0043C. All typical values are for T_C = 25°C.

Typical Performance Characteristics

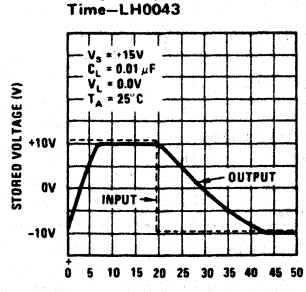
Power Dissipation



Sample Acquisition Time—LH0043

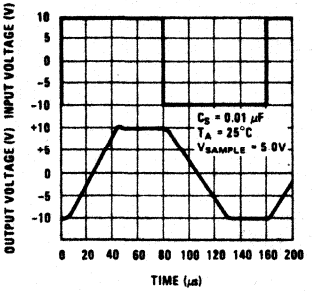


Sample Acquisition Time—LH0043

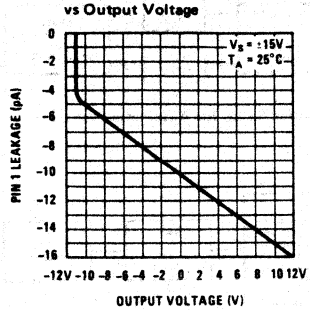


Typical Performance Characteristics (Continued)

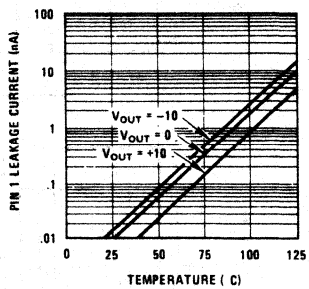
Sample Acquisition Time—LH0023



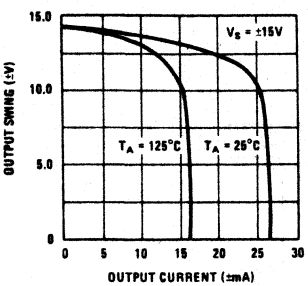
Pin 1 Leakage Current vs Output Voltage



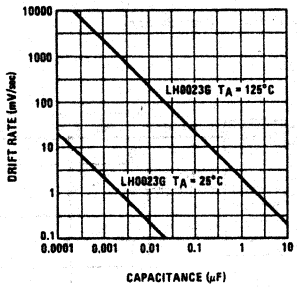
Pin 1 Leakage Current vs Temperature



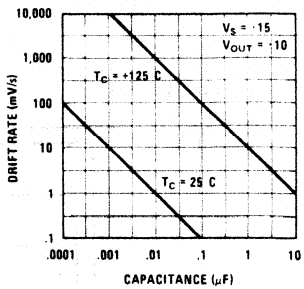
Output Current Limiting



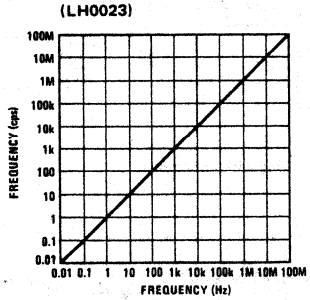
Drift vs Capacitance (LH0023)



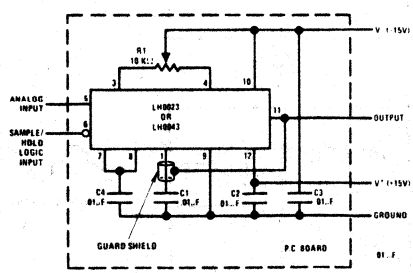
Drift vs Capacitance (LH0043)



(LH0023)



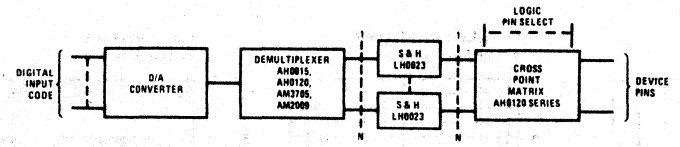
Typical Applications



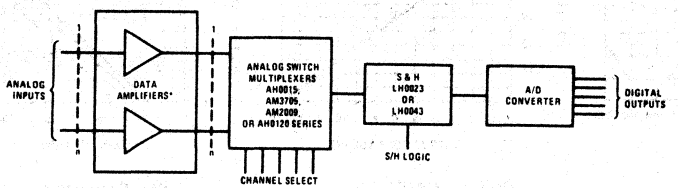
Note 1: C1 is polystyrene.
Note 2: C2, C3, C4 are ceramic disc.
Note 3: Jumper 7–8 and C4 not required for LH0043.
Note 4: R1 optional if zero trim is required.

How to Build a Sample and Hold Module

Typical Applications (Continued)

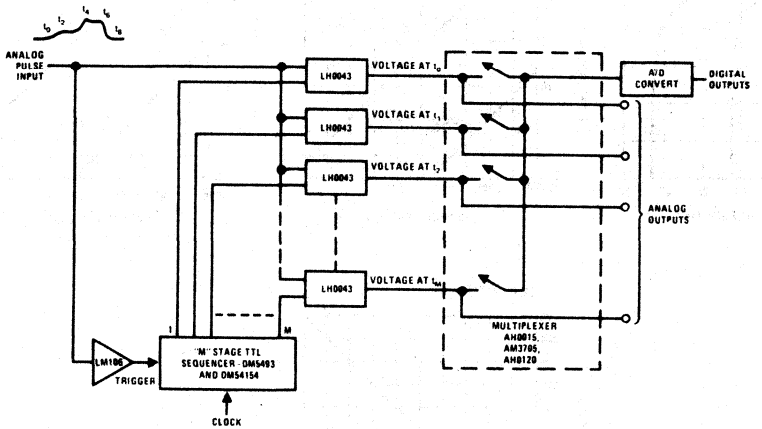


Forcing Function Setup for Automatic Test Gear

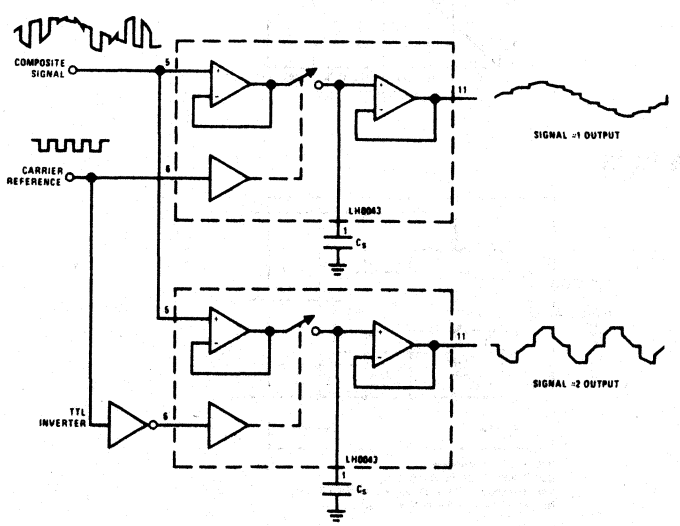


*See op amp selection guide for details. Most popular types include LH0052, LM108, LM112, LH0044, LH0036, and LH0038.

Data Acquisition System



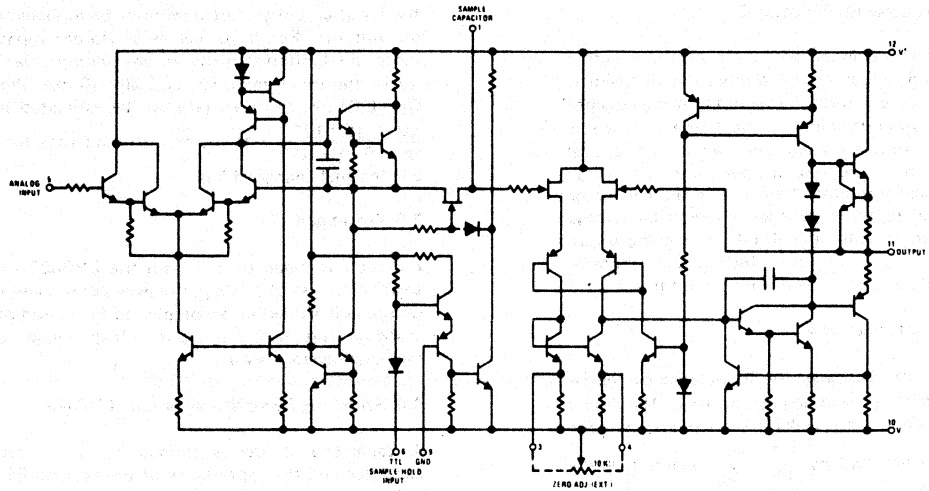
Single Pulse Sampler



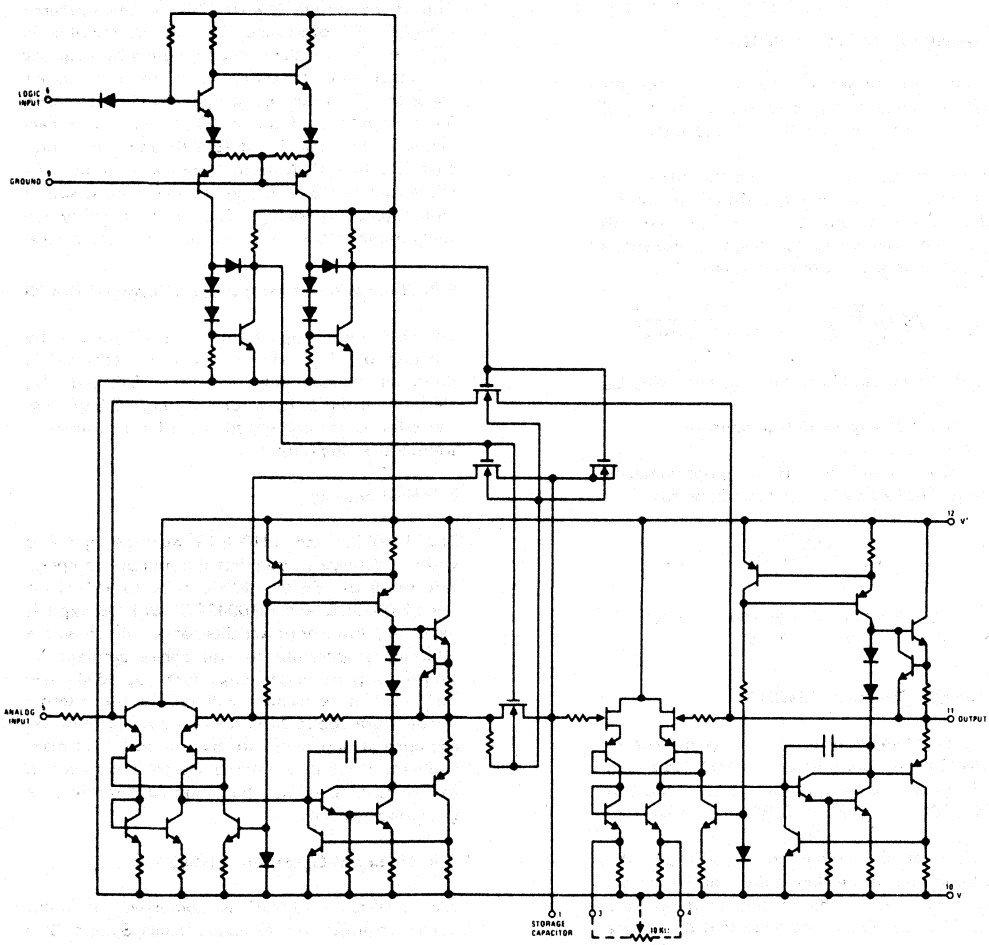
Two Channel Double Sideband Demodulator

Schematic Diagrams

LH0043/LH0043C



LH0023/LH0023C



Applications Information

1.0 Drift Error Minimization

In order to minimize drift error, care in selection of C_S and layout of the printed circuit board is required. The capacitor should be of high quality Teflon, polycarbonate, or polystyrene construction. Board cleanliness and layout are critical particularly at elevated temperatures. See AN-63 for detailed recommendations. A guard conductor connected to the output surrounding the storage node (pin 1) will be helpful in meeting severe environmental conditions which would otherwise cause leakage across the printed circuit board.

2.0 Capacitor Selection

The size of the capacitor is dictated by the required drift rate and acquisition time. The drift is determined by the leakage current at pin 1 and may be calculated by $\frac{dV}{dt} = \frac{I_L}{C_S}$, where I_L is the total leakage current at pin 1 of the device, and C_S is the value of the storage capacitor.

2.1 Capacitor Selection – LH0023

At room temperature leakage current for the LH0023 is approximately 100 pA. A drift rate of 10 mV/sec would require a 0.01 μF capacitor.

For values of C_S up to 0.01 μF the acquisition time is limited by the slew rate of the input buffer amplifier, A1, typically 0.5 V/μs. Beyond this point, current availability to charge C_S also enters the picture. The acquisition time is given by:

$$t_A \cong \sqrt{\frac{2\Delta e_O RC_S}{0.5 \times 10^6}} = 2 \times 10^{-3}\sqrt{\Delta e_O RC_S}$$

where: R = the internal resistance in series with C_S

Δe_O = change in voltage sampled

An average value for R is approximately 600 ohms. The expression for t_A reduces to:

$$t_A \cong \sqrt{\frac{\Delta e_O C_S}{20}}$$

For a −10V to +10V change and C_S = .05 μF, acquisition time is typically 50 μs.

2.2 Capacitor Selection—LH0043

At 25°C case temperature, the leakage current for the LH0043G is approximately 10 pA, so a drift rate of 5 mV/s would require a capacitor of $C_S = 10 \cdot 10^{-12}/5 \cdot 10^{-3} = 2000$ pF or larger.

For values of C_S below about 5000 pF, the acquisition time of the LH0043G will be limited by the slew rate of the output amplifier (the signal will be acquired, in the sense that the voltage will be stored on the capacitor, in much less time as dictated by the slew rate and current capacity of the input amplifier, but it will not be available at the output). For larger values of storage capacitance, the limitation is the current sinking capability of the input amplifier, typically 10 mA. With $C_S = 0.01\ \mu$F, the slew rate can be estimated by $\frac{dV}{dt} = \frac{10 \cdot 10^{-3}}{0.01 \cdot 10^{-6}} = 1$V/$\mu$s or a slewing time for a 5 volt signal change of 5μs.

3.0 Offset Null

Provision is made to null both the LH0023 and LH0043 by use of a 10k pot between pins 3 and 4. Offset null should be accomplished in the sample mode at one half the input voltage range for minimum average error.

4.0 Switching Spike Minimization—LH0043

A capacitive divider is formed by the storage capacitor and the capacitance of the internal FET switch which causes a small error current to be injected into the storage capacitor at the termination of the sample interval. This can be considered a negative DC offset and nulled out as described in (3.0), or the transient may be nulled by coupling an equal but opposite signal to the storage capacitor. This may be accomplished by connecting a capacitor of about 30 pF (or a trimmer) between the logic input (pin 6) and the storage capacitor (pin 1). Note that this capacitor must be chosen as carefully as the storage capacitor itself with respect to leakage. The LH0023 has switch spike minimization circuitry built into the device.

5.0 Elimination of the 5V Logic Supply—LH0023

The 5V logic supply may be eliminated by shorting pin 7 to pin 8 which connects a 10k dropping resistor between the +15V and V_C. Decoupling pin 8 to ground through 0.1 μF disc capacitor is recommended in order to minimize transients in the output.

6.0 Heat Sinking

The LH0023 and LH0043G may be operated without damage throughout the military temperature range of −55 to +125°C (−25 to +85°C for the LH0023CG and LH0043CG) with no explicit heat sink, however power dissipation will cause the internal temperature to rise above ambient. A simple clip-on heat sink such as Wakefield #215-1.9 or equivalent will reduce the internal temperature about 20°C thereby cutting the leakage current and drift rate by one fourth at max. ambient. There is no internal electrical connection to the case, so it may be mounted directly to a grounded heat sink.

7.0 Theory of Operation—LH0023

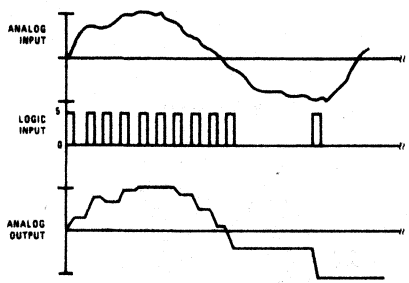
The LH0023/LH0023C is comprised of input buffer amplifier, A1, analog switches, S1 and S2, a

Applications Information (Continued)

TTL to MOS level translator, and output buffer amplifier, A2. In the "sample" mode, the logic input is raised to logic "1" ($V_6 \leq 2.0V$) which closes S1 and opens S2. Storage capacitor, C_S, is charged to the input voltage through S1 and the output slews to the input voltage. In the "hold" mode, the logic input is lowered to logic "0" ($V_6 \leq 0.8V$) opening S1 and closing S2. C_S retains the sample voltage which is applied to the output via A2. Since S1 is open, the input signal is overridden, and leakage across the MOS switch is therefore minimized. With S1 open, drift is primarily determined by input bias current of A2, typically 100 pA at 25°C.

7.1 Theory of Operation—LH0043

The LH0043/LH0043C is comprised of input buffer amplifier A1, FET switch S1 operated by a TTL compatible level translator, and output buffer amplifier A2. To enter the "sample" mode, the logic input is taken to the TTL logic "0" state (V_6 = 0.8V) which commands the switch S1 closed and allows A1 to make the storage capacitor voltage equal to the analog input voltage. In the "hold" mode (V_6 = 2.0V), S1 is opened isolating the storage capacitor from the input and leaving it charged to a voltage equal to the last analog input voltage before entering the hold mode. The storage capacitor voltage is brought to the output by low leakage amplifier A2.



8.0 Definitions

- V_5: The voltage at pin 5, e.g., the analog input voltage.
- V_6: The voltage at pin 6, e.g., the logic control input signal.
- V_{11}: The voltage at pin 11, e.g., the output signal.
- T_A: The temperature of the ambient air.
- T_C: The temperature of the device case at the center of the bottom of the header.

Acquisition Time:
The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to the input (pin 5) with the logic input (pin 6) in the low state.

Aperture Time:
The time indeterminacy when switching from sample mode to hold including the delay from the time the mode control signal (pin 6) passes through its threshold (1.4 volts) to the time the circuit actually enters the hold mode.

Output Offset Voltage:
The voltage at the output terminal (pin 11) with the analog input (pin 5) at ground and logic input (pin 6) in the "sample" mode. This will always be adjustable to zero using a 10k pot between pins 3 and 4 with the wiper arm returned to V^-.

National Semiconductor

LH0053/LH0053C High Speed Sample and Hold Amplifier

General Description

The LH0053/LH0053C is a high speed sample and hold circuit capable of acquiring a 20V step signal in under 5.0μs.

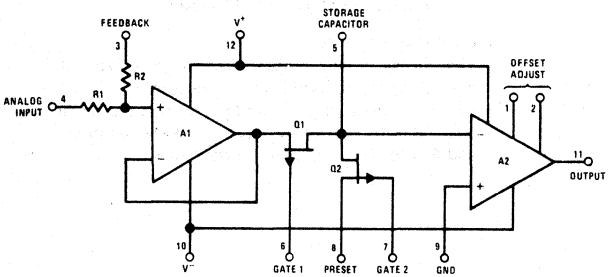
The device is ideally suited for a variety of high speed data acquisition applications including analog buffer memories for A to D conversion and synchronous demodulation.

An auxiliary switch within the device extends its usefulness in applications such as preset integrators.

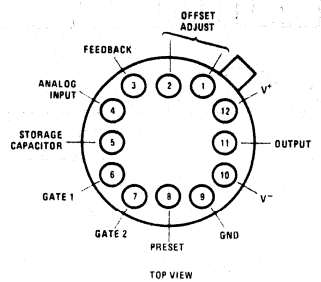
Features

- Sample acquisition time 10μs max for 20V signal
- FET switch for preset or reset function
- Sample accuracy null
- Offset adjust to 0V
- DTL/TTL compatible FET gate
- Single storage capacitor

Schematic and Connection Diagrams

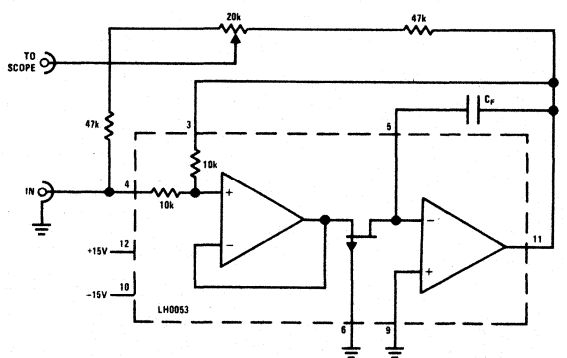


Metal Can Package



Order Number LH0053G or LH0053CG
See Package H12B

AC Test Circuit



Acquisition Time Test Circuit

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±18V
Gate Input Voltage (V_6 and V_7)	±20V
Analog Input Voltage (V_4)	±15V
Input Current (I_8 and I_5)	±10 mA
Power Dissipation	1.5W
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0053	−55°C to +125°C
LH0053C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

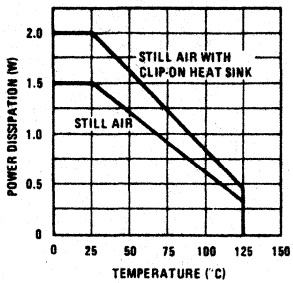
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0053			LH0053C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Sample (Gate "0") Input Voltage				0.5			0.5	V
Sample (Gate "0") Input Current	V_6 = 0.5V, T_A = 25°C V_6 = 0.5			5.0 100			5.0 100	µA µA
Hold (Gate "1") Input Voltage		4.5			4.5			V
Hold (Gate "1") Input Current	V_6 = 4.5V, T_A = 25°C V_6 = 4.5V			1.0 1.0			1.0 1.0	nA µA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	V_4 = 0V V_6 = 0.5V		13	18		13	18	mA
Input Bias Current (I_4)	V_4 = 0V, T_A = 25°C		120	250		150	500	nA
Input Resistance		9.0	10	11	9.0	10	11	kΩ
Analog Output Voltage Range	R_L = 2.0k	±10	±12		±10	±12		V
Output Offset Voltage	V_4 = 0V, V_6 = 0.5V, T_A = 25°C V_4 = 0V, V_6 = 0.5V		5.0	7.0 10		5.0	10 15	mV mV
Sample Accuracy (Note 2)	V_4 = ±10V, V_6 = 0.5V, T_A = 25°C		0.1	0.2		0.1	0.3	%
Aperture Time	ΔV_6 = 4.5V, T_A = 25°C		10	25		10	25	ns
Sample Acquisition Time	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF, V_6 = 0V		5.0	10		8.0	15	µs
Sample Acquisition Time	V_4 = ±10V, T_A = 25°C, C_F = 100 pF, V_6 = 0V		4.0			4.0		µs
Output Slew Rate	ΔV_{IN} = ±10V, T_A = 25°C, C_F = 100 pF, V_6 = 0V		20			20		V/µs
Large Signal Bandwidth	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF		200			200		kHz
Leakage Current (Pin 5)	V_4 = ±10V, T_A = 25°C, V_4 = ±10V		6.0	30 30		10	50 3.0	pA nA
Drift Rate	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF		6.0	30		10	50	mV/s
Drift Rate	V_4 = ±10V, C_F = 1000 pF			30			3.0	V/s
Q2 Switch ON Resistance	V_7 = 0.5V, I_8 = 1.0 mA, T_A = 25°C		100	300		100	300	Ω

Note 1: Unless otherwise noted, these specifications apply for V_S = ±15V, pin 9 grounded, a 1000 pF capacitor between pin 5 and pin 11, pin 3 shorted to pin 11, over the temperature range −55°C to +125°C for the LH0053 and −25°C to +85°C for the LH0053C. All typical values are for T_A = 25°C.

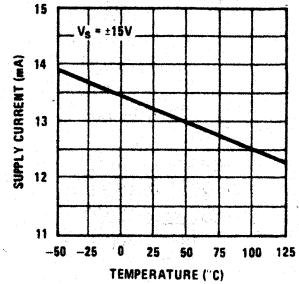
Note 2: Sample accuracy may be nulled by inserting a potentiometer in the feedback loop. This compensates for source impedance and feedback resistor tolerances.

Typical Performance Characteristics

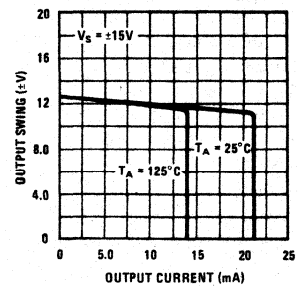
Power Dissipation



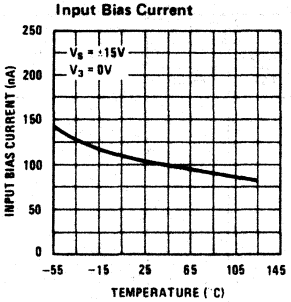
Supply Current vs Temperature



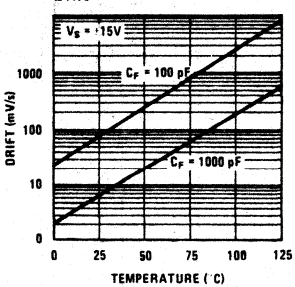
Output Current Limiting



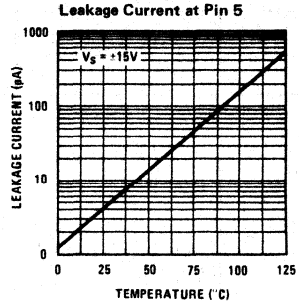
Input Bias Current



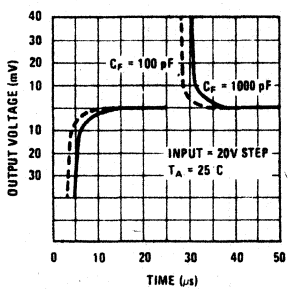
Drift



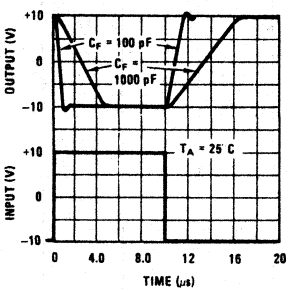
Leakage Current at Pin 5



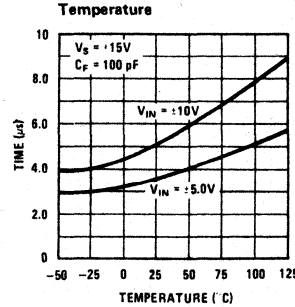
Sample Acquisition Time



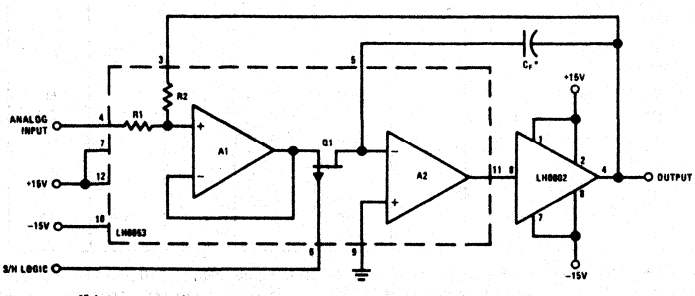
Output Slew Rate



Acquisition Time vs Temperature

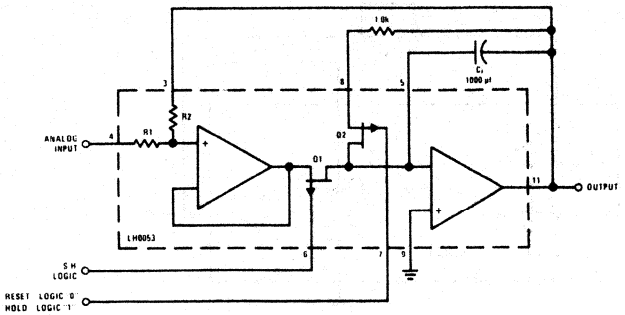


Typical Applications

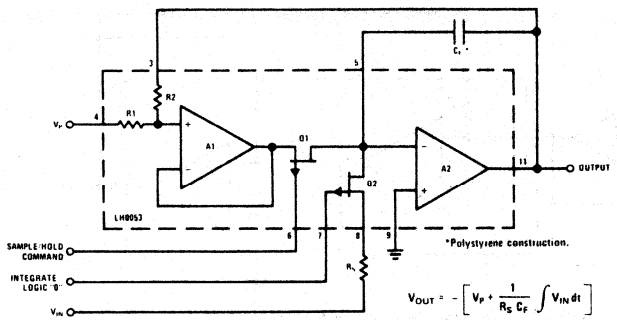


Increasing Output Drive Capability

Typical Applications (Continued)



Sample and Hold with Reset



Preset Integrator

Applications Information

SOURCE IMPEDANCE COMPENSATION

The gain accuracy (linearity) of the LH0053/LH0053C is set by two internal precision resistors. Circuit applications in which the source impedance is non-zero will result in a closed loop gain error, e.g. if R_S = 10Ω, a gain error of 0.1% results. Figure 1 and 2 show methods for accommodating non-zero source impedance.

DRIFT ERROR MINIMIZATION

In order to minimize drift error, care in selection C_F and layout of the printed circuit board is required. The capacitor should be of high quality teflon, polycarbonate or polystyrene construction. Board layout and clean lines are critical particularly at elevated temperature.

A ground guard (shield) surrounding pin 5 will minimize leakage currents to and from the summing junction, arising from extraneous signals. See AN-63 for detailed recommendations.

CAPACITOR SELECTION

The size of the capacitor is determined by the required drift rate usually at the expense of acquisition time.

The drift is dictated by leakage current at pin 5 and is given by:

$$\frac{dv}{dt} = \frac{I_L}{C_F}$$

Where I_L is the leakage current at pin 5 and C_F is the value of the capacitance. The room temperature leakage of the LH0053 is typical 6.0 pA, and a 1000 pF capacitor will yield a drift rate of 6.0 mV per second.

For values of C_F below 1000 pF acquisition for the LH0053 is primarily governed by the slew rate of the input amplifier (20 V/μs) and the setting time of output amplifier (≅ 1.0μs). For values above C_F = 1000 pF, acquisition time is given by:

$$t_a = \frac{C_F\,\Delta V}{I_{DSS}} + t_{S2}$$

Where:

C_F = The value of the capacitor

ΔV = The magnitude of the input step; e. g. 20V

I_{DSS} = The ON current of switch Q1 ≅ 5.0 mA

t_{S2} = The setting time of output amplifier ≅ 1.0μs

Applications Information (Continued)

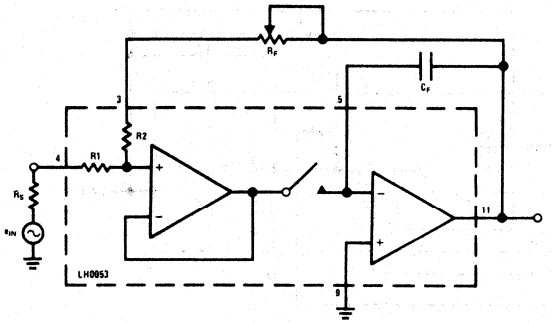


FIGURE 1. Non-Zero Source Impedance Compensation

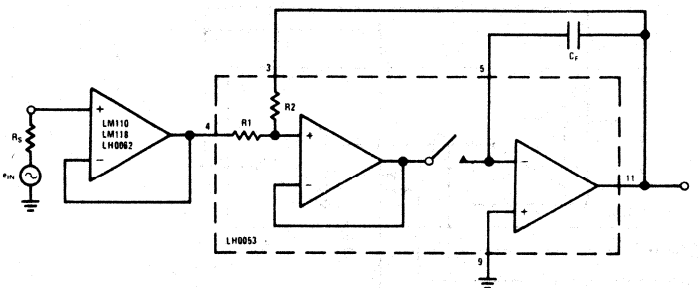


FIGURE 2. Non-Zero Source Impedance Buffering

GATE INPUT CONSIDERATIONS

5.0V TTL Applications

The LH0053 Gate inputs Gate 1 (pin 6) and Gate 2 (pin 7) will interface directly with 5.0V TTL. However, TTL gates typically pull up to 2.5V in the logic "1" state. It is therefore advisable to use a 10k pull up resistor between the 5.0V, V_{CC}, and the output of the gate as shown in Figure 3.

To obtain the highest speed and fastest acquisition time, the gate drive shown in Figure 6 is recommended.

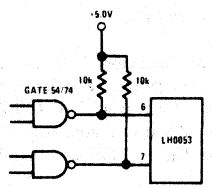


FIGURE 3. TTL Logic Compatibility

CMOS Applications

The LH0053 gate inputs may be interfaced directly with 74C, CMOS operating off of V_{CC}'s from 5.0V to 15V. However transient currents of several milliamps can flow on the rising and falling edges of the input signal. It is, therefore, advisable to parallel the outputs of two 54C/74C gates as shown in Figure 4.

It should be noted that leakage at pin 5 in the hold mode will be increased by a factor of 2 to 3 when operating into 15V logic levels.

Unused Switch, Q2

In applications when switch Q2 is not used the logic input (pin 7) should be returned to +5.0V (or +15V for HTL applications) through a 10kΩ resistor. Analog Input, preset (pin 8) should be grounded.

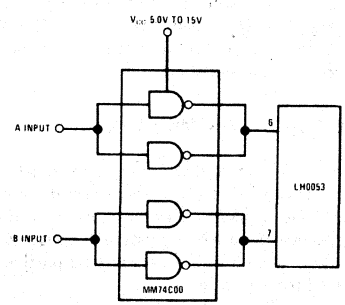


FIGURE 4. CMOS Logic Compatibility

HEAT SINKING

The LH0053 may be operated over the military temperature range, −55°C to +125°C, without incurring damage to the device. However, a clip on heat sink such as the Wakefield 215 Series or Thermolloy 2240 will reduce the internal temperature rise by about 20°C. The result is a two-fold improvement in drift rate at temperature.

Applications Information (Continued)

Since the case of the device is electrically isolated from the circuit, the LH0053 may be mounted directly to a grounded heat sink.

POWER SUPPLY DECOUPLING

Amplifiers A1 and A2 within the LH0053 are very wide band devices and are sensitive to power supply inductance. It is advisable to by-pase V^+ (pin 12) and V^- (pin 10) to ground with 0.1μF disc capacitors in order to prevent oscillation. Should this procedure prove inadequate, the disc capacitors should be paralled with 4.7μF solid tantalum electrolytic capacitors.

DC OFFSET ADJUST

Output offset error may be adjusted to zero using the circuit shown in Figure 5. Offset null should be accomplished in the sample mode ($V_6 \leq 0.5V$) and analog input (pin 4) equal to zero volts.

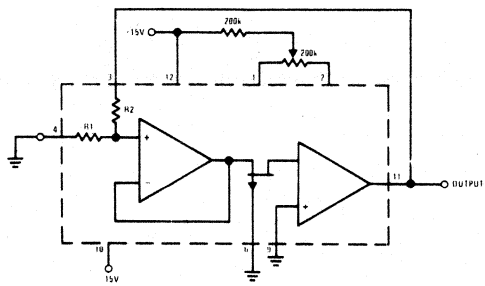


FIGURE 5. Offset Null Circuit

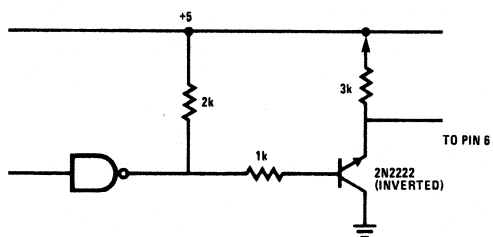


FIGURE 6. High Speed Gate Drive Circuit

Definition of Terms

Voltage, V_4: The voltage at pin 4, i.e., the analog input voltage.

Voltage, V_6: The voltage at pin 6, i.e., the logic control signal. A logic "1" input,, $V_6 \leq 4.5V$, places the LH0053 in the HOLD mode; a logic "0" input ($V_6 \leq 0.5V$) places the device in sample mode.

Acquisition Time: The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to Analog Input 1 (pin 4) with logic input, Gate 1, (pin 6) in the logic "0" state.

Aperture Time: The time indeterminacy when switching from the "sample" mode to the HOLD mode measured from time the logic input passes through it's threshold (2.0V) to the time the device actually enters the HOLD mode.

Sample Accuracy: Difference between input voltage and output voltage while in the sample mode, expressed as a percent of input voltage.

Section 12

Sensors/Transducers

12

Section Contents

National Semiconductor

LM134/LM234/LM334
3-Terminal Adjustable Current Sources

General Description

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64 mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈+0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the new current sources include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The LM134-3/LM234-3 and LM134-6/LM234-6 are specified as true temperature sensors with guaranteed initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

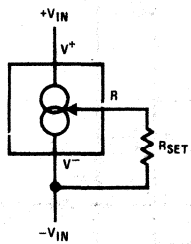
The LM134 is guaranteed over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO-46 hermetic and TO-92 plastic packages.

Features

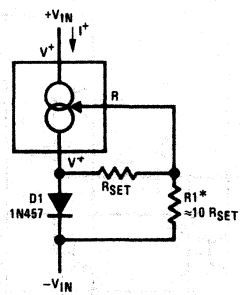
- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1 μA to 10 mA
- True 2-terminal operation
- Available as fully specified temperature sensor
- ±3% initial accuracy

Typical Applications

Basic 2-Terminal Current Source

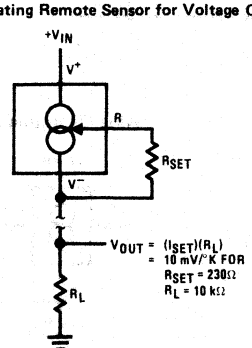


Zero Temperature Coefficient Current Source

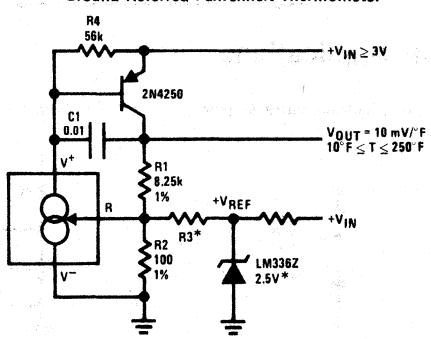


*Select ratio of R1 to R_{SET} to obtain zero drift. $I^+ \approx 2\ I_{SET}$

Terminating Remote Sensor for Voltage Output



Ground Referred Fahrenheit Thermometer



*Select R3 = V_{REF}/583 μA. V_{REF} may be any stable positive voltage ≥ 2V
Trim R3 to calibrate

12

National Semiconductor

LM135/LM235/LM335, LM135A/LM235A/LM335A Precision Temperature Sensors

General Description

The LM135 series are precision, easily-calibrated, integrated circuit temperature sensors. Operating as a 2-terminal zener, the LM135 has a breakdown voltage directly proportional to absolute temperature at +10 mV/°K. With less than 1Ω dynamic impedance the device operates over a current range of 400 μA to 5 mA with virtually no change in performance. When calibrated at 25°C the LM135 has typically less than 1°C error over a 100°C temperature range. Unlike other sensors the LM135 has a linear output.

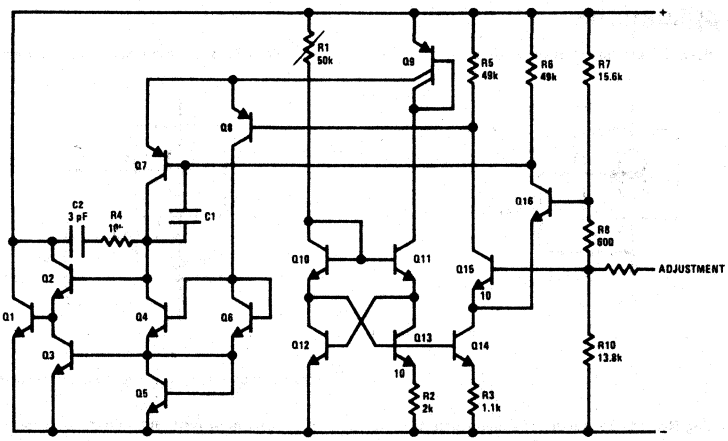
Applications for the LM135 include almost any type of temperature sensing over a −55°C to +150°C temperature range. The low impedance and linear output make interfacing to readout or control circuitry especially easy.

The LM135 operates over a −55°C to +150°C temperature range while the LM235 operates over a −40°C to +125°C temperature range. The LM335 operates from −10°C to +100°C. The LM135/LM235/LM335 are available packaged in hermetic TO-46 transistor packages while the LM235 and LM335 are also available in plastic TO-92 packages.

Features

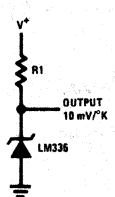
- Directly calibrated in °Kelvin
- 1°C initial accuracy available
- Operates from 400 μA to 5 mA
- Less than 1Ω dynamic impedance
- Easily calibrated
- Wide operating temperature range
- 200°C overrange
- Low cost

Schematic Diagram

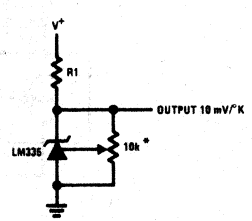


Typical Applications

Basic Temperature Sensor

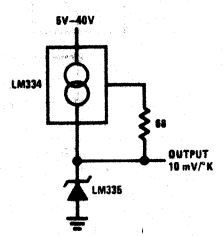


Calibrated Sensor



*Calibrate for 2.982V at 25°C

Wide Operating Supply



Absolute Maximum Ratings

Reverse Current	10 mA
Forward Current	10 mA
Storage Temperature	
TO-46 Package	−60°C to +180°C
TO-92 Package	−60°C to +150°C
Specified Operating Temperature Range	

	Continuous	Intermittent
LM135, LM135A	−55°C to +150°C	150°C to 200°C
LM235, LM235A	−40°C to +125°C	125°C to 150°C
LM335, LM335A	−10°C to +100°C	100°C to 125°C
Lead Temperature (Soldering, 10 seconds)		300°C

Temperature Accuracy LM135/LM235, LM135A/LM235A (Note 1)

PARAMETER	CONDITIONS	LM135A/LM235A			LM135/LM235			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage	$T_C = 25°C$, $I_R = 1$ mA	2.97	2.98	2.99	2.95	2.98	3.01	V
Uncalibrated Temperature Error	$T_C = 25°C$, $I_R = 1$ mA		0.5	1		1	3	°C
Uncalibrated Temperature Error	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		1.3	2.7		2	5	°C
Temperature Error with 25°C Calibration	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		0.3	1		0.5	1.5	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1$ mA		0.3	0.5		0.3	1	°C

Temperature Accuracy LM335, LM335A (Note 1)

PARAMETER	CONDITIONS	LM335A			LM335			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage	$T_C = 25°C$, $I_R = 1$ mA	2.95	2.98	3.01	2.92	2.98	3.04	V
Uncalibrated Temperature Error	$T_C = 25°C$, $I_R = 1$ mA		1	3		2	6	°C
Uncalibrated Temperature Error	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		2	5		4	9	°C
Temperature Error with 25°C Calibration	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		0.5	1		1	2	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1$ mA		0.3	1.5		0.3	1.5	°C

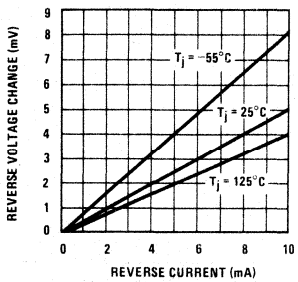
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM135/LM235 LM135A/LM235A			LM335 LM335A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage Change with Current	400 μA < I_R < 5 mA At Constant Temperature		2.5	10		3	14	mV
Dynamic Impedance	$I_R = 1$ mA		0.5			0.6		Ω
Output Voltage Temperature Drift			+10			+10		mV/°C
Time Constant	Still Air		80			80		sec
	100 ft/Min Air		10			10		sec
	Stirred Oil		1			1		sec
Time Stability	$T_C = 125°C$		0.2			0.2		°C/khr

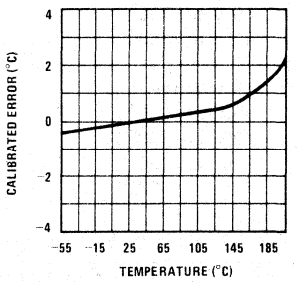
Note 1: Accuracy measurements are made in a well-stirred oil bath. For other conditions, self heating must be considered.

Typical Performance Characteristics

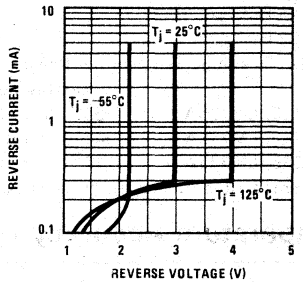
Reverse Voltage Change



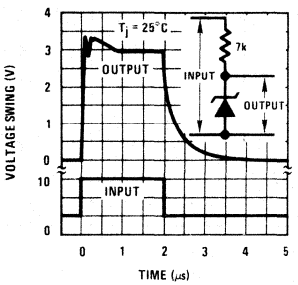
Calibrated Error



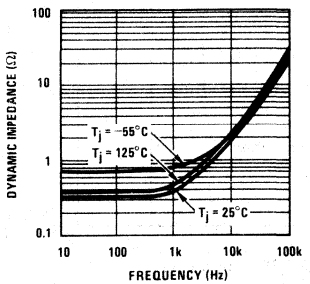
Reverse Characteristics



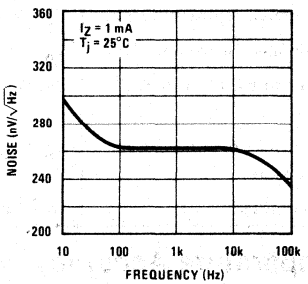
Response Time



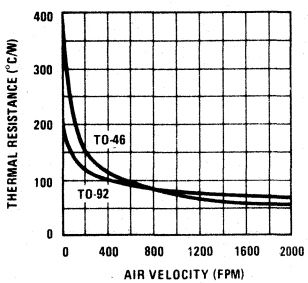
Dynamic Impedance



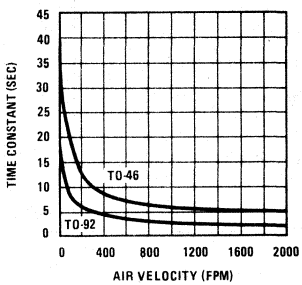
Noise Voltage



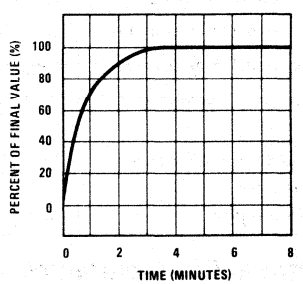
Thermal Resistance Junction to Air



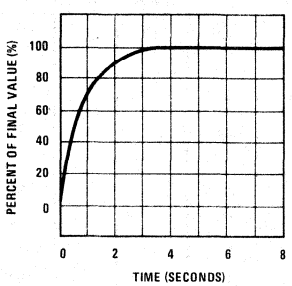
Thermal Time Constant



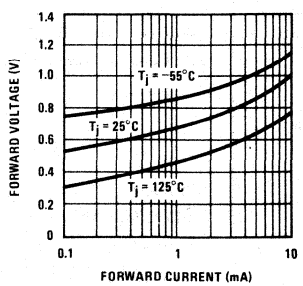
Thermal Response in Still Air



Thermal Response in Stirred Oil Bath



Forward Characteristics



Application Hints

CALIBRATING THE LM135

Included on the LM135 chip is an easy method of calibrating the device for higher accuracies. A pot connected across the LM135 with the arm tied to the adjustment terminal allows a 1-point calibration of the sensor that corrects for inaccuracy over the full temperature range.

This single point calibration works because the output of the LM135 is proportional to absolute temperature with the extrapolated output of sensor going to 0V output at 0°K (−273.15°C). Errors in output voltage versus temperature are only slope (or scale factor) so a slope calibration at one temperature corrects at all temperatures.

The output of the device (calibrated or uncalibrated) can be expressed as:

$$V_{OUT_T} = V_{OUT_{T_O}} \times \frac{T}{T_O}$$

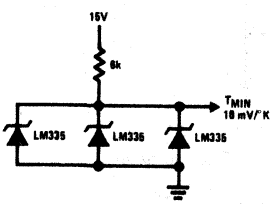
where T is the unknown temperature and T_O is a reference temperature, both expressed in degrees Kelvin. By calibrating the output to read correctly at one temperature the output at all temperatures is correct. Nominally the output is calibrated at 10 mV/°K.

To insure good sensing accuracy several precautions must be taken. Like any temperature sensing device, self heating can reduce accuracy. The LM135 should be operated at the lowest current suitable for the application. Sufficient current, of course, must be available to drive both the sensor and the calibration pot at the maximum operating temperature.

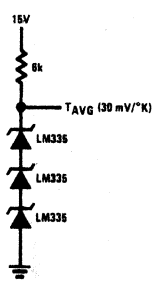
If the sensor is used in an ambient where the thermal resistance is constant, self heating errors can be calibrated out. This is possible if the device is run with a temperature stable current. Heating will then be proportional to zener voltage and therefore temperature. This makes the self heating error proportional to absolute temperature the same as scale factor errors.

Typical Applications (Continued)

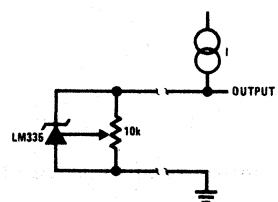
Minimum Temperature Sensing



Average Temperature Sensing



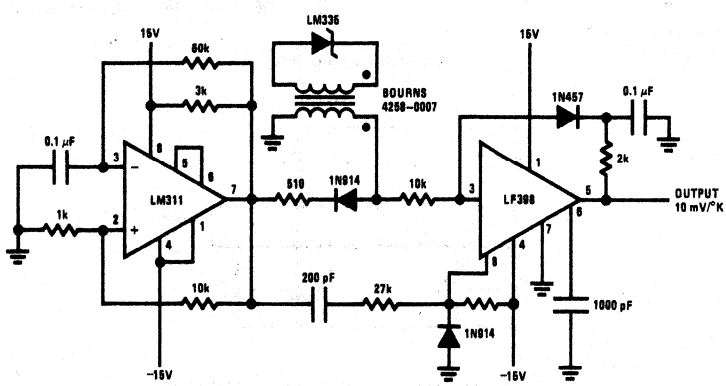
Remote Temperature Sensing



Wire length for 1° C error due to wire drop

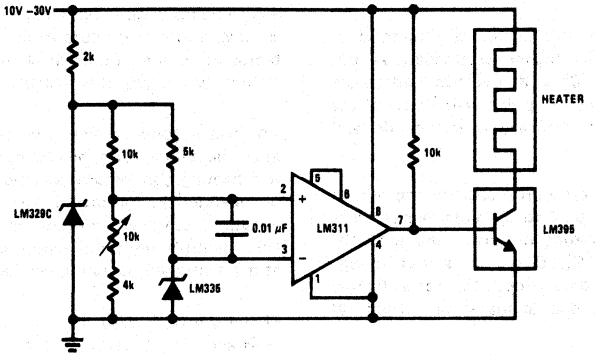
AWG	I_R = 1 mA FEET	I_R = 0.5 mA FEET
14	4000	8000
16	2500	5000
18	1600	3200
20	1000	2000
22	625	1250
24	400	800

Isolated Temperature Sensor

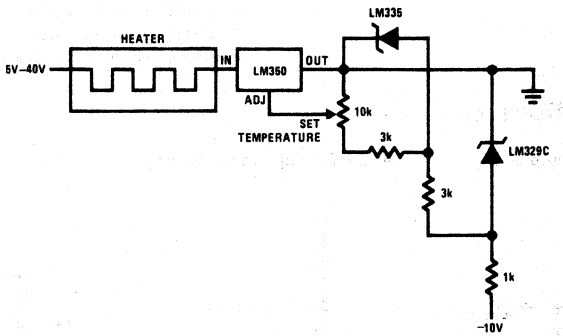


Typical Applications (Continued)

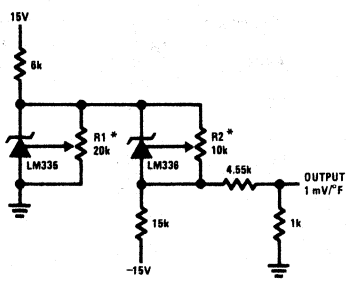
Simple Temperature Controller



Simple Temperature Control

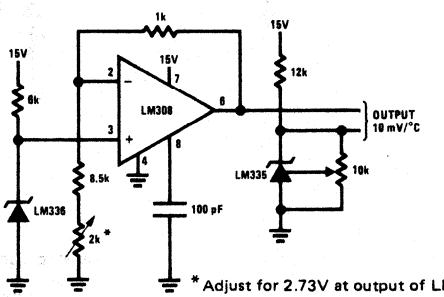


Ground Referred Fahrenheit Thermometer



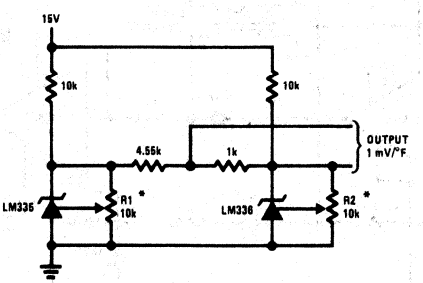
*Adjust R2 for 2.554V across LM336.
Adjust R1 for correct output.

Centigrade Thermometer



*Adjust for 2.73V at output of LM308

Fahrenheit Thermometer

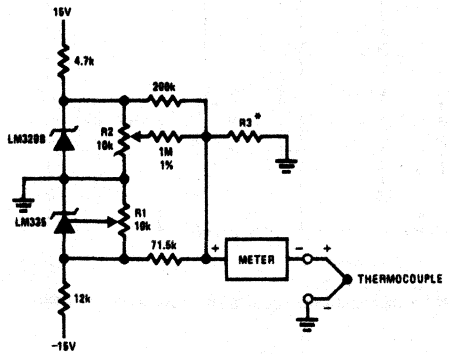


*To calibrate adjust R2 for 2.554V across LM336.
Adjust R1 for correct output.

Typical Applications (Continued)

THERMOCOUPLE COLD JUNCTION COMPENSATION

Compensation for Grounded Thermocouple



*Select R3 for proper thermocouple type

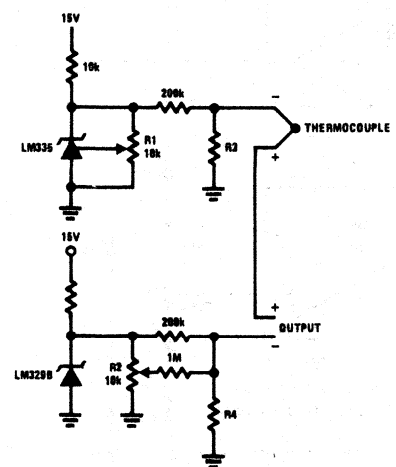
THERMOCOUPLE	R3	SEEBECK COEFFICIENT
J	377Ω	52.3 μV/°C
T	308Ω	42.8 μV/°C
K	293Ω	40.8 μV/°C
S	45.8Ω	6.4 μV/°C

Adjustments: Compensates for both sensor and resistor tolerances

1. Short LM329B
2. Adjust R1 for Seebeck Coefficient times ambient temperature (in degrees K) across R3
3. Short LM335 and adjust R2 for voltage across R3 corresponding to thermocouple type

J	14.32 mV	K	11.17 mV
T	11.79 mV	S	1.768 mV

Single Power Supply Cold Junction Compensation



*Select R3 and R4 for thermocouple type

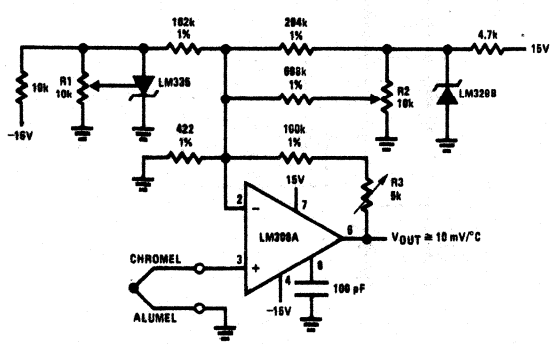
THERMOCOUPLE	R3	R4	SEEBECK COEFFICIENT
J	1.05K	385Ω	52.3 μV/°C
T	856Ω	315Ω	42.8 μV/°C
K	816Ω	300Ω	40.8 μV/°C
S	128Ω	46.3Ω	6.4 μV/°C

Adjustments:

1. Adjust R1 for the voltage across R3 equal to the Seebeck Coefficient times ambient temperature in degrees Kelvin.
2. Adjust R2 for voltage across R4 corresponding to thermocouple

J	14.32 mV	K	11.17 mV
T	11.79 mV	S	1.768 mV

Centigrade Calibrated Thermocouple Thermometer



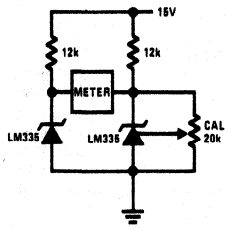
Terminate thermocouple reference junction in close proximity to LM335.

Adjustments:

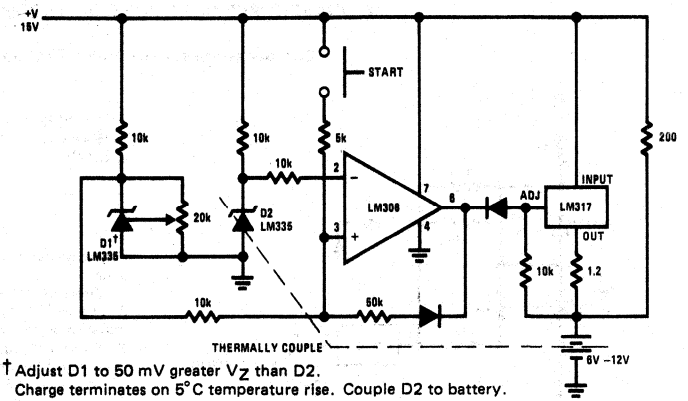
1. Apply signal in place of thermocouple and adjust R3 for a gain of 245.7.
2. Short non-inverting input of LM308A and output of LM329B to ground.
3. Adjust R1 so that V_{OUT} = 2.982V @ 25°C.
4. Remove short across LM329B and adjust R2 so that V_{OUT} = 246 mV @ 25°C.
5. Remove short across thermocouple.

Typical Applications (Continued)

Differential Temperature Sensor

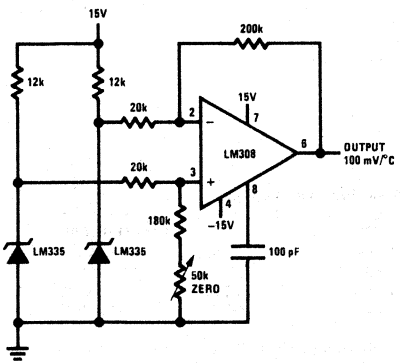


Fast Charger for Nickel-Cadmium Batteries

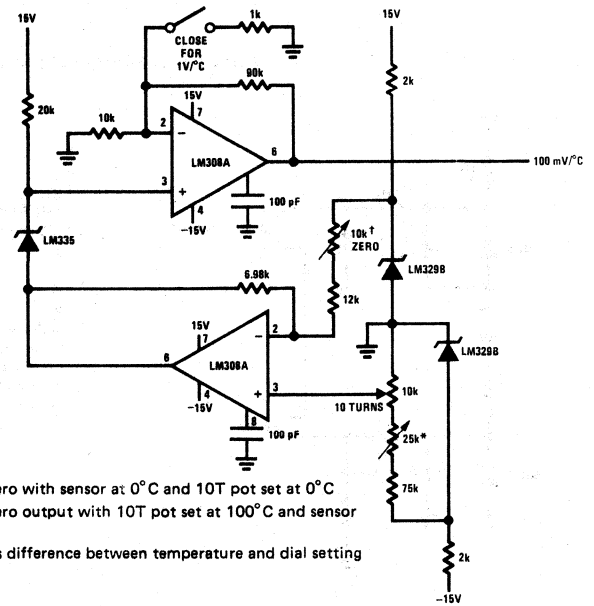


† Adjust D1 to 50 mV greater V_Z than D2.
Charge terminates on 5°C temperature rise. Couple D2 to battery.

Differential Temperature Sensor

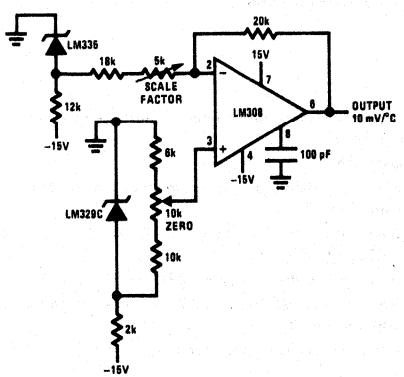


Variable Offset Thermometer‡

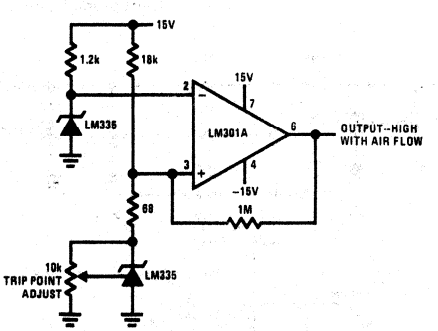


† Adjust for zero with sensor at 0°C and 10T pot set at 0°C
* Adjust for zero output with 10T pot set at 100°C and sensor at 100°C
‡ Output reads difference between temperature and dial setting of 10T pot

Ground Referred Centigrade Thermometer



Air Flow Detector*



* Self heating is used to detect air flow

Definition of Terms

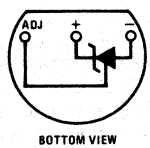
Operating Output Voltage: The voltage appearing across the positive and negative terminals of the device at specified conditions of operating temperature and current.

Uncalibrated Temperature Error: The error between the operating output voltage at 10 mV/°K and case temperature at specified conditions of current and case temperature.

Calibrated Temperature Error: The error between operating output voltage and case temperature at 10 mV/°K over a temperature range at a specified operating current with the 25°C error adjusted to zero.

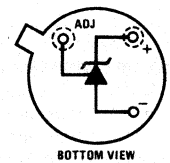
Connection Diagrams

TO-92
Plastic Package



Order Number LM235Z, LM335Z
or LM335AZ
See NS Package Z03A

TO-46
Metal Can Package*



*Case is connected to negative pin

Order Number LM135H, LM235H,
LM335H, LM135AH, LM235AH
or LM335AH
See NS Package H03H

National Semiconductor

Sensors/Transducers

LM3911 Temperature Controller

General Description

The LM3911 is a highly accurate temperature measurement and/or control system for use over a −25°C to +85°C temperature range. Fabricated on a single monolithic chip, it includes a temperature sensor, a stable voltage reference and an operational amplifier.

The output voltage of the LM3911 is directly proportional to temperature in degrees Kelvin at 10 mV/°K. Using the internal op amp with external resistors any temperature scale factor is easily obtained. By connecting the op amp as a comparator, the output will switch as the temperature transverses the set-point making the device useful as an on-off temperature controller.

An active shunt regulator is connected across the power leads of the LM3911 to provide a stable 6.8V voltage reference for the sensing system. This allows the use of any power supply voltage with suitable external resistors.

The input bias current is low and relatively constant with temperature, ensuring high accuracy when high source impedance is used. Further, the output collector can be returned to a voltage higher than 6.8V allowing the LM3911 to drive lamps and relays up to a 35V supply.

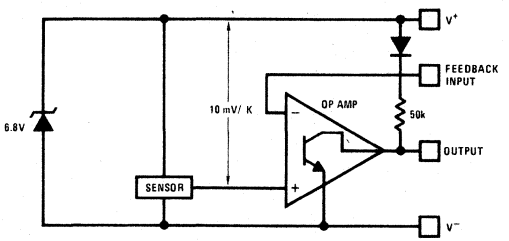
The LM3911 uses the difference in emitter-base voltage of transistors operating at different current densities as the basic temperature sensitive element. Since this output depends only on transistor matching the same reliability and stability as present op amps can be expected.

The LM3911 is available in three package styles—a metal can 4-lead TO-5, a metal can TO-46 and an 8-lead epoxy mini-DIP. In the epoxy package all electrical connections are made on one side of the device allowing the other 4 leads to be used for attaching the LM3911 to the temperature source. The LM3911 is rated for operation over a −25°C to +85°C temperature range.

Features

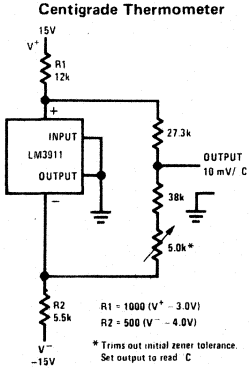
- Uncalibrated accuracy ±10°C
- Internal op amp with frequency compensation
- Linear output of 10 mV/°K (10 mV/°C)
- Can be calibrated in degrees Kelvin, Celsius or Fahrenheit
- Output can drive loads up to 35V
- Internal stable voltage reference
- Low cost

Block Diagram

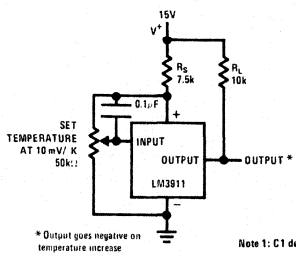


Typical Applications

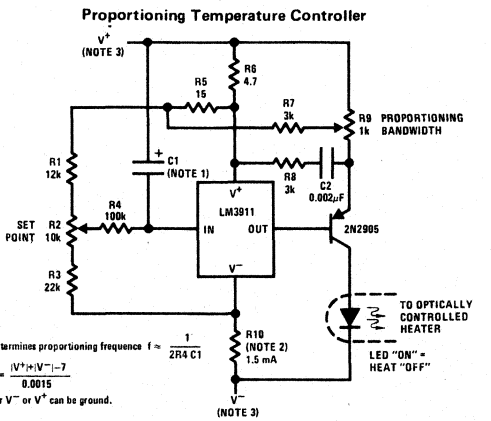
Ground Referred Centigrade Thermometer



Basic Temperature Controller



Proportioning Temperature Controller



Absolute Maximum Ratings

Supply Current (Externally Set)	10 mA	Operating Temperature Range	−25°C to +85°C
Output Collector Voltage, V^{++}	36V	Storage Temperature Range	−65°C to +150°C
Feedback Input Voltage Range	0V to +7.0V	Lead Temperature (Soldering, 10 seconds)	300°C
Output Short Circuit Duration	Indefinite		

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SENSOR					
Output Voltage	T_A = −25°C, (Note 2)	2.36	2.48	2.60	V
Output Voltage	T_A = 25°C, (Note 2)	2.88	2.98	3.08	V
Output Voltage	T_A = 85°C, (Note 2)	3.46	3.58	3.70	V
Linearity	ΔT = 100°C		0.5	2	%
Long-Term Stability			0.3		%
Repeatability			0.3		%
VOLTAGE REFERENCE					
Reverse Breakdown Voltage	1 mA ≤ I_Z ≤ 5 mA	6.55	6.85	7.25	V
Reverse Breakdown Voltage Change With Current	1 mA ≤ I_Z ≤ 5 mA		10	35	mV
Temperature Stability			20	85	mV
Dynamic Impedance	I_Z = 1 mA		3.0		Ω
RMS Noise Voltage	10 Hz ≤ f ≤ 10 kHz		30		μV
Long Term Stability	T_A = +85°C		6.0		mV
OP AMP					
Input Bias Current	T_A = +25°C		35	150	nA
Input Bias Current			45	250	nA
Voltage Gain	R_L = 36k, V^{++} = 36V	2500	15000		V/V
Output Leakage Current	T_A = 25°C (Note 3)		0.2	2	μA
Output Leakage Current	(Note 3)		1.0	8	μA
Output Source Current	V_{OUT} ≤ 3.70	10			μA
Output Sink Current	1V ≤ V_{OUT} ≤ 36V	2.0			mA

Note 1: These specifications apply for −25°C ≤ T_A ≤ +85°C and 0.9 mA ≤ I_{SUPPLY} ≤ 1.1 mA unless otherwise specified; C_L ≤ 50 pF.

Note 2: The output voltage applies to the basic thermometer configuration with the output and input terminals shorted and a load resistance of ≥ 1.0 MΩ. This is the feedback sense voltage and includes errors in both the sensor and op amp. This voltage is specified for the sensor in a rapidly stirred oil bath. The output is referred to V^+.

Note 3: The output leakage current is specified with ≥ 100 mV overdrive. Since this voltage changes with temperature, the voltage drive for turn-off changes and is defined as V_{OUT} (with output and input shorted) −100 mV. This specification applies for V_{OUT} = 36V.

Application Hints

Although the LM3911 is designed to be totally trouble-free, certain precautions should be taken to insure the best possible performance.

As with any temperature sensor, internal power dissipation will raise the sensor's temperature above ambient. Nominal suggested operating current for the shunt regulator is 1.0 mA and causes 7.0 mW of power dissipation. In free, still, air this raises the package temperature by about 1.2°K. Although the regulator will operate at higher reverse currents and the output will drive loads up to 5.0 mA, these higher currents will raise the sensor temperature to about 19°K above ambient—degrading accuracy. Therefore, the sensor should be operated at the lowest possible power level.

With moving air, liquid or surface temperature sensing, self-heating is not as great a problem since the measured media will conduct the heat from the sensor. Also, there are many small heat sinks designed for transistors which will improve heat transfer to the sensor from the surrounding medium. A small finned clip-on heat sink is quite effective in free-air. It should be mentioned that the LM3911 die is on the base of the package and therefore coupling to the base is preferrable.

The internal reference regulator provides a temperature stable voltage for offsetting the output or setting a comparison point in temperature controllers. However, since this reference is at the same temperature as the sensor temperature changes will also cause reference drift. For application where maximum accuracy is needed an external reference should be used. Of course, for fixed temperature controllers the internal reference is adequate.

Typical Performance Characteristics

Temperature Conversion

$$T_{CENTIGRADE} = T_C$$

$$T_{FAHRENHEIT} = T_F$$

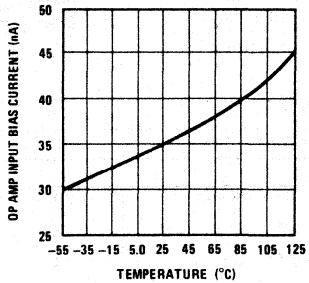
$$T_{KELVIN} = T_K$$

$$T_K = T_C + 273$$

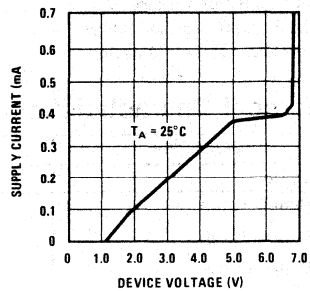
$$T_C = (40 + T_F)\ \frac{5}{9} - 40$$

$$T_F = (40 + T_C)\ \frac{9}{5} - 40$$

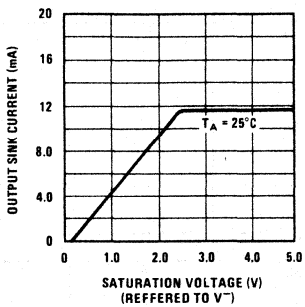
Op Amp Input Current



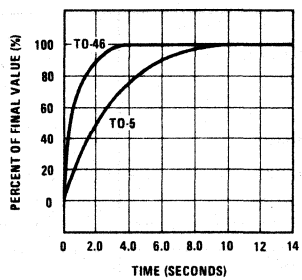
Power Supply Current



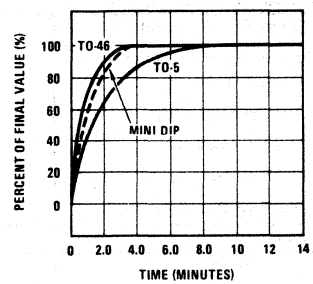
Output Saturation Voltage



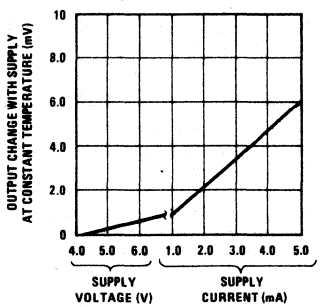
Thermal Time Constant in Stirred Oil Bath



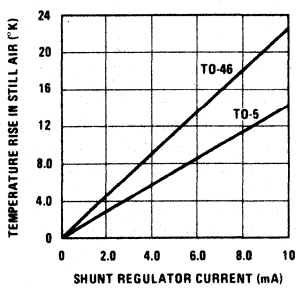
Thermal Time Constant in Still Air



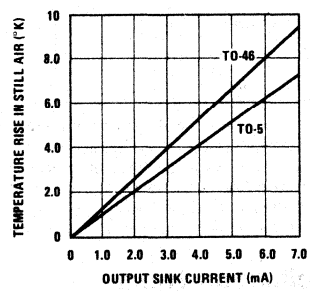
Supply Sensitivity



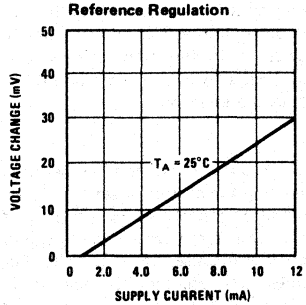
Device Temperature Rise



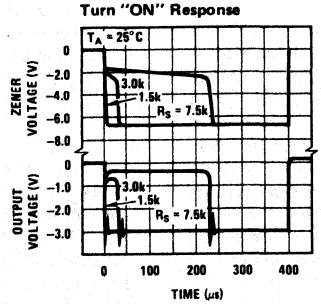
Device Temperature Rise



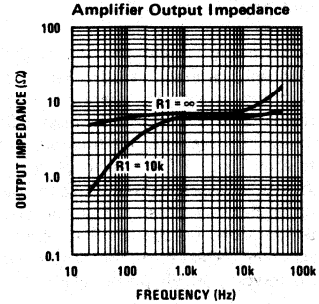
Reference Regulation



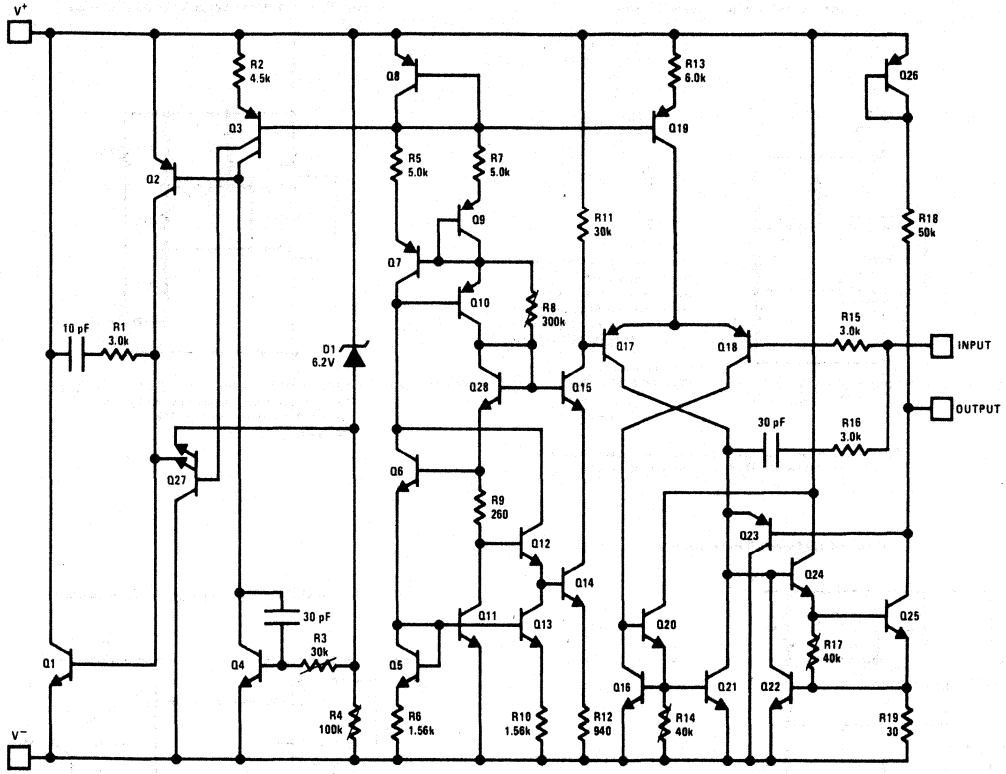
Turn "ON" Response



Amplifier Output Impedance

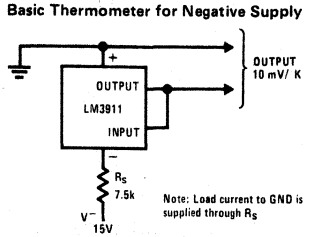


Schematic Diagram



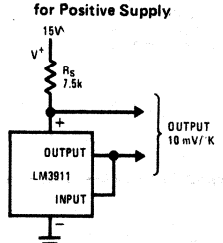
Typical Applications (Continued)

Basic Thermometer for Negative Supply



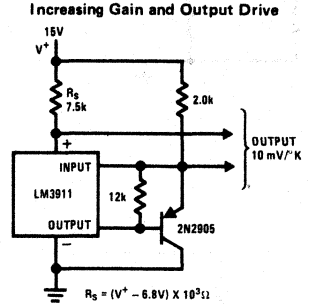
$R_S = (V^- - 6.8V) \times 10^3\Omega$

Basic Thermometer for Positive Supply



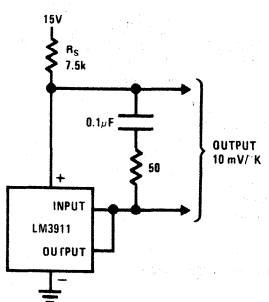
$R_S = (V^- - 6.8V) \times 10^3\Omega$

Increasing Gain and Output Drive

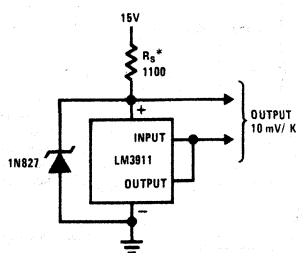


$R_S = (V^+ - 6.8V) \times 10^3\Omega$

External Frequency Compensation for Greater Stability when Driving Capacitive Loads

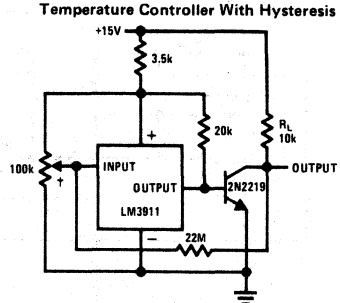


Operating With External Zener for Lower Power Dissipation and Ambient Reference



* Depends on Zener current.

Temperature Controller With Hysteresis

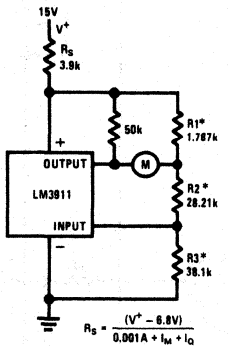


* Output goes positive on temperature increase

†Set temperature

Typical Applications (Continued)

Thermometer With Meter Output



$$R1^* = \frac{(V_Z)\,0.01\Delta T}{I_M\,(V_Z - 0.01\,T_O)}\ **$$

Select $I_Q \le \frac{2V}{R1}$

$$R2 = \frac{0.01\,T_O - I_Q\,R1}{I_Q}$$

$$R3 = \frac{V_Z}{I_Q} - R1 - R2$$

$\left(I_Q \le \frac{2V}{R1}\right)$

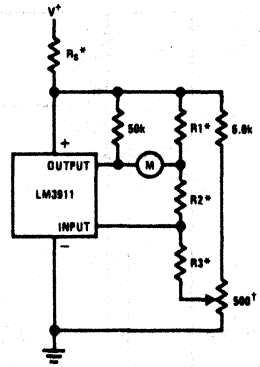
V_Z = Shunt regulator voltage (use 6.8V)
ΔT = Meter temperature span (°K)
I_M = Meter full scale current (A)
T_O = Meter zero temperature (°K)
I_Q = Current through R1, R2, R3 at zero meter current (10μA to 1.0 mA) (A)

$$R_S = \frac{(V^+ - 6.8V)}{0.001A + I_M + I_Q}$$

*Values shown for:
T_O = 300°K, ΔT = 100°K,
I_M = 1.0 mA, I_Q = 100 μA

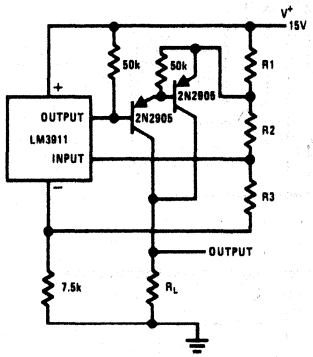
** The 0.01 in the above and following equations is in units of V/ K or V/ C, and is a result of the basic 0.01V/ K sensitivity of the transducer

Meter Thermometer With Trimmed Output



*Selected as for meter thermometer except T_O should be 5°K more than desired and I_Q = 100μA
†Calibrates T_O

Ground Referred Thermometer



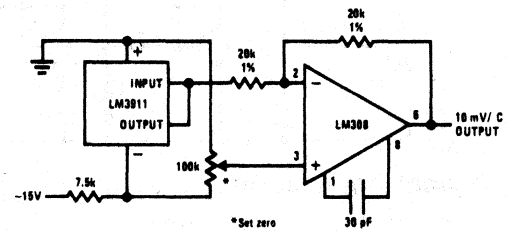
$$R1 = \frac{(V_Z)(10\,mV)(\Delta T)}{\frac{V_O}{R_L}\,(V_Z - 0.01\,T_O)}$$

$$R2 = \frac{0.01\,T_O - I_Q\,R1}{I_Q}$$

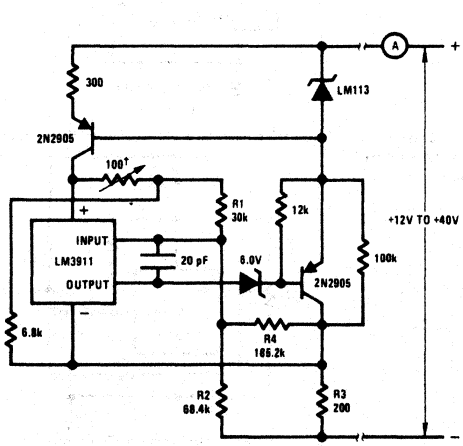
$$R3 = \frac{V_Z}{I_Q} - R1 - R2$$

V_Z = Shunt regulator voltage
ΔT = Temperature span (°K)
T_O = Temperature for zero output (°K)
V_O = Full scale output voltage ≤ 10V
I_Q = Current through R1, R2, R3 at zero output voltage (typically 100μA to 1.0 mA)

Ground Referred Centigrade Thermometer



Two Terminal Temperature to Current Transducer*



$$R2\ (\Omega) = \frac{\left(V_Z - 0.01\,T_L\right)\left(I_H - \frac{0.01\,T_H}{R1}\right) + \left(V_Z - 0.01\,T_H\right)\left(\frac{0.01\,T_L}{R1} - I_L\right)}{\frac{0.01}{R1\,R3}\left|T_H\,(V_Z - 0.01\,T_L) - T_L\,(V_Z - 0.01\,T_H)\right|}\ **$$

$$R3\ (\Omega) = \frac{V_Z\left(\frac{T_H}{T_L} - 1\right)}{I_H - \frac{I_L\,T_H}{T_L}}$$

$$\frac{1}{R4} = \frac{1}{(V_Z - 0.01\,T_L)(R2)}\left[\frac{(R2)(0.01\,T_L)}{R1} + \frac{\left(\frac{V_Z - 0.01\,T_L}{R2} - I_L\right)}{\frac{1}{R2} + \frac{1}{R3}}\right] - \frac{1}{R2}$$

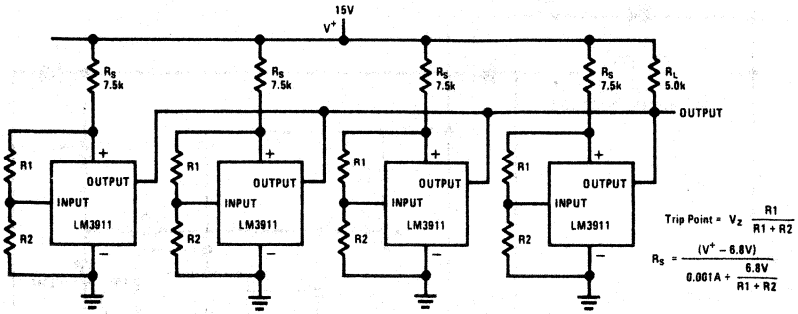
T_L = Temperature for I_L (°K)
T_H = Temperature for I_H (°K)
V_Z = Zener voltage (V)
I_L = Low temperature output current (A)
I_H = High temperature output current (A)

*Values shown for I_{OUT} = 1 mA to 10 mA for 70°F to 100°F
†Set temperature

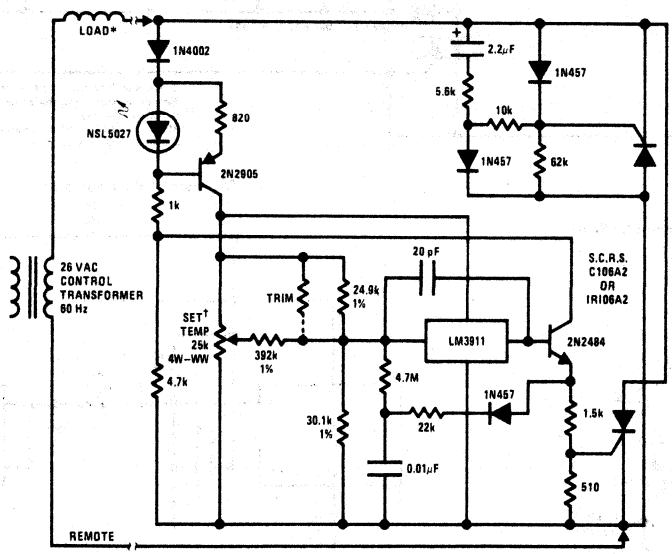
** The 0.01 in the above and following equations is in units of V/ K or V/ C, and is a result of the basic 0.01V/ K sensitivity of the transducer

Typical Applications (Continued)

Over Temperature Detectors With Common Output



Two-Wire Remote A.C. Electronic Thermostat (Gas or Oil Furnace Control)

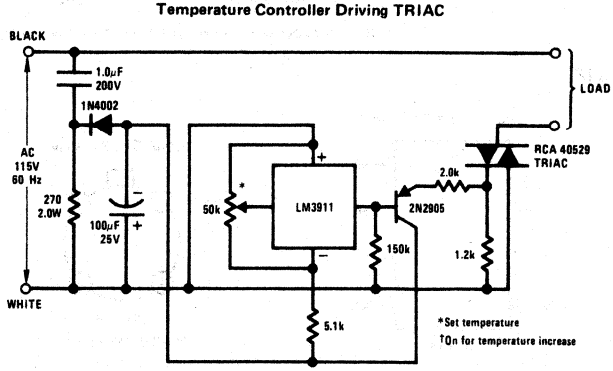


*Solenoid or 6–15W heater

†Pot will provide about a 50°F to 90°F setting range. The trim resistor (100k) is selected to bring 70°F near the middle of the pot rotation.

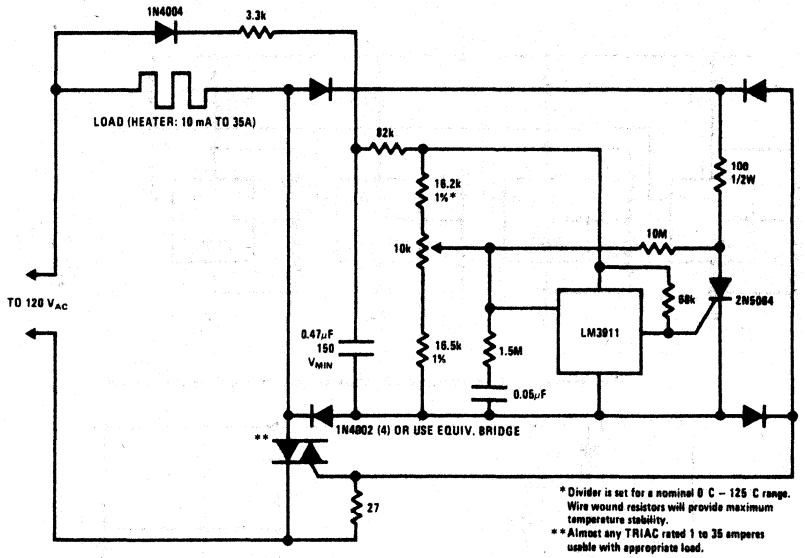
SCR heating, by proper positioning, can preheat the sensor giving control anticipation as is presently used in many home thermostats.

Temperature Controller Driving TRIAC



Typical Applications (Continued)

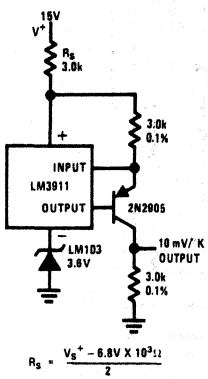
Three-Wire Electronic Thermostat



* Divider is set for a nominal 0 C – 125 C range. Wire wound resistors will provide maximum temperature stability.

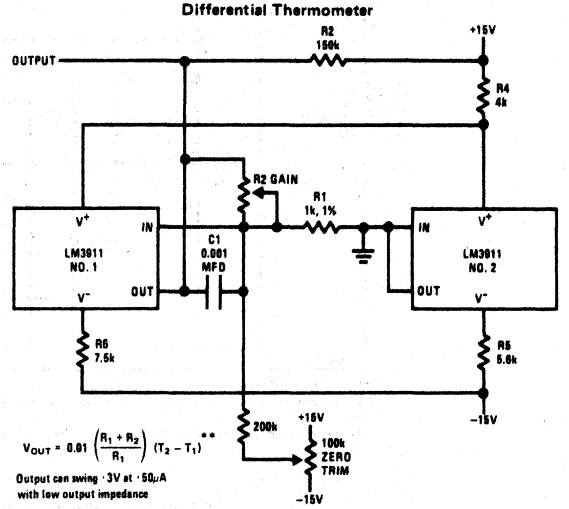
** Almost any TRIAC rated 1 to 35 amperes usable with appropriate load.

Kelvin Thermometer With Ground Referred Output



$$R_S = \frac{V_S^+ - 6.8V \times 10^3 \Omega}{2}$$

Differential Thermometer



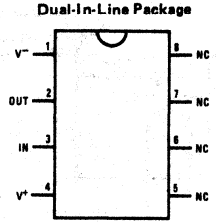
$$V_{OUT} = 0.01\left(\frac{R_1 + R_2}{R_1}\right)(T_2 - T_1)^{**}$$

Output can swing ·3V at ·50μA with low output impedance

** The 0.01 in the above equation is in units of V/ K or V/ C, and is a result of the basic 0.01 V/ K sensitivity of the transducer

Connection Diagram

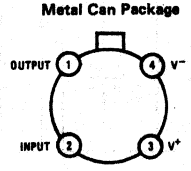
Dual-In-Line Package



TOP VIEW

Order Number LM3911N
See NS Package N08B

Metal Can Package



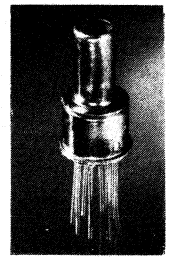
TOP VIEW

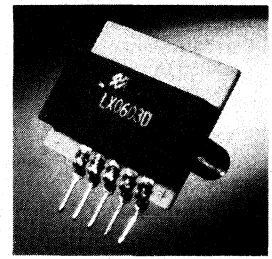
Note: Pin 4 connected to case.

Order Number LM3911H-46
See NS Package H04A

National Semiconductor

Monolithic Pressure Transducers LX05XXA, LX06XXD, LX06XXGB Series





General Description

The monolithic pressure transducers are piezoresistive integrated circuits which provide an output voltage proportional to applied pressure. The devices are provided in compact packages with pressure ports, suitable for PC board mounting and attachment of flexible tubing.

The LX05XXA is an absolute pressure transducer with a single pressure inlet tube axially aligned with its TO-5 package, suitable for use with non-ionic working fluids.

The LX06XXGB is a gage transducer with a single tube and an ambient inlet. It is well suited for use with package-compatible working fluids, including water.

The LX06XXD is a differential pressure transducer with 2 pressure ports, suitable for use with non-ionic working fluids in either pressure port, and package-compatible working fluids in the positive pressure port.

See Application Guide — Media Compatibility

Advantages of Monolithic

The monolithic transducers include only the basic monolithic pressure IC chip used in National's hybrid pressure transducer products. This greatly reduces unit cost and allows the electronic designer greater freedom in implementing transducer circuits. The monolithic transducer is temperature compensated with respect to sensitivity and features low offset temperature coefficient. High sensitivity and low noise allow easy amplification. These devices are especially useful in applications requiring battery power, circuit flexibility, or compatibility with microprocessors.

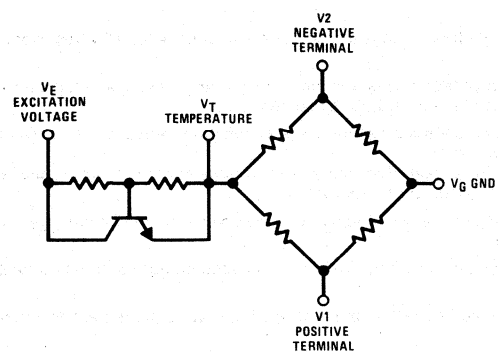
Features

- Low cost
- Interface circuit flexibility
- Temperature compensation of span
- Compact, PC board compatible
- Low noise
- High natural frequency
- Low volumetric displacement
- Separate temperature-sensitive output

Applications

- Automated equipment
- Residential, commercial and industrial controls
- Medical diagnostics
- Automotive diagnostics and controls
- Machine tool controls
- Barometry

Schematic Diagram



Pin Connections

Symbol	LX05XX	LX06XX
V_E	3	5
V_T	7	1
V1	6	3
V2	5	4
V_G	8	2

This edition supersedes the August 1979 Monolithic Pressure Transducer specifications

LX0503A, LX0603D, LX0603GB Characteristics

Absolute Maximum Ratings

Excitation Voltage V_E	12V
Temperature Range	−40°C to +105°C
Pressure Range	
LX0503A	100 psia
LX0603D	−100 psid
	45 psid
LX0603GB	45 psig
Common Mode Line Pressure, LX0603D	400 psig
Bridge Voltage, V_T	$\leq V_E$
Lead Temperature (Soldering, 10 seconds)	260°C

Reference Conditions

Excitation Voltage, V_E	7.5V
Reference Temperature	25°C
Reference Temperature Range	0°C to 85°C
Offset Reference Pressure	
LX0503A	0 psia
LX0603D	0 psid
LX0603GB	0 psig
Common Mode Line Pressure, LX0603D	0 psig

Performance Characteristics

DEVICE TYPE	OPERATING PRESSURE RANGE	GUARANTEED SPECIFICATIONS					
		OFFSET CHARACTERISTICS (NOTE 5)			SPAN CHARACTERISTICS (NOTE 6)		
		OFFSET CALIBRATION	REPEATABILITY (NOTE 1)	STABILITY (NOTE 2)	SENSITIVITY CALIBRATION	LINEARITY, HYSTERESIS & REPEATABILITY (NOTE 3)	STABILITY (NOTE 2)
		mV	±%FS	±%FS	mV/psi	±%S	±%S
LX0503A	0 to 30 psia	0 ± 100	0.4	1.7	2 to 8	0.67	0.3
LX0603D	±30 psid	0 ± 100	0.4	8	2 to 8	1.33	0.3
LX0603GB	vacuum to 30 psig	0 ± 100	0.4	1.1	2 to 8	0.67	0.3

DEVICE TYPE	OPERATING PRESSURE RANGE	TYPICAL CHARACTERISTICS					
		OFFSET TEMPERATURE COEFFICIENT (NOTE 5)	SPAN TEMPERATURE COEFFICIENT (NOTE 6)	BIAS CURRENT	BRIDGE RESISTANCE	DIAPHRAGM NATURAL FREQUENCY	COMPENSATION CIRCUIT TEMPERATURE COEFFICIENT (NOTE 4)
		%FS/°C	%S/°C	mA	kΩ	kHz	mV/°C
LX0503A	0 to 30 psia	−0.050	−0.015	2.0	1.8	50	−10.0
LX0603D	±30 psid	−0.025	−0.015	2.0	1.8	50	−8.0
LX0603GB	vacuum to 30 psig	−0.033	−0.015	2.0	1.8	50	−8.0

Specification Notes

Note 1: Offset Repeatability — the transducer's ability to reproduce offset voltage at constant temperature (25°C) when exposed to a maximum of 50 full pressure range cycles.

Note 2: Stability — the transducer's ability to reproduce the output voltage corresponding to a specific pressure and temperature in a period of one year during which permitted operating and storage conditions are not exceeded.

Note 3: Linearity — the maximum deviation of measured output over the full pressure range at constant temperature (25°C) from the best straight line intersecting the output at the offset reference pressure.

Hysteresis and Span Repeatability — the transducer's ability to reproduce any output voltage over the full pressure range at constant temperature (25°C) when exposed to a maximum of 50 full pressure range cycles.

Note 4: Compensation Circuit Temperature Coefficient $\Delta V_{ET}/\Delta T$, the change in voltage across the compensation circuit, $V_{ET} = V_E - V_T$, as the temperature changes within the permitted operating range.

Note 5: Offset errors are independent of applied pressure and specified as %FS, percent of full span operating pressure range. See Application Guide.

Note 6: Span errors are proportional to applied pressure and specified as %S, percent of span operating pressure. See Application Guide.

LX0520A, LX0620D, LX0620GB Characteristics

Absolute Maximum Ratings

Excitation Voltage, V_E	12V
Temperature Range	−40°C to +105°C
Pressure Range	
LX0520A	200 psia
LX0620D	−200 psid
	150 psid
LX0620GB	150 psig
Common Mode Line Pressure, LX0620D	400 psig
Bridge Voltage, V_T	$\leq V_E$
Lead Temperature (Soldering, 10 seconds)	260°C

Reference Conditions

Excitation Voltage, V_E	7.5V
Reference Temperature	25°C
Reference Temperature Range	−40°C to 85°C
Offset Reference Pressure	
LX0520A	0 psia
LX0620D	0 psid
LX0620GB	0 psig
Common Mode Line Pressure, LX0620D	0 psig

Performance Characteristics

DEVICE TYPE	OPERATING PRESSURE RANGE	GUARANTEED SPECIFICATIONS					
		OFFSET CHARACTERISTICS (NOTE 5)			SPAN CHARACTERISTICS (NOTE 6)		
		OFFSET CALIBRATION	REPEATABILITY (NOTE 1)	STABILITY (NOTE 2)	SENSITIVITY CALIBRATION	LINEARITY, HYSTERESIS & REPEATABILITY (NOTE 3)	STABILITY (NOTE 2)
		mV	±%FS	±%FS	mV/psi	±%S	±%S
LX0520A	0 to 100 psia	0 ± 50	0.4	1.2	0.2 to 0.8	0.67	0.3
LX0620D	±100 psid	0 ± 50	0.4	0.6	0.2 to 0.8	1.33	0.3
LX0620GB	vacuum to 100 psig	0 ± 50	0.4	1.0	0.2 to 0.8	0.67	0.3

DEVICE TYPE	OPERATING PRESSURE RANGE	TYPICAL CHARACTERISTICS					
		OFFSET TEMPERATURE COEFFICIENT (NOTE 5)	SPAN COEFFICIENT (NOTE 6)	BIAS CURRENT	BRIDGE RESISTANCE	DIAPHRAGM NATURAL FREQUENCY	COMPENSATION CIRCUIT TEMPERATURE COEFFICIENT (NOTE 4)
		%FS/°C	%S/°C	mA	kΩ	kHz	mV/°C
LX0520A	0 to 100 psia	−0.15	−0.02	2.0	1.8	100	−10.0
LX0620D	±100 psid	−0.08	−0.02	2.0	1.8	100	−8.0
LX0620GB	vacuum to 100 psig	−0.13	−0.02	2.0	1.8	100	−8.0

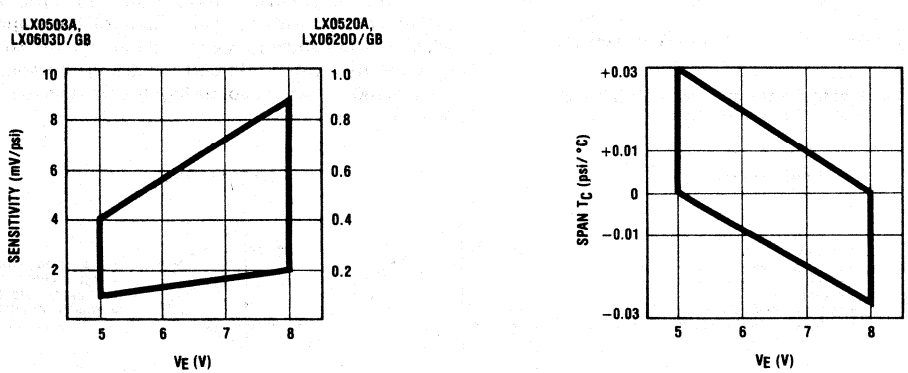


Figure 1. Typical Ranges of Sensitivity and Span TC vs. Applied Voltage V_E for LX05XXA and LX06XXD, GB Pressure Transducers

Application Guide

Accuracy Specifications — Autoreferencing

Error parameters are specified separately for offset and span. These errors are independent which allows easy computation of error bands, recalibration, and use of autoreferencing, a technique of automatic recalibration. The following describes the basic use of these error parameters. For a detailed discussion, see Application Note AN246.

Span Accuracy

Span errors are proportional to applied pressure and specified as %S, percent of span. The span error in psi is given by:

$$\text{Span Error} = \frac{(\%S)}{100} \times |P_A - P_{REF}|$$

where $|P_A - P_{REF}|$ is the absolute value of applied pressure P_A as measured from the offset reference P_{REF}. This produces error bands as exemplified in Figure 2. Note that at the reference pressure, span errors are zero, and the only errors are in offset.

Offset Accuracy

Offset errors are constant with pressure and given as %FS, where FS is full span voltage or operating pressure range. For example, the pressure range of the LX0620GB is vacuum to 100 psig, 115 psig full span, and the specified offset stability is ±1.0%FS. The error in psi is therefore:

$$\text{Offset Stability (LX0620GB)} = \frac{1.0\%}{100} \times 115\,\text{psi} = \pm 1.15\,\text{psi}$$

Since offset errors are independent of applied pressure they can be fully or partially "calibrated out" by manual referencing or autoreferencing at any known pressure, normally the specified offset reference pressure. For a full discussion of autoreferencing, see Section 7 of the 1977 Pressure Transducer Handbook.

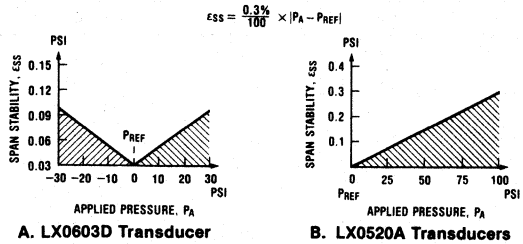


Figure 2. Span Stability Error Bands for LX0603D and LX0520A Monolithic Transducers

Consulting the Handbook

The 1977 Pressure Transducer Handbook should be consulted before using any National pressure transducer product. The handbook was written for hybrid transducers and includes comprehensive information on pressure transducer installation, specifications, accuracy, auto-referencing, and many applications. In consulting the handbook relative to monolithic pressure transducers, it is important to note that monolithic devices are not fully signal conditioned and require additional circuitry for the applications described.

Signal Conditioning

The illustration of pressure transducer symbols (*Figure 3*) shows the level of signal conditioning for both hybrid and monolithic transducers. The essential difference is that the hybrid device includes scaling and buffering, with a single-ended high level output and offset temperature compensation. Effective application of the monolithic device will require external circuits to perform these functions. The included Application Hints provide guidance in designing such circuits. The three Example Circuits illustrate designs for low cost, high sensitivity, and digital interface applications.

Media Compatibility — Humidity

The heart of the transducer is a monolithic silicon chip with a cavity etched out to form a diaphragm. The top side of the diaphragm contains the transducer pressure sensing circuitry.

As shown in *Figure 4a*, the LX05XXA has a single pressure inlet that allows the working fluid to make contact with the circuit side of the diaphragm. This area is covered with a thin, compliant layer of parylene. Parylene does not protect against water and other aqueous and ionic fluids. Therefore, these must be kept out of the pressure inlet to avoid electrical failure.

As shown in *Figure 4b*, the LX06XX series transducers have 2 pressure inlets which differ in susceptibility to moisture and other fluids. The ambient pressure port (or negative pressure port for differential devices) allows the working fluid to make contact with the circuit side of the diaphragm and thus requires the same precautions discussed relative to the LX05XXA above. The working fluid port (or positive pressure port, for differentials) makes contact with the cavity side of the diaphragm, which is insensitive to water and ionic fluids. The main criterion for fluid in this port is package compatibility. That is, the fluid must not be highly corrosive to brass or silicon.

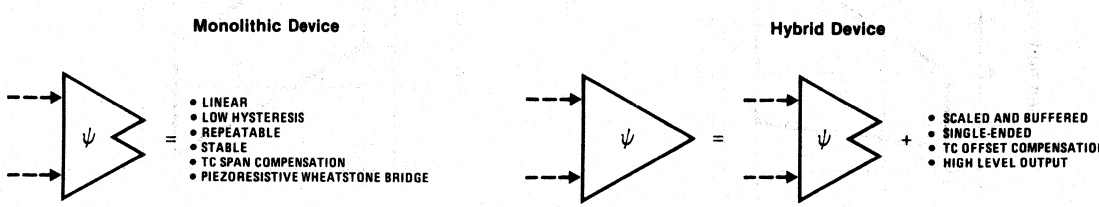


Figure 3. Pressure Transducer Symbols

Hence, the LX06XXGB can operate with aqueous working fluids but water must be kept out of the ambient inlet during operation. Similarly, the LX06XXD can operate with aqueous working fluids in the negative pressure port, but must be protected from aqueous fluids in the positive port. Both devices can be adversely affected by very high humidity ambient conditions.

Leak Rate

PX5 and PX6 packages are not hermetic. National's pressure transducers are guaranteed to have an effective leak area less than $10^{-7}cm^2$ as defined in App. Note AN232. Each transducer is leak tested at room temperature with 45 psig compressed air.

However, the user should be aware that the leak rate can depend on the type, viscosity, pressure, and temperature of the fluid and can increase with fatigue resulting from pressure cycling. This is especially important in static systems where a fluid under pressure is to be maintained for an extended period in an enclosure without replenishment. In such cases it may be necessary to enclose the LX05XXA in the pressure vessel and bring the leads out via a hermetic feedthrough connector installed in the enclosure wall.

"Dead-Ending" Feature

If the pressure applied to the LX05XXA greatly exceeds proof pressure (maximum specified operating pressure), the silicon diaphragm could rupture. But, unlike gage transducers, the absolute devices are "dead-ended" so that diaphragm rupture does not necessarily result in fluid leakage.

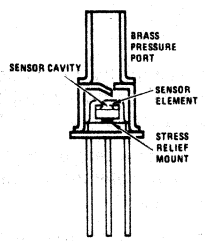


Figure 4a. LX05XXA Pressure Transducer Structure

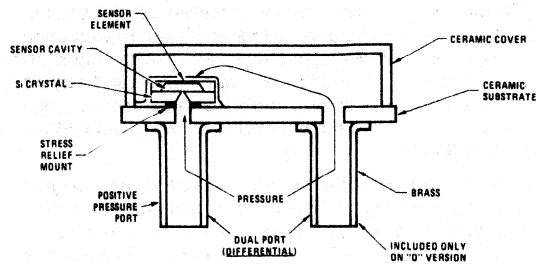


Figure 4b. LX06XX Pressure Transducer Structure

Application Hints

Hint 1. Input/Output Polarity

The LX05XXA transducer output signals, pins 6 and 5, are taken directly from a Wheatstone bridge. Pin 6 is the positive signal output. It goes positive when the absolute pressure increases. Pin 5, the negative signal output, goes negative (less positive) when the absolute pressure increases. *Figure 5a* shows a bottom view of the TO-5 pinout.

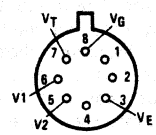


Figure 5a. LX05XXA Pinout, Bottom View

The LX06XX series transducer output signals, pins 3 and 4, are taken directly from a Wheatstone bridge. Pin 3 is the positive signal output. It goes positive when pressure is increased at the left-most port as viewed from the bottom of the device as shown in *Figure 5b*. Pin 4 is the negative signal output. It goes negative (less positive) when the pressure is increased at the left-most port. The left-most port is the *positive port* for the LX06XXD and the *gage pressure port* for the LX06XXGB.

Hint 2. Bridge Buffering

Interfacing with the diffused piezoresistive Wheatstone bridge is the most critical step in signal conditioning. If designed and fabricated properly, the interface/buffer circuit will provide high gain and minimum interaction of temperature coefficients. This greatly simplifies subsequent signal conditioning and processing.

The diffused bridge has a resistance of approximately 1800Ω at room temperature. Severe bridge loading by external resistors (i.e., low value resistors with temperature coefficients very different than that of the bridge) cause distortion of transducer characteristics and temperature coefficients. The most effective bridge buffering circuits use very high impedance, well-matched, carefully installed resistors. High quality instrumentation amplifiers can also be used (see Example Circuits, *Figure 7*).

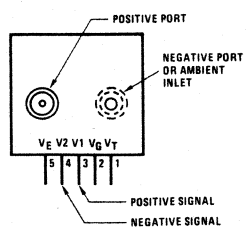


Figure 5b. LX06XX Pinout, Portside View

Hint 3. Calibration and Scaling

The principal problem encountered in calibration and scaling of a transducer is the interaction of offset (common-mode) and span (normal-mode) parameters and their temperature coefficients. Since most signal conditioning circuits have this problem, it is important to make span-offset independence a prime criterion from the outset. The rewards are easy calibration, simple scaling, and a natural interface with auto-referencing. (See Hint 8 and Section 7 of the handbook for auto-reference discussions.) The simplest technique for effective reduction of span-offset interaction requires the use of 2 amplifier stages. Step-by-step procedure is given in the individual circuit discussions.

Hint 4. Temperature Compensation

The span temperature compensation circuit built into the monolithic device is adequate for most users. It requires V_E to be regulated at 7.5V and repeatable with temperature. As shown in *Figure 1*, improved span temperature compensation can be achieved simply by tailoring V_E to the specific device. To select the best excitation voltage, vary temperature slowly while switching pressure between high and low operating levels and varying V_E. When the difference in output at high and low pressures (span voltage) remains constant with temperature, V_E is optimum.

For improved offset temperature compensation a signal conditioning circuit can be used. To adjust the temperature compensation circuit, vary the temperature slowly while trimming the appropriate resistor to minimize the output voltage rate of change. The method requiring the lowest parts count uses a low temperature coefficient, high value resistor (see *Figure 6*, R5). A more effective method is to use the temperature sensitive output, V_T, to feed a compensating signal to the summing junction of the output stage (see *Figure 7*). With either of these methods, auto-referencing can provide further improvement.

Hint 5. Uses of V_T Pin

As discussed in Hint 4, V_T can be used for offset temperature compensation if the voltage applied to V_E is well regulated and repeatable with temperature. It can also be characterized as a temperature sensor, if desired. In either case, the V_T pin cannot be allowed to source or sink more than 25μA in this circuit configuration. The preferred method of buffering is shown in the High Sensitivity Circuit.

For applications that do not require span temperature compensation, such as those having a limited temperature range within their duty cycles, the excitation voltage can be applied to pin V_T instead of to V_E. This bypasses the internal span temperature coefficient compensation circuit and provides the following potential advantages:

1. Sensitivity is greater with the same excitation voltage applied directly to the bridge.
2. Applied voltage can be other than 7.5V. For example, 5V can be used for compatibility with logic systems.
3. The bridge is inherently ratiometric in the absence of the span temperature compensation circuit (see Hint 6).

These advantages can be realized along with span temperature compensation if a temperature sensitive supply (1500 ppm/°C to 2000 ppm/°C) is applied to V_T.

IMPORTANT: V_T must never be more positive than V_E. To prevent this when applying excitation to V_T, connect V_T to V_E.

Hint 6. Supply Voltage Sensitivity — Regulation

As illustrated in *Figure 1*, the change in sensitivity of the transducer with supply voltage is governed by the equation:

$$S_p \cong k(V_E - V_{ET})$$

where S_p is the sensitivity in mV/psi, V_E is applied voltage, and k is a device dependent constant relating sensitivity to the supply voltage in mV/psi/V.

The voltage, V_{ET} is a constant of the temperature compensation circuit, nominally 3V for the LX06XX and 4V for the LX05XX devices.

To determine k for a device, set V_E to some nominal value, say 7.5V, then measure S_p and V_{ET}. If S_p is found to be 4.5 mV/psi and V_{ET} is 3V, for example, then $k = 1$ mV/psi/V.

True ratiometricity ($S_p = k V_E$) is realized at the expense of internal temperature compensation by applying excitation voltage to V_T instead of V_E as discussed in Hint 5.

Hint 7. Noise Suppression — Mechanical/Electrical

Noise in a pressure transducer arises from both mechanical and electrical sources. Careful attention to both is required in applying transducers for high accuracy and trouble-free performance.

The most prevalent source of common-mode noise is in the input pressure line. The monolithic pressure transducer will accurately sense all mechanical and thermo-mechanical effects, including those in the acoustic domain. Where acoustics are parasitic, snubbing (i.e., constricting the input pressure orifice to slow the signal) is recommended. Hydro-thermal effects can be minimized by understanding and avoiding creation of a "hot-bulb thermometer" in the plumbing (see sections 5 and 13 of the handbook).

Electrical noise can also be minimized by certain standard practices. These include: keeping resistor leads to summing junctions short; using low noise amplifiers (such as the LH0044); and decoupling the supply by capacitive bypass. With the monolithic transducer, it is also possible to decouple V_T to ground and filter the first amplifier stage. A low noise regulator (such as the LM329) should also be used in the supply circuit.

Hint 8. Auto-Referencing

Auto-referencing is a family of techniques for compensating errors in pressure transducers by using a known reference pressure. Originally introduced by National and discussed comprehensively in section 7 of the 1977 Pressure Transducer Handbook, these techniques, because of the high accuracy they provide, are now finding widespread application.

WARNING

When soldering or cleaning transducers, the pressure inlet ports (including the ambient port) must be protected from harmful contaminants, such as flux and acidic fumes.

Example Circuits

All Example Circuits accommodate independent span and offset adjustability, and allow the use of auto-referencing and the preceding application hints.

Low Cost Circuit — *Figure 6*

Dual supply, zener reference, and 2-stage amplification provide a temperature compensated zero-based output characteristic:

Step No. 1 Offset Temperature Compensation: Monitor the output while slowly varying temperature. Select R5 value and connection to minimize the change in output with a change in temperature.

Step No. 2 Offset Adjust: Monitor the output. Select R6 value and conection to achieve 0V output.

Step No. 3 Span Adjust: Monitor output while applying full-scale pressure. Select R10 value to achieve desired full-scale voltage.

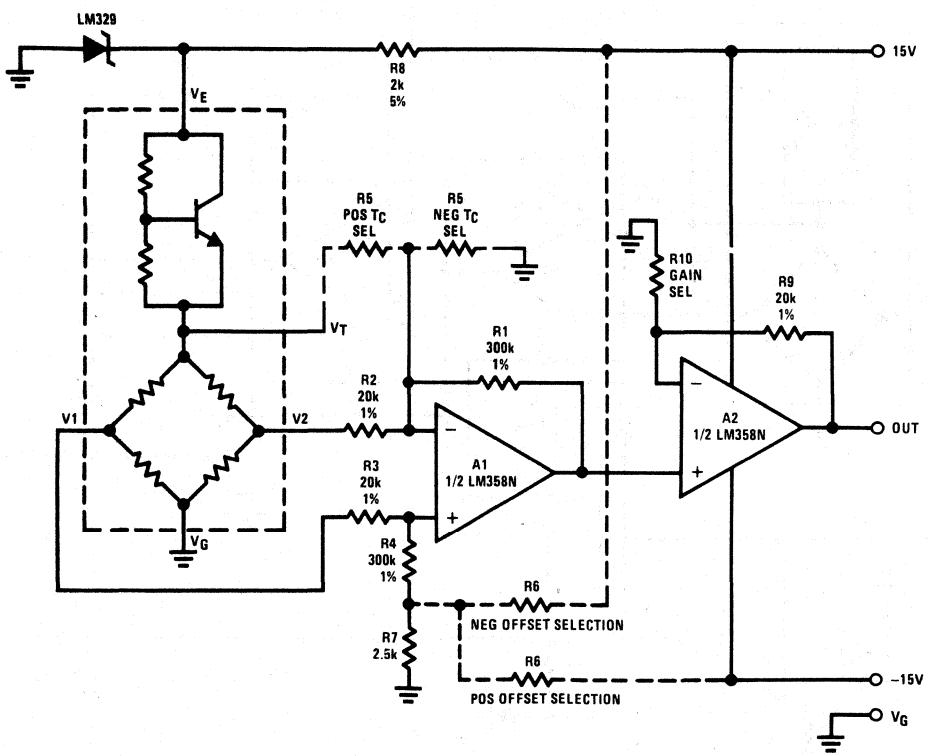


Figure 6. Low Cost/Zero Based

Example Circuits (Continued)

High Sensitivity Circuit — *Figure 7*

This circuit has a dual supply, buffered zener reference, low noise first stage amplification, isolated offset temperature coefficient compensation, 2-stage amplification, and provides a fully temperature compensated, high sensitivity, zero-based output characteristic.

Step No. 1 Span Temperature Compensation: Vary temperature slowly while switching input pressure between very high and low operating levels and varying R1. When the difference in output voltage at high and low pressures remains constant with temperature, R1 is optimum.

Step No. 2 Initial Offset Adjust: Monitor the voltage at point D, the first stage amplifier output. Select R12 value and connection to achieve 0V at point D.

Step No. 3 Second Offset Adjust: Monitor the voltage at point E. Select R7 value to achieve 0V at point E.

Step No. 4 Span Adjust: Monitor the output while applying full-scale pressure. Select R16 value to achieve desired full-scale voltage.

Step No. 5 Offset Temperature Compensation: Monitor the output while slowly varying temperature. Select the value and connection of R6 to minimize change in output with change in temperature. Alternatively, the value of R6 can be chosen analytically. Measure the change in output voltage (ΔV) resulting from a known change in temperature (ΔT). The compensation resistor value can then be chosen in accordance with the equation: R6 ≅ 1600 ΔT/ΔV; where R6 is in ohms, ΔT is in degrees Centigrade, and ΔV is in volts.

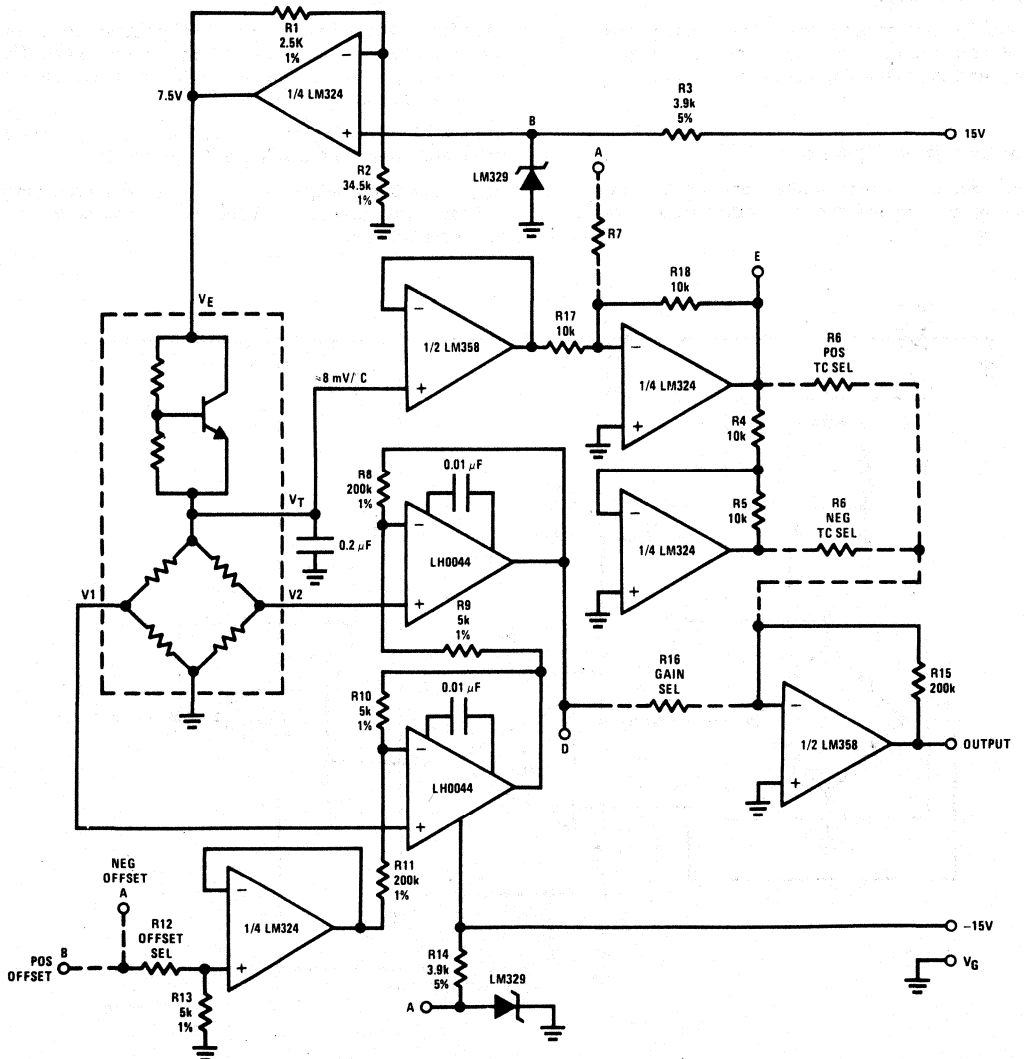


Figure 7. High Sensitivity Circuit

Example Circuits (Continued)

FM Output Circuit — *Figure 8*

A single supply, zener reference, 2-stage amplification, and voltage to frequency converter provide a frequency output compatible with analog-to-digital converter or microprocessor input.

Step No. 1 Offset Temperature Compensation: Monitor point A while slowly varying temperature. Select R4 value and connection to minimize change in temperature.

Step No. 2 DC Offset Adjust: Monitor point A and point B. Select R5 value to achieve zero difference voltage between points A and B.

Step No. 3 Frequency Offset Adjust: Monitor frequency output. Select R18 value to achieve desired frequency offset (1 kHz for circuit values shown).

Step No. 4 Frequency Span Adjust: Monitor frequency output while applying full-scale pressure. Select R12 value to achieve desired full-scale frequency (maximum output frequency is 10 kHz for circuit values shown, see LM331 data sheet).

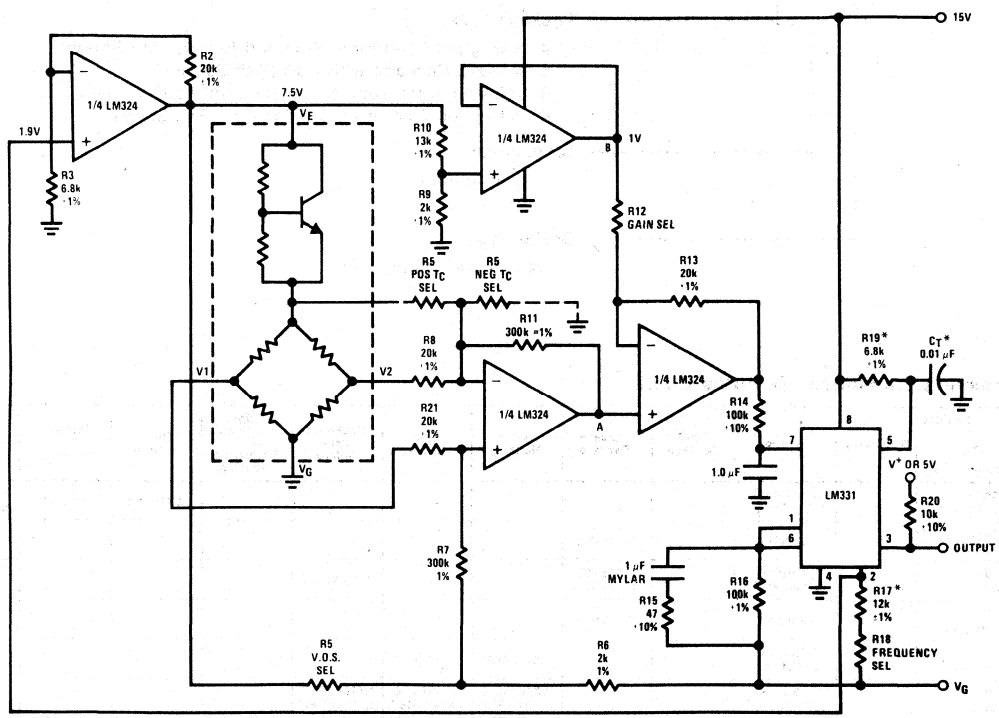


Figure 8. Frequency Output

Pressure Transducer Selection Guide

Ordering Information

LX 0 6 20 G B

Standard Option
- B = Backward Gage Version (PX6B, PX8B)
- N = Nylon Housing (PX8N, PX8BN)
- S = Stainless Steel Package (PX4S)
- Z = Zinc Housing (PX8Z, PX8BZ, PX8DZ)
- BN = Combine B and N Options
- BZ = Combine B and Z Options
- F = Fluid Filled Version (PX4F)
- FS = Combine F and S Options (PX4FS)

Pressure Type
- A = Absolute
- D = Differential
- G = Gage

Pressure Range (Characteristics Table)

Package Type
- 4 = Rugged Cylindrical Plumbed Fitting (PX4 Series)
- 5 = TO-5 Package with Port (PX5 Series)
- 6 = Ceramic Package for PCB Mounting (PX6 Series)
- 8 = Rugged Zinc or Nylon Housing (PX8 Series)

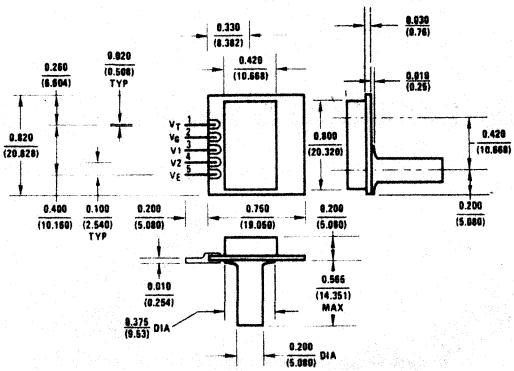
Technology
- 0 = Monolithic
- 1 = Hybrid

Device Type
- LX = Linear Transducer

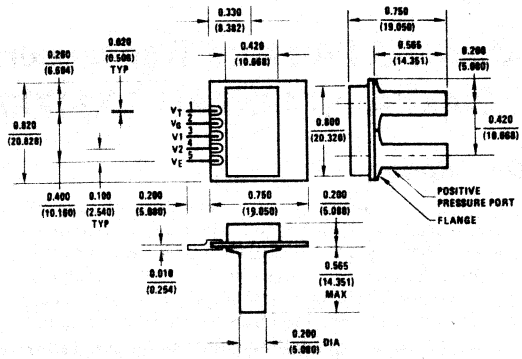
Pressure Transducer Features Chart

Feature / Product	Monolithic	Hybrid	TO-5 Package	Ceramic Package	Nylon Housing	Zinc Housing	Backward Gage Isolator	High Common-Mode Differential Housing	Brass Housing	Stainless Steel Housing	Fluid Filled Isolator
LX14XX Absolute		LX14XXA(S) LX14XXAF(S)							LX14XXA	LX14XXAS	LX14XXAF LX14XXAFS
LX16XX Absolute		LX16XXA		LX16XXA							
LX16XX Gage		LX16XXG LX16XXGB		LX16XXG LX16XXGB			LX16XXGB				
LX16XX Differential		LX16XXD		LX16XXD							
LX18XX Absolute		LX18XXAZ LX18XXAN			LX18XXAN	LX18XXAZ					
LX18XX Gage		LX18XXG(N) LX18XXGB(N)			LX18XXGN LX18XXGBN	LX18XXGZ LX18XXGBZ	LX18XXGBZ LX18XXGBN				
LX18XX Differential		LX18XXDZ				LX18XXDZ		LX18XXDZ			
LX05XX Absolute	LX0503A LX0520A		LX0503A LX0520A								
LX06XX Gage	LX0603GB LX0620GB			LX0603GB LX0620GB			LX0603GB LX0620GB				
LX06XX Differential	LX0603D LX0620D			LX0603D LX0620D							

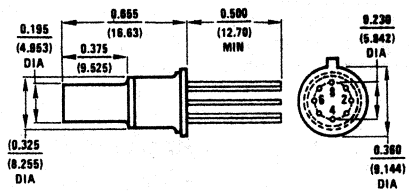
Physical Dimensions inches (millimeters)



PX6B (LX06XXGB)
0.2″ Port, Pressure Transducer Package
Weight: 5 grams



PX6D (LX06XXD)
0.2″ Port, Pressure Transducer Package
Weight: 5 grams



PX5A (LX05XXA)
8-Lead TO-5, Absolute Pressure Transducer Package
Weight: 1.5 grams

Warranty

National Semiconductor Corporation warrants that its products shall be free from defects in workmanship and materials, and shall conform to National's published specifications, or other specifications accepted by National in writing for a period of one (1) year from the date of National's shipment.

Limitation of Warranty Liability:

This warranty does not apply to any products which have been subject to misuse, neglect, accident, or modification. National's sole obligation under its warranty shall be to replace the product or issue credit. National's warranty and remedies are exclusive and are made expressly in lieu of all other warranties expressed or implied, either in fact or by operation of law, statutory or otherwise, including warranties of merchantability and fitness for use. National shall not be liable for damages due to delays in deliveries or use and shall in no event be liable for incidental or consequential damages of any kind, whether arising from contract, tort, or negligence, including but not limited to, loss of profits, loss of customers, loss of goodwill, overhead, or other like damages. No National product may be used in a life support application.

Limitation of Application Liability:

National assumes the buyer to be expert in his intended application of National's products. National claims no special expertise in the application of its products into the buyer's equipment. National accepts no responsibility for the buyer's selection and use of National's products. Buyer's interpretation and implementation of application suggestions and recommendation by National, general or specific, transmitted verbally or in writing, published or unpublished, is strictly at the buyer's own risk.

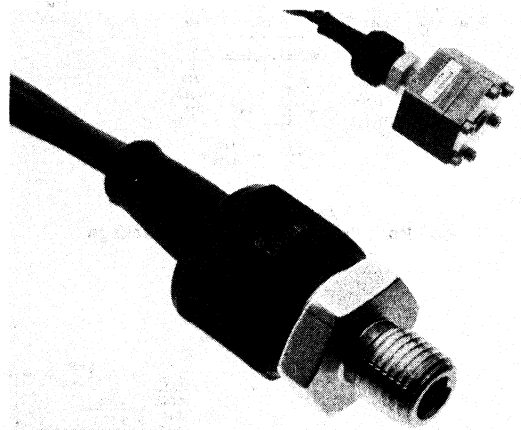
National Semiconductor

Absolute Pressure Transducers
LX14XXA, LX14XXAF, LX14XXAS, LX14XXAFS Series

Description

The LX14XX Series provides a selection of ruggedly packaged absolute transducers with operating pressure ranges of 0-100 psia to 0-5000 psia. These devices feature the compact concentric PX4 brass or PX4S stainless steel housing for easy installation with a crescent wrench and ten-inch flying leads for easy soldering and secure electrical connection. The leads are epoxy-sealed to provide protection against hostile exterior environments. Fluid-filled housings PX4F and PX4FS are also available for systems using corrosive or conductive working fluids

Like other National IC pressure transducers, the LX14XXA units are designed to provide high accuracy and excellent stability. They are field interchangeable and can be easily interfaced with auto-reference, control and display systems. Each device includes internal temperature compensation, voltage regulation and full signal conditioning by an operational amplifier with a low-impedance 10V output span.



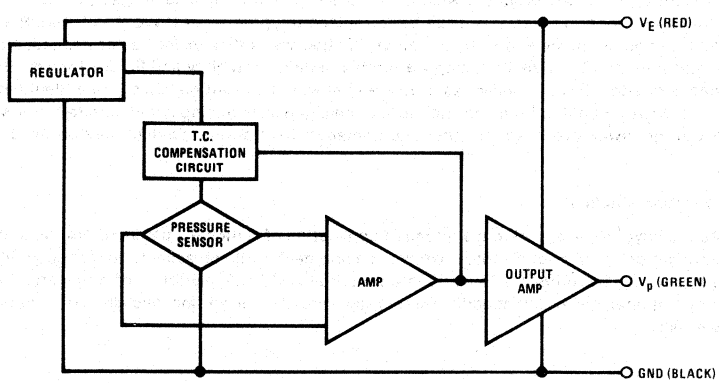
Features

- 0-100 psia to 0-5000 psia
- Rugged concentric housing
- Flying leads
- Submersible fluid-filled version
- High accuracy and stability
- Temperature compensation
- High level output voltage — 2.5V to 12.5V
- Field interchangeability
- Available from National distributors

Applications

- Engine diagnostics
- Machine tools
- Hydraulics
- Off-road vehicles
- Pneumatics
- Pressurized tanks and lines
- Deep well pumps
- Oceanography
- Welding machines

Block Diagram



LX14XXA Characteristics

Maximum Ratings

Excitation Voltage (Note 6)	30V
Output Current	
Source	20 mA
Sink	10 mA
Transducer Bias Current	20 mA
Operating Temperature Range	0 °C to 85 °C
Storage Temperature Range	−40 °C to +105 °C
Lead Soldering Temperature (10 seconds)	260 °C

Typical Characteristics

Output Voltage Sensitivity to Excitation Voltage	0.5%
Output Impedance	<50Ω
Electrical Noise Equivalent ($0 \leq f \leq 1$ kHz)	0.04% Span
Natural Frequency of Sensor Diaphragm	>100 kHz
Transducer Bias Current	7-10 mA

Reference Conditions

Excitation Voltage, V_E (Note 6)	15V
Reference Temperature	25 °C
Reference Temperature Range	0 °C to 85 °C
Offset Reference Pressure	0 psia

Guaranteed Specifications

DEVICE TYPE (NOTE 1)	OPERATING PRESSURE RANGE	MAXIMUM OVER PRESSURE	OFFSET SPECIFICATIONS (NOTE 4)				SPAN SPECIFICATIONS (NOTE 5)			
			OFFSET CALIBRATION	TEMP. COEFFICIENT	REPEATABILITY	STABILITY	SENSITIVITY CALIBRATION	TEMP. COEFFICIENT	L-H-R (NOTE 2)	STABILITY
			V	±%FS/°C	±%FS	±%FS	mV/psi	±%S/°C	±%S	±%S
LX1420A	0 to 100 psia	150 psia	2.5 ± 0.25	0.04	0.4	1.2	100 ± 2	0.05	0.67	0.3
LX1430A	0 to 300 psia	450 psia	2.5 ± 0.25	0.03	0.4	1.0	33.3 ± 0.67	0.05	0.67	0.3
LX1440A	0 to 1000 psia	1500 psia	2.5 ± 0.25	0.03	0.4	1.0	10 ± 0.2	0.05	1.00	0.4
LX1450A	0 to 2000 psia	3000 psia	2.5 ± 0.25	0.03	0.4	1.0	5 ± 0.1	0.05	1.50	0.4
LX1460A	0 to 3000 psia	4500 psia	2.5 ± 0.25	0.03	0.4	1.0	3.33 ± 0.067	0.05	2.00	0.4
LX1470A	0 to 5000 psia	5000 psia	2.5 ± 0.25	0.03	0.4	1.0	2 ± 0.04	0.05	3.00	0.4

Note 1: Offset Repeatability — the transducer's ability to reproduce offset voltage at constant temperature (25 °C) when exposed to a maximum of 50 full pressure range cycles.

Note 2: Stability — the transducer's ability to reproduce the output voltage corresponding to a specific pressure and temperature in a period of one year during which permitted operating and storage conditions are not exceeded.

Note 3: Linearity — the maximum deviation of measured output over the full pressure range at constant temperature (25 °C) from the best straight line intersecting the output at the offset reference pressure.

Hysteresis and Span Repeatability — the transducer's ability to reproduce any output voltage over the full pressure range at constant temperature (25 °C) when exposed to a maximum of 50 full pressure range cycles.

Note 4: Offset errors are independent of applied pressure and specified at %FS, percent of full span operating pressure range. See Application Guide.

Note 5: Span errors are proportional to applied pressure and specified as %S, percent of span operating pressure. See Application Guide.

Note 6: The LX14XXA series is not polarity protected. Incorrect application of excitation voltage or ground to the wrong lead can cause electrical failure.

Do Not Use in Life Support Applications.

Application Guide

The LX14XX Series devices are enclosed in rugged concentric housings that protect the basic integrated circuit pressure transducer from physical abuse and corrosive environments. However, many applications require special consideration of device characteristics. The following application hints are supplementary to Sections 4 and 5 of the 1977 Pressure Transducer Handbook which should be consulted before using any NSC pressure transducer product.

1. Accuracy Specifications — Autoreferencing

Error parameters are specified separately for offset and span. These errors are independent which allows easy computation of error bands, recalibration, and use of autoreferencing, a technique of automatic recalibration. The following describes the basic use of these error parameters. For a detailed discussion, see Application Note AN246.

Span Accuracy

Span errors are proportional to applied pressure and specified as %S, percent of span. The span error in psi is given by:

$$\text{Span Error} = \frac{(\%S)}{100} \times |P_A - P_{REF}|$$

where $|P_A - P_{REF}|$ is the absolute value of applied pressure P_A as measured from the offset reference P_{REF}. Note that at the reference pressure, 0 psia for all LX14XX devices, span errors are zero, and the only errors are in offset.

Offset Accuracy

Offset errors are constant with pressure and given as %FS, where FS is full span voltage or operating pressure range. For example, the presure range of the LX1430A is 300 psia full span, and the specified offset stability is 1%FS. The error in psi is therefore:

$$\text{Offset Stability Error} = \frac{1.0\%}{100} \times 300\,\text{psi} = 3\,\text{psi}$$

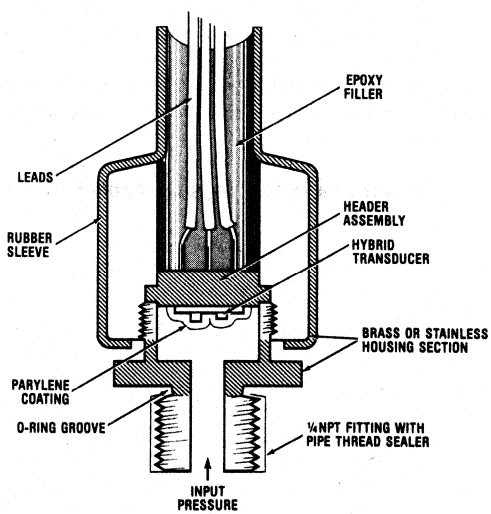
Since offset errors are independent of applied pressure they can be fully or partially "calibrated out" by manual referencing or autoreferencing at any known pressure, normally the specified offset reference pressure. For a full discussion of autoreferencing, see Section 7 of the 1977 Pressure Transducer Handbook.

2. Use of Absolute as Gage — Altitude Effect

The LX14XXA devices are *absolute* pressure transducers with a vacuum enclosed in the silicon chip for reference. The measured pressure is therefore equal to gage pressure plus the local barometric pressure. This appears as an offset in output signal and can vary from 15 psia near sea level to about 10 psia at 10,000 ft. altitude. The local variations in barometric pressure ($\leq$ 0.5 psi) are normally insignificant, even for the 100 psia device (the LX1420A); but a change from sea level to 10,000 ft. would reduce the apparent gage pressure by 5 psi. If not "zeroed out", this variation could appear as a significant gage error for the LX1420A or LX1430A (300 psia) transducers. To measure gage pressure in these ranges, other National transducers, such as the LX1820GZ, or the LX1830GZ, should probably be used (see Selection Guide). However, in going to transducers with higher pressure ranges, the barometric offset and variations become less significant, which allows these devices, LX1440A through LX1470A, to easily be used as "pseudo" gage transducers.

3. "Dead-Ending" Feature

If the pressure applied to the transducer greatly exceeds proof pressure (maximum specified operating pressure), the silicon diaphragm could rupture. But, unlike gage transducers, the LX14XXA devices are "dead-ended" so that diaphragm rupture does not influence fluid leakage. However, excessive overpressure can cause deformation of the inner seal which would allow a slow leak of working fluid through the body of the transducer (see Transducer Structure Diagram).



LX14XXA Series Transducer Structure

4. Leak Rate — Static Systems

The PX4 series packages are not hermetic. National's pressure transducers are guaranteed to have an effective leak area less than 10^{-7} cm^2 as defined in App. Note AN232. Each Transducer is leak tested at room temperature with 100 psig compressed air.

However, the user should be aware that the leak rate can depend on the type, viscosity, pressure, and the temperature of the fluid and can increase with fatigue resulting from pressure cycling. This is especially important in static systems where a fluid under pressure is to be maintained for an extended period in an enclosure without replenishment. In such cases it may be necessary to enclose the transducer in the pressure vessel and bring the leads out via a hermetic feedthrough connector installed in the enclosure wall.

5. Fatigue Life — Cyclic Systems

In systems requiring a large number of pressure cycles, such as machine tools, brake systems, and other cyclic pneumatic and hydraulic equipment, the fatigue life of the transducer becomes important. Although the basic sensor can withstand more than one million full operating pressure cycles, the seal between the header assembly and the transducer body degrades such that significant leakage typically occurs within the first several hundred thousand pressure cycles. For enhanced life, the transducer can be completely enclosed in the pressure system as described above for static pressure systems.

6. Pressure Spikes — Importance of Snubbing

In many cyclic pressure systems, large pressure spikes can occur as a result of pumping action, valve closure, or mechanical resonance. Such spikes can damage the transducer as well as other components in the pressure system. In addition to limiting valve closure rate and avoiding undesirable mechanical resonance, it is good design practice to protect critical components, including the transducer, with adequate snubbing or other damping methods. This can greatly improve reliability by reducing fatigue and avoiding catastrophic failure of the transducer.

7. Fast Response — Measuring Transients

The snubbing problem is also complicated by the fact that older mechanical-type transducers and manometers do not have fast enough response to measure the magnitude of pressure spikes; hence the spikes could go undetected. However, the LX14XXA Series can accurately measure and characterize sub-millisecond pressure transients. Although the silicon diaphragm can respond much faster, since its resonant frequency is greater than 100 kHz, the overall response time is limited to about 10 kHz by the amplifier circuit. But plumbing limits the response time in most systems. This fast response capability of the LX14XXA series transducers can be used in measuring and evaluating pressure transients as well as for closed-loop operation in fast pneumatic and hydraulic systems. Response time is degraded by damping in the fluid-filled LX14XXAF series.

8. Compatible Fluids — Humidity

The basic LX14XXA pressure transducer is compatible with many non-aqueous fuels, oils, refrigerants, hydraulic fluids and non-corrosive gases. The basic integrated circuit pressure transducer element is coated with a thin compliant layer of parylene. But moisture condensate or other ionic, acidic, or corrosive fluids cause erroneous readings followed by electrical failure. For ionic and corrosive working fluids such as sea water and others not compatible with parylene (see 1977 Handbook, Section 4) the fluid isolator ("F" version) is recommended. This device employs a Viton diaphragm which is compatible with most aqueous and acidic solutions and hydrocarbons, but cannot tolerate ketones, alkaline solutions, or brake fluid. The Viton diaphragm is also limited to temperatures of 85 °C or below, even in storage, since it deteriorates rapidly above that temperature.

9. Submersibility

Although the LX14XXA housing is not fully "hermetic", it is externally submersible as long as ambient pressure doesn't significantly exceed working fluid pressure. For example, it can be used in equipment that must be steam cleaned, or mounted out-of-doors in rain or snow, as long as the working fluid port is properly sealed.

The LX14XXAF series fluid-filled version is fully submersible. For example, it could be immersed directly in water to measure depth.

Pressure Transducer Selection Guide

Ordering Information

LX 1 4 20 A FS

Standard Option
- B = Backward Gage Version (PX6B, PX8B)
- N = Nylon Housing (PX8N, PX8BN)
- S = Stainless Steel Package (PX4S)
- Z = Zinc Housing (PX8Z, PX8BZ, PX8DZ)
- BN = Combine B and N Options
- BZ = Combine B and Z Options
- F = Fluid Filled Version (PX4F)
- FS = Combine F and S Options (PX4FS)

Pressure Type
- A = Absolute
- D = Differential
- G = Gage

Pressure Range (Characteristics Table)

Package Type
- 4 = Rugged Cylindrical Plumbed Fitting (PX4 Series)
- 5 = TO-5 Package with Port (PX5 Series)
- 6 = Ceramic Package for PCB Mounting (PX6 Series)
- 8 = Rugged Zinc or Nylon Housing (PX8 Series)

Technology
- 0 = Monolithic
- 1 = Hybrid

Device Type
- LX = Linear Transducer

Pressure Transducer Features Chart

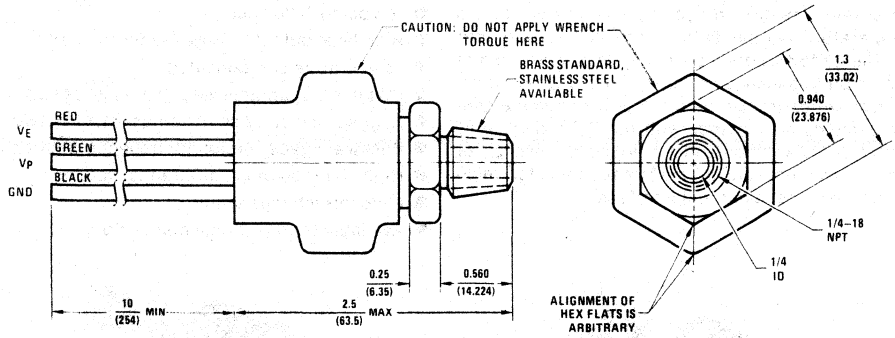
Feature / Product	Monolithic	Hybrid	TO-5 Package	Ceramic Package	Nylon Housing	Zinc Housing	Backward Gage Isolator	High Common-Mode Differential Housing	Brass Housing	Stainless Steel Housing	Fluid Filled Isolator
LX14XX Absolute		LX14XXA(S) LX14XXAF(S)							LX14XXA	LX14XXAS	LX14XXAF LX14XXAFS
LX16XX Absolute		LX16XXA		LX16XXA							
LX16XX Gage		LX16XXG LX16XXGB		LX16XXG LX16XXGB			LX16XXGB				
LX16XX Differential		LX16XXD		LX16XXD							
LX18XX Absolute		LX18XXAZ LX18XXAN			LX18XXAN	LX18XXAZ					
LX18XX Gage		LX18XXG(N) LX18XXGB(N)			LX18XXGN LX18XXGBN	LX18XXGZ LX18XXGBZ	LX18XXGBZ LX18XXGBN				
LX18XX Differential		LX18XXDZ				LX18XXDZ		LX18XXDZ			
LX05XX Absolute	LX0503A LX0520A		LX0503A LX0520A								
LX06XX Gage	LX0603GB LX0620GB			LX0603GB LX0620GB			LX0603GB LX0620GB				
LX06XX Differential	LX0603D LX0620D			LX0603D LX0620D							

Housings

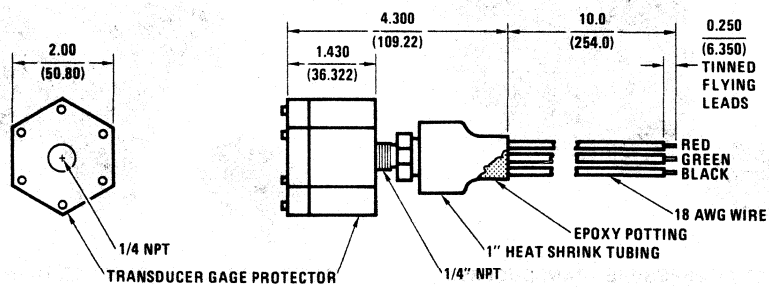
LX14XXA Housing Key

Device	Description	Housing Type
LX14XXA	Brass Housing	PX4
LX14XXAF	LX14XXA with Fluid Isolator	PX4F
LX14XXAS	Stainless Steel Housing	PX4S
LX14XXAFS	LX14XXAS with Fluid Isolator	PX4FS

Physical Dimensions inches (millimeters)



PX4 and PX4S Housings
Weight: 105 grams



PX4F and PX4FS Housings
Weight: 700 grams

Warranty

National Semiconductor Corporation warrants that its products shall be free from defects in workmanship and materials, and shall conform to National's published specifications, or other specifications accepted by National in writing for a period of one (1) year from the date of National's shipment.

Limitation of Warranty Liability:

This warranty does not apply to any products which have been subject to misuse, neglect, accident, or modification. National's sole obligation under its warranty shall be to replace the product or issue credit. National's warranty and remedies are exclusive and are made expressly in lieu of all other warranties expressed or implied, either in fact or by operation of law, statutory or otherwise, including warranties of merchantability and fitness for use. National shall not be liable for damages due to delays in deliveries or use and shall in no event be liable for incidental or consequential damages of any kind, whether arising from contract, tort, or negligence, including but not limited to, loss of profits, loss of customers, loss of goodwill, overhead, or other like damages. No National product may be used in a life support application.

Limitation of Application Liability:

National assumes the buyer to be expert in his intended application of National's products. National claims no special expertise in the application of its products into the buyer's equipment. National accepts no responsibility for the buyer's selection and use of National's products. Buyer's interpretation and implementation of application suggestions and recommendation by National, general or specific, transmitted verbally or in writing, published or unpublished, is strictly at the buyer's own risk.

National Semiconductor

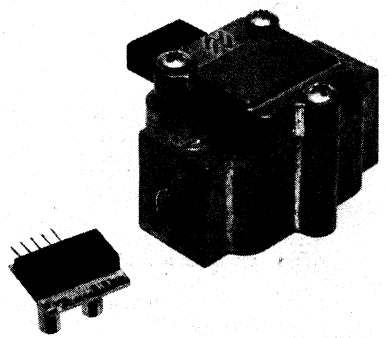
LX16XX, LX18XX Series Pressure Transducers: Absolute, Differential, Gage and Backward Gage Devices

General Description

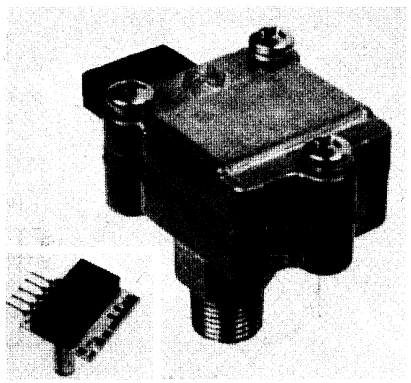
These are fully conditioned hybrid pressure transducers with temperature compensation and high level output voltage. The LX16XX series transducers are provided in compact ceramic packages for easy PC board mounting. The LX18XX series transducers are provided in die cast zinc or molded nylon housings with 1/8 NPT fittings; they replace the LX17XX series and are equivalent except for housing improvements and a 3-pin Molex connector which allows easy, low-cost electrical interface.

Features

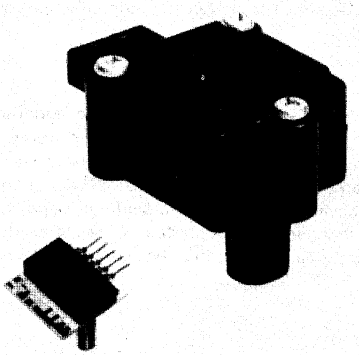
- ±5 psi to 0-300 psi
- High level output voltage—2.5V to 12.5V
- Temperature compensated
- PC board mountable versions—LX16XX series
- Rugged zinc or nylon housings—LX18XX series
- Backward gage version for aqueous working fluids
- High common-mode differential version
- Field interchangeability
- Available from National distributors



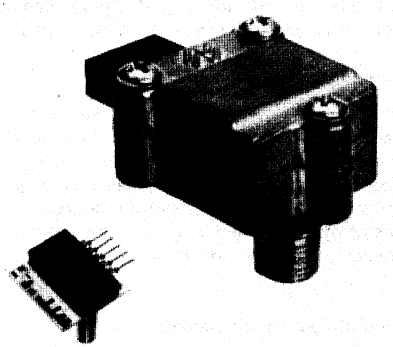
DIFFERENTIAL PRESSURE TRANSDUCERS: Negative Port Protected from Aqueous Working Fluids. Ceramic or High Common-Mode Zinc Housing.



BACKWARD GAGE PRESSURE TRANSDUCERS: Gage Port Protected from Aqueous Working Fluids. Ceramic, Zinc or Nylon Housings.



GAGE PRESSURE TRANSDUCERS: Reference Port Protected from Corrosive Environment. Ceramic, Zinc or Nylon Housings.



ABSOLUTE PRESSURE TRANSDUCER: Enclosed Vacuum Reference Ceramic, Zinc or Nylon Housings.

Pressure Transducer Characteristics

MAXIMUM RATINGS

Excitation Voltage (Note 7)	30V
Output Current	
Source	20 mA
Sink	10 mA
Transducer Bias Current	20 mA
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	−40°C to +105°C
Lead Soldering Temperature (10 seconds)	260°C
Common Mode Line Pressure, LX16XXD LX18XXDZ	400 psig

TYPICAL CHARACTERISTICS

Output Voltage Sensitivity to Excitation Voltage	0.5%
Output Impedance	<50Ω
Electrical Noise Equivalent (0 ≤ f ≤ 1 kHz)	0.04% Span
Natural Frequency of Sensor Diaphragm	50 kHz
Transducer Bias Current	11 mA–15 mA

REFERENCE CONDITIONS

Excitation Voltage, V_E (Note 7)	15V
Reference Temperature	25°C
Reference Temperature Range	0°C to 85°C
Reference Offset Pressure	0 psi (Note 4)
Common Mode Line Pressure, LX16XXD LX18XXDZ	0 psig

Pressure Transducer Characteristics

Device Family	Operating Pressure Range	Guaranteed Specifications							
		Offset Characteristics (Note 5)				Span Characteristics (Note 6)			
		Offset Calibration V (Note 4)	Temp. Coefficient ± %FS/°C	Repeatability (Note 1) ± %FS	Stability (Note 2) ± %FS	Sensitivity Calibration mV/psi	Temp. Coefficient ± %S/°C	Linearity Hysterisis Repeatability (Note 3) ± %S	Stability (Note 2) ± %S
LX1601 LX1801	±5 psi (Note 4)	7.5 ±0.70	0.06	0.5	5.0	1000 ±20	0.05	1.33	1.0
LX1602 LX1802	15 psi	2.5 ±0.50	0.05	0.4	3.3	670 ±13	0.05	0.67	0.7
LX1603 LX1803	30 psi	2.5 ±0.35	0.05	0.4	1.7	333 ±6	0.05	0.67	0.3
LX1604 LX1804	±15 psi	7.5 ±0.35	0.05	0.4	1.7	333 ±6.7	0.05	1.33	0.3
LX1610 LX1810	60 psi	2.5 ±0.30	0.04	0.4	1.5	167 ±3.3	0.05	0.67	0.3
LX1620 LX1820	100 psi	2.5 ±0.30	0.04	0.4	1.2	100 ±2	0.05	0.67	0.3
LX1830	300 psi	2.5 ±0.30	0.03	0.4	1.0	33.3 ±0.67	0.05	0.67	0.3

Specification Notes:

Note 1: Offset Repeatability—the transducer's ability to reproduce offset voltage at constant temperature (25°C) when exposed to a maximum of 50 full pressure range cycles.

Note 2: Stability—the transducer's ability to reproduce the output voltage corresponding to a specific pressure and temperature in a period of one year during which permitted operating and storage conditions are not exceeded.

Note 3: Linearity—the maximum deviation of measured output over the full pressure range at constant temperature (25°C) from the best straight line through the output at offset reference pressure.

Hysteresis, and Span Repeatability—the transducer's ability to reproduce any output voltage over the full pressure range at constant temperature (25°C) when exposed to a maximum of 50 full pressure range cycles.

Note 4: Offset Reference Pressure—15 psia for LX1601A and LX1801A family; 0 psi for all other LX16XX and LX18XX devices.

Note 5: Offset errors are independent of applied pressure and specified as %FS, percent of full span operating pressure range. See Application Guide.

Note 6: Span errors are proportional to applied pressure and specified as %S, percent of span operating pressure. See Application Guide.

Note 7: The LX16XX and LX18XX series are not polarity protected. Incorrect application of excitation voltage or ground to the wrong pin can cause electrical failure.

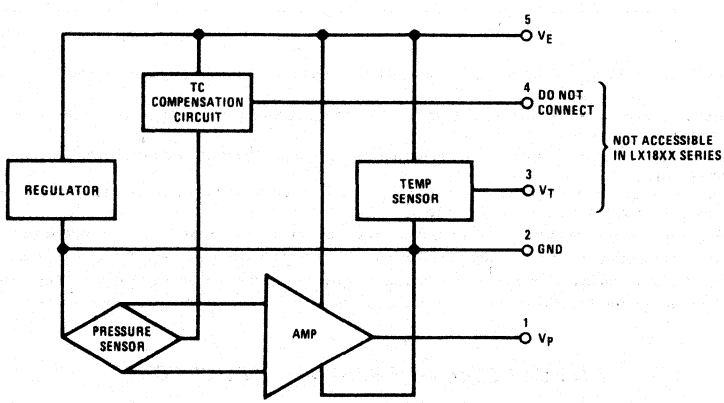
DO NOT USE IN LIFE SUPPORT APPLICATIONS

Device Pressure Ratings

Device Type	Operating Pressure Range	Maximum Over Pressure
ABSOLUTE PRESSURE DEVICES		
LX1601A LX1801A (N, Z)	10 to 20 psia	100 psia
LX1602A LX1802A (N, Z)	0 to 15 psia	100 psia
LX1603A LX1803A (N, Z)	0 to 30 psia	100 psia
LX1610A LX1810A (N, Z)	0 to 60 psia	125 psia
LX1620A LX1820A (N, Z)	0 to 100 psia	200 psia
LX1830A (N, Z)	0 to 300 psia	450 psia
DIFFERENTIAL PRESSURE DEVICES		
LX1601D LX1801DZ	−5 to +5 psid	$^{+100}_{-45}$ psid
LX1602D LX1802DZ	0 to 15 psid	$^{+100}_{-45}$ psid
LX1603D LX1803DZ	0 to 30 psid	$^{+100}_{-45}$ psid
LX1604D LX1804DZ	−15 to +15 psid	$^{+100}_{-45}$ psid
LX1610D LX1810DZ	0 to 60 psid	$^{+125}_{-90}$ psid
LX1620D LX1820DZ	0 to 100 psid	$^{+200}_{-150}$ psid
LX1830DZ	0 to 300 psid	$^{+450}_{-400}$ psid

Device Type	Operating Pressure Range	Maximum Over Pressure
GAGE PRESSURE DEVICES		
LX1601G LX1801G (N, Z)	−5 to +5 psig	100 psig
LX1602G LX1802G (N, Z)	0 to 15 psig	100 psig
LX1603G LX1803G (N, Z)	0 to 30 psig	100 psig
LX1604G LX1804G (N, Z)	−15 to +15 psig	100 psig
LX1610G LX1810G (N, Z)	0 to 60 psig	125 psig
LX1620G LX1820G (N, Z)	0 to 100 psig	200 psig
LX1830G (N, Z)	0 to 300 psig	450 psig
BACKWARD GAGE DEVICES		
LX1601GB LX1801GB (N, Z)	−5 to +5 psig	45 psig
LX1602GB LX1802GB (N, Z)	0 to 15 psig	45 psig
LX1603GB LX1803GB (N, Z)	0 to 30 psig	45 psig
LX1604GB LX1804GB (N, Z)	−15 to +15 psig	45 psig
LX1610GB LX1810GB (N, Z)	0 to 60 psig	100 psig
LX1620GB LX1820GB (N, Z)	0 to 100 psig	150 psig
LX1830GB (N, Z)	0 to 300 psig	400 psig

Schematic Diagram



Application Guide

ACCURACY SPECIFICATIONS — AUTOREFERENCING

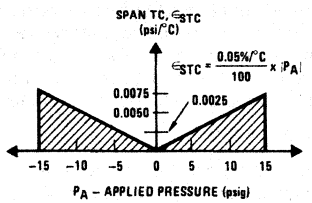
Error parameters are specified separately for offset and span. These errors are independent which allows easy computation of error bands, recalibration, and use of autoreferencing, a technique of automatic recalibration. The following describes the basic use of these error parameters. For a detailed discussion, see Application Note AN-246.

Span Accuracy

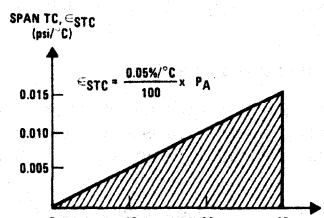
Span errors are proportional to applied pressure and specified as %S, percent of span. The span error in psi is given by:

$$\text{Span Error} = \frac{(\%S)}{100} \times |P_A - P_{REF}|$$

where $|P_A - P_{REF}|$ is the absolute value of applied pressure P_A as measured from the offset reference P_{REF}. This produces error bands as shown in *Figure 1*. Note that at the reference pressure span errors are zero and the only errors are in offset.



a. LX1604G Transducer



b. LX1603G Transducer

FIGURE 1. Span Temperature Coefficients: Error Bands for LX1604G (± 15 psig) and LX1603G (0 to 30 psig) Devices

Offset Accuracy

Offset errors are constant with pressure and given as %FS, where FS is full span voltage or operating pressure range. For example, the pressure range of the LX1604G is ± 15 psig, or 30 psig full span, and the specified offset stability is ± 1.7%FS. The error in psi is therefore:

$$\text{Offset Stability} = \frac{\pm 1.7\%}{100} \times 30\,\text{psi} = \pm 0.5\,\text{psi}$$

Since offset errors are independent of applied pressure they can be fully or partially "calibrated out" by manual referencing or autoreferencing at any known pressure, normally the specified offset reference pressure. For a full discussion of autoreferencing, see Section 7 of the 1977 Pressure Transducer Handbook.

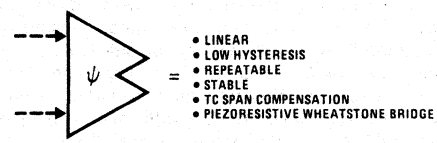
Consulting the Handbook

The 1977 Pressure Transducer Handbook should be consulted before using any National pressure transducer product. The handbook was written for hybrid transducers and includes comprehensive information on pressure transducer installation, definitions, accuracy computation, auto-referencing, and many applications. The following supplements the handbook for the LX16XX and LX18XX series transducers.

Signal Conditioning — Hybrid vs Monolithic

The LX16XX and LX18XX series transducers are fully signal-conditioned hybrid pressure transducers with temperature compensation, single-ended 10V output span, and internal voltage regulation to allow operation with a 15V to 30V supply. They offer easy electrical interface and high accuracy over a wide temperature range *(Figure 2)*. If the user has the capability of developing temperature compensation circuits (or if TC is not required), the LX05XX or LX06XX series monolithic sensors may offer a viable low-cost alternative (see "LX05XXA, LX06XXD, LX06XXGB Series Monolithic Pressure Transducers" data sheet).

Monolithic Device



Hybrid Device

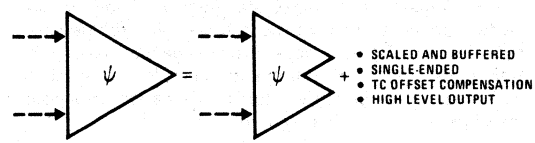


FIGURE 2. Pressure Transducer Symbols

LX16XX vs LX18XX

As shown in *Figure 3*, the LX16XX series hybrid transducers are provided in a ceramic SIP (single-in-line package) for easy PC board mounting, with pressure ports suitable for attachment of flexible tubing. The sensor chip is attached with a stress-relieving mount to minimize stress transfer; but to achieve high accuracy the user must avoid stressing the ceramic package in installation (see 1977 Handbook, Section 4). The advantages of using the LX16XX series are low-cost and high density packaging. They are available with operating pressure ranges up to 100 psi.

Application Guide (Continued)

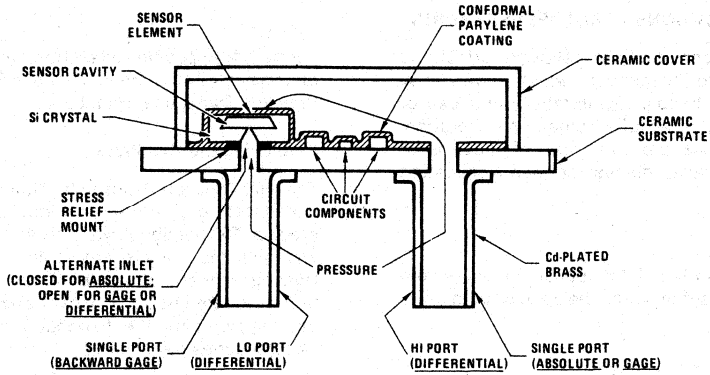


FIGURE 3. Basic LX16XX Series Hybrid IC Pressure Transducer Structure

The LX18XX series devices are LX16XX devices enclosed in rugged zinc or nylon housings, with internal O-ring seals, and 1/8 NPT fittings. They mate with standard connectors. They offer protection against rough handling and stress from the pressure system. The stress protection feature is enhanced in the LX18XXDZ high common-mode differential versions which can measure small pressure differentials on a line pressurized up to 400 psig. The LX18XX series is available with operating pressure ranges up to 300 psi.

MEDIA COMPATIBILITY — HUMIDITY

As shown in *Figure 3,* the basic hybrid transducer structure allows for two pressure inlets which differ in susceptibility to moisture and other fluids, according to whether the fluid is applied to the top side (circuit side) or to the back side (cavity side) of the diaphragm. The top side is coated with a thin compliant layer of parylene. The parylened circuit is compatible with many non-aqueous fluids, and the back side of the diaphragm is compatible with aqueous fluids. This is summarized below for each pressure transducer type.

The circuit-side inlet (absolute, gage or hi-differential ports) can be used with most fuels, oils, refrigerants, hydraulic fluids, and non-corrosive gasses (see 1977 Handbook, Section 4). But moisture condensate or other ionic, acidic or corrosive fluids can cause erroneous readings and electrical failure.

The cavity-side inlet (backward gage or lo-differential ports) can be used with aqueous fluids but cannot be used with acids and other fluids corrosive to device construction material.

Hence, the *backward gage* version can be used with many aqueous working fluids but requires a dry ambient. The *differential* version can tolerate aqueous fluids in the lo-port but not in the hi-port. The *absolute* and *gage* versions both require dry working fluids, but the ambient can be humid.

LEAK RATE

The PX6 (LX16XX) and PX8 (LX18XX) packages are not hermetic. National's pressure transducers are guaranteed to have an effective leak area less than 10^{-7} cm^2 as defined in Application Note AN-232. Each transducer is leak tested at room temperature with 45 psig compressed air. However, the user should be aware that the leak rate can depend on the type, viscosity, pressure, and temperature of the fluid and can increase with fatigue resulting from pressure cycling. This is especially important in static systems where a fluid under pressure is to be maintained for an extended period in an enclosure without replenishment. In such cases it may be necessary to enclose an absolute pressure transducer [LX16XXA or LX18XXA (N, Z)] in the pressure vessel and bring the leads out via an hermetic feedthrough connector installed in the enclosure wall.

"Dead-Ending" Feature

If the pressure applied to the LX16XXA or LX18XXA (N, Z) exceeds proof pressure (maximum specified operating pressure), the silicon diaphragm could rupture. But, unlike gage transducers, the absolute devices are "dead-ended" so that diaphragm rupture does not necessarily result in fluid leakage.

INPUT/OUTPUT POLARITY

The output signal is at pin 1 for all LX16XX series hybrid transducers. *Figure 4* shows the pinout for these transducers, with pressure ports extending out of the drawing.

The output signal of absolute and gage transducers is positive-going for increasing pressure applied to the absolute or gage port.

The output signal of backward gage transducers is positive-going for increasing pressure applied to the backward gage port.

The output signal of differential transducers is positive going for increasing pressure applied to the hi-port relative to the lo-port.

The LX16XX and LX18XX series are not polarity protected. Incorrect application of excitation voltage or ground to the wrong pin can cause electrical failure.

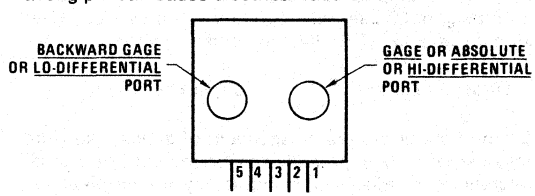


FIGURE 4. LX16XX Pinout, Portside View

Pressure Transducer Selection Guide

ORDERING INFORMATION

LX 1 8 20 G BZ

Standard Option

B = Backward Gage Version (PX6B, PX8B)
N = Nylon Housing (PX8N, PX8BN)
S = Stainless Steel Package (PX4S)
Z = Zinc Housing (PX8Z, PX8BZ, PX8DZ)
BN = Combine B and N Options
BZ = Combine B and Z Options
F = Fluid Filled Version (PX4F)
FS = Combine F and S Options (PX4FS)

Pressure Type

A = Absolute
D = Differential
G = Gage

Pressure Range (Characterstics Table)

Package Type

4 = Rugged Cylindrical Plumbed Fitting (PX4 Series)
5 = TO-5 Package with Port (PX5 Series)
6 = Ceramic Package for PCB Mounting (PX6 Series)
8 = Rugged Zinc or Nylon Housing (PX8 Series)

Technology

0 = Monolithic
1 = Hybrid

Device Type

LX = Linear Transducer

PRESSURE TRANSDUCER FEATURES CHART

Feature / Product	Monolithic	Hybrid	TO-5 Package	Ceramic Package	Nylon Housing	Zinc Housing	Backward Gage Isolator	High Common-Mode Differential Housing	Brass Housing	Stainless Steel Housing	Fluid Filled Isolator
LX14XX Absolute		LX14XXA(S) LX14XXAF(S)							LX14XXA	LX14XXAS	LX14XXAF LX14XXAFS
LX16XX Absolute		LX16XXA		LX16XXA							
LX16XX Gage		LX16XXG LX16XXGB		LX16XXG LX16XXGB			LX16XXGB				
LX16XX Differential		LX16XXD		LX16XXD							
LX18XX Absolute		LX18XXAZ LX18XXAN			LX18XXAN	LX18XXAZ					
LX18XX Gage		LX18XXG(N) LX18XXGB(N)			LX18XXGN LX18XXGBN	LX18XXGZ LX18XXGBZ	LX18XXGBZ LX18XXGBN				
LX18XX Differential		LX18XXDZ				LX18XXDZ		LX18XXDZ			
LX05XX Absolute	LX0503A LX0520A		LX0503A LX0520A								
LX06XX Gage	LX0603GB LX0620GB			LX0603GB LX0620GB			LX0603GB LX0620GB				
LX06XX Differential	LX0603D LX0620D			LX0603D LX0620D							

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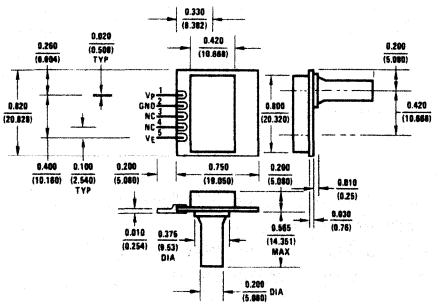
Package and Housing Dimensions inches (millimeters)

Package Key

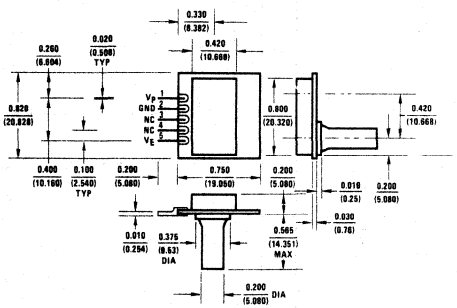
Device	Package
LX16XXA LX16XXG	PX6
LX18XXA (N, Z) LX18XXG (N, Z)	PX8 (N, Z)
LX16XXD	PX6D
LX18XXDZ	PX8DZ
LX16XXGB	PX6B
LX18XXGB (N, Z)	PX8B (N, Z)

LX18XX (PX8) Mating Connector

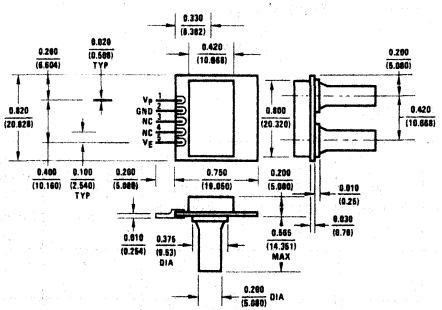
Vendor	Connector No.	Male Pin No.
Litton-Winchester Win-Com Series	59-03P1000	159-1018P
Waldon/Molex	03-09-2031	02-09-2103
Molex—without mounting ears	03-09-2032	



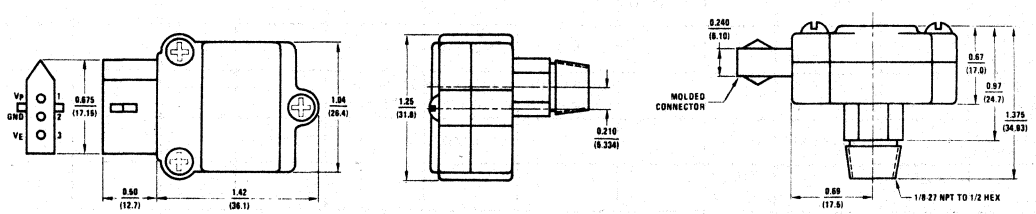
PX6
0.2″ Port, Hybrid Pressure Transducer Package
Weight: 5 Grams



PX6B
0.2″ Port, Hybrid Pressure Transducer Package
Weight: 5 Grams

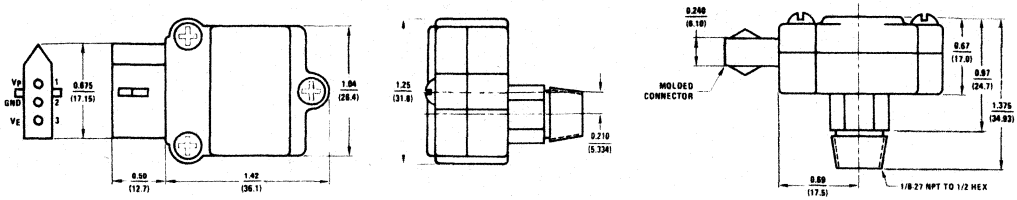


PX6D
0.2″ Port, Hybrid Pressure Transducer Package
Weight: 5 Grams

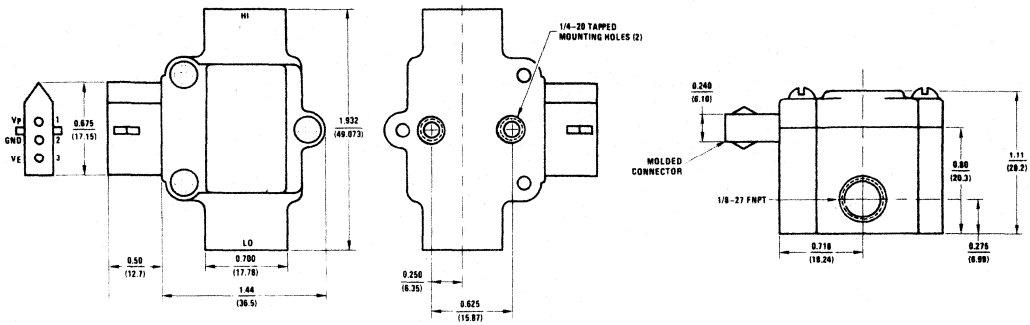


PX8 (N, Z)
1/8″ NPT Nylon (N) or Zinc (Z) Pressure Transducer Package
Weight: 100 Grams (Zinc), 50 Grams (Nylon)

Package and Housing Dimensions (Continued) inches (millimeters)



PX8B (N, Z)
1/8" NPT Nylon (N) or Zinc (Z) Pressure Transducer Package
Weight: 100 Grams (Zinc), 50 Grams (Nylon)



PX8DZ
1/8" FNPT Zinc Pressure Transducer Package
Weight: 170 Grams

WARRANTY

National warrants that its products shall be free from defects in workmanship and materials, and shall conform to National's published specifications, or other specifications accepted by National in writing for a period of one (1) year from the date of National's shipment.

LIMITATION OF WARRANTY LIABILITY

The warranty does not apply to any products which have been subject to misuse, neglect, accident, or modification. National's sole obligation under its warranty shall be to replace the product or issue credit. National's warranty and remedies are exclusive and are made expressly in lieu of all other warranties express or implied, either in fact or by operation of law, statutory or otherwise, including warranties of merchantability and fitness for use. National shall not be liable for damages due to delays in deliveries or use and shall in no event be liable for incidental or consequential damages of any kind, whether arising from contract, tort or negligence, including but not limited to, loss of profits, loss of customers, loss of goodwill, overhead or other like damages. No National product may be used in a life support application.

LIMITATION OF APPLICATION LIABILITY

National assumes the buyer to be expert in his intended application of National's products. National claims no special expertise in the application of its products into the buyer's equipment. National accepts no responsibility for the buyer's selection and use of National's products. Buyer's interpretation and implementation of application suggestions and recommendation by National, general or specific, transmitted verbally or in writing, published or unpublished, is strictly at the buyer's own risk.

Section 13

Successive Approximation Registers/Comparators

13

Successive Approximation Registers/Comparators

Section Contents

National Semiconductor

Successive Approximation Registers/Comparators

DM2502, DM2503, DM2504 Successive Approximation Registers

General Description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary in combination with a D/A converter to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable.

The DM2503 has 8 bits and is expandable without serial capability.

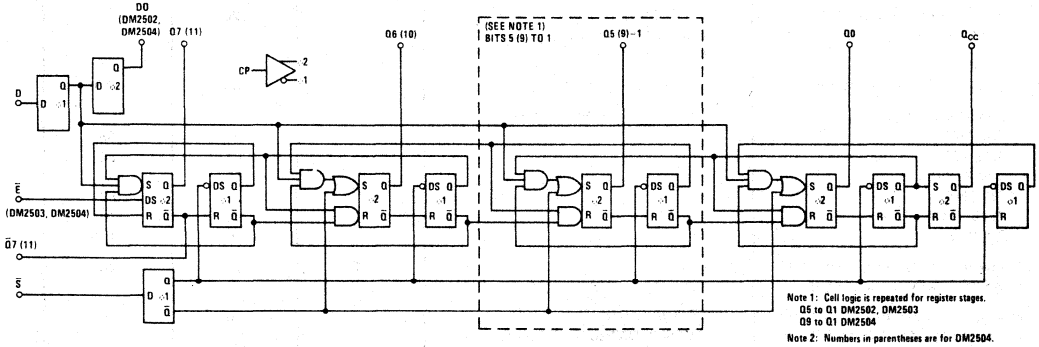
The DM2504 has 12 bits with serial capability and expandability.

All three devices are available in ceramic DIP, ceramic flatpak, and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

Features

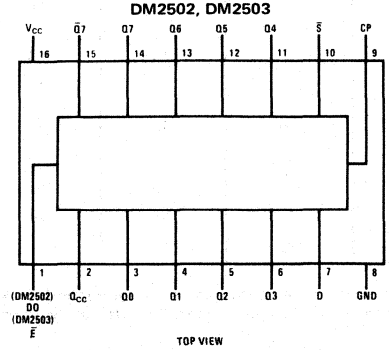
- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

Logic Diagram



Connection Diagrams (Dual-In-Line and Flat Packages)

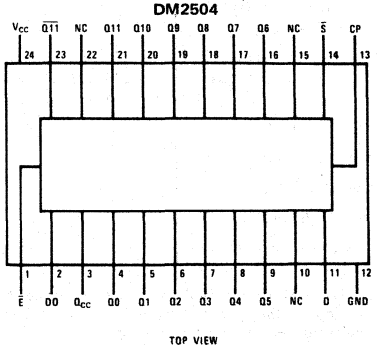
DM2502, DM2503



TOP VIEW

Order Number DM2502J, DM2502CJ, DM2503J or DM2503CJ
See NS Package J16A
Order Number DM2502CN or DM2503CN
See NS Package N16A
Order Number DM2502W, DM2502CW, DM2503W, or DM2503CW
See NS Package W16A

DM2504



TOP VIEW

Order Number DM2504F or DM2504CF
See NS Package F24A

Order Number DM2504J or DM2504CJ
See NS Package J24A

Order Number DM2504CN
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM2502C, DM2503C, DM2504C	4.75	5.25	V
DM2502, DM2503, DM2504	4.5	5.5	V
Temperature, T_A			
DM2502C, DM2503C, DM2504C	0	+70	°C
DM2502, DM2503, DM2504	−55	+125	°C

Electrical Characteristics (Notes 2 and 3) V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})	V_{CC} = Min	2.0			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max				
CP Input	V_{IH} = 2.4V		6	40	μA
D, $\overline{E}$, $\overline{S}$ Inputs	V_{IH} = 2.4V		6	80	μA
All Inputs	V_{IH} = 5.5V			1.0	mA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Min			0.8	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max				
CP, $\overline{S}$ Inputs	V_{IL} = 0.4V		−1.0	−1.6	mA
D, $\overline{E}$ Inputs	V_{IL} = 0.4V		−1.0	−3.2	mA
Logical "1" Output Voltage (V_{OH})	V_{CC} = Min, I_{OH} = −0.48 mA	2.4	3.6		V
Output Short Circuit Current (Note 4) (I_{OS})	V_{CC} = Max; V_{OUT} = 0.0V; Output High; CP, D, $\overline{S}$, High; $\overline{E}$ Low	−10	−20	−45	mA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OL} = 9.6 mA		0.2	0.4	V
Supply Current (I_{CC})	V_{CC} = Max, All Outputs Low				
DM2502C			65	95	mA
DM2502			65	85	mA
DM2503C			60	90	mA
DM2503			60	80	mA
DM2504C			90	124	mA
DM2504			90	110	mA
Propagation Delay to a Logical "0" From CP to Any Output (t_{pd0})		10	18	28	ns
Propagation Delay to a Logical "0" From $\overline{E}$ to Q7 (Q11) Output (t_{pd0})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		16	24	ns
Propagation Delay to a Logical "1" From CP to Any Output (t_{pd1})		10	26	38	ns
Propagation Delay to a Logical "1" From $\overline{E}$ to Q7 (Q11) Output (t_{pd1})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		13	19	ns
Set-Up Time Data Input ($t_{s(D)}$)		−10	4	8	ns
Set-Up Time Start Input ($t_{s(\overline{S})}$)		0	9	16	ns
Minimum Low CP Width (t_{PWL})			30	42	ns
Minimum High CP Width (t_{PWH})			17	24	ns
Maximum Clock Frequency (f_{MAX})		15	21		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM2502, DM2503 and DM2504, and across the 0°C to +70°C range for the DM2502C, DM2503C and DM2504C. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Application Information

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator 1/2 full range + 1/2 LSB and using the complement of the MSB ($\overline{Q7}$ or $\overline{Q11}$) with a binary D/A converter. Offset binary is used in the same manner but with the MSB (Q7 or Q11). BCD D/A converters can be used with the addition of illegal code suppression logic.

ACTIVE HIGH OR ACTIVE LOW LOGIC

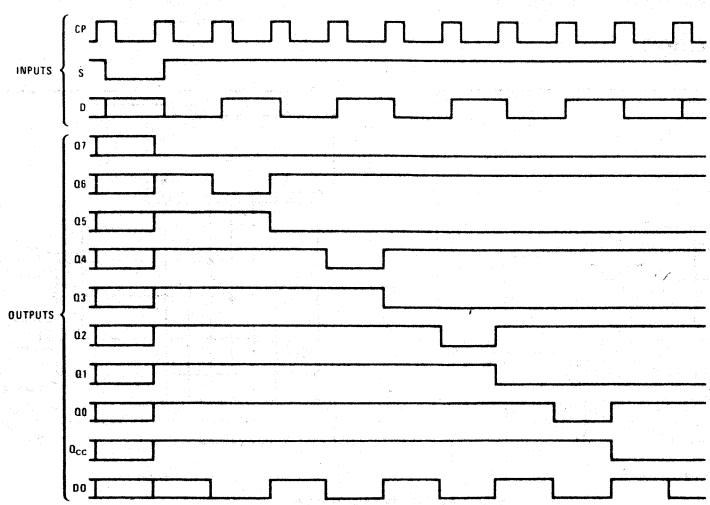
The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start signal resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

Timing Diagram

DM2502, DM2503



Application Information (Continued)

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below ±1/2 LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +1/2 LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −1/2 LSB.

Definition of Terms

CP: The clock input of the register.

D: The serial data input of the register.

DO: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_i i = 7 (11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

Q7 (11): The true output of the MSB of the register.

$\overline{Q7}$ (11): The complement output of the MSB of the register.

$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

Truth Table

DM2502, DM2503

TIME	INPUTS			OUTPUTS[1]									
t_n	D	$\overline{S}$	$\overline{E}$[2]	D0[3]	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

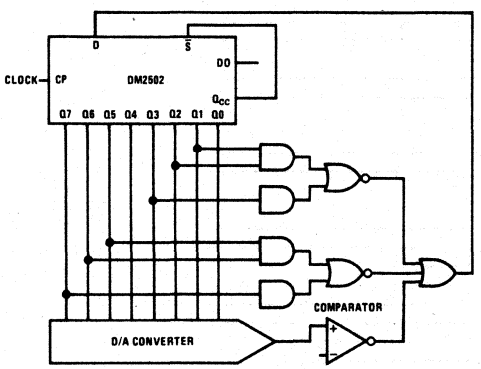
Note 1: Truth table for DM2504 is extended to include 12 outputs.

Note 2: Truth table for DM2502 does not include $\overline{E}$ column or last line in truth table shown.

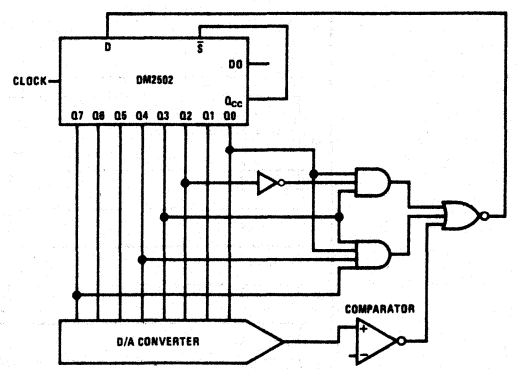
Note 3: Truth table for DM2503 does not include D0 column.

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NC = No Change

Typical Applications



Active High

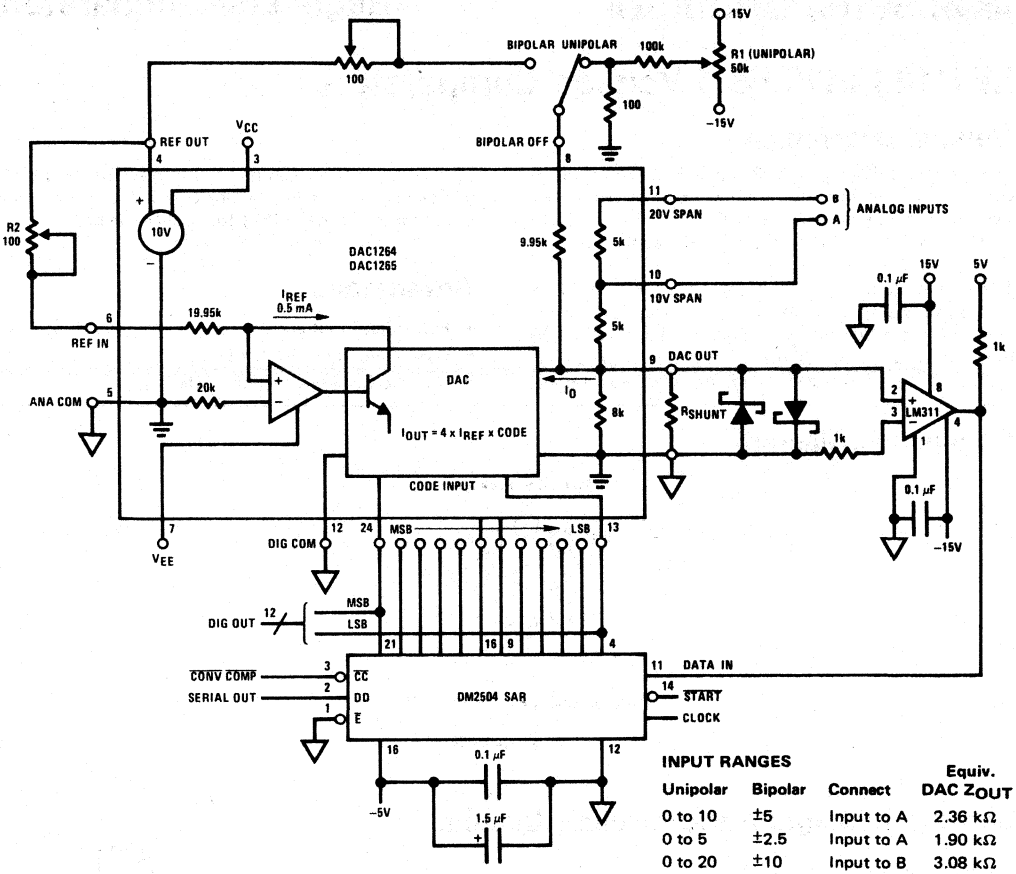


Active Low

BCD Illegal Code Suppression

Typical Applications (Continued)

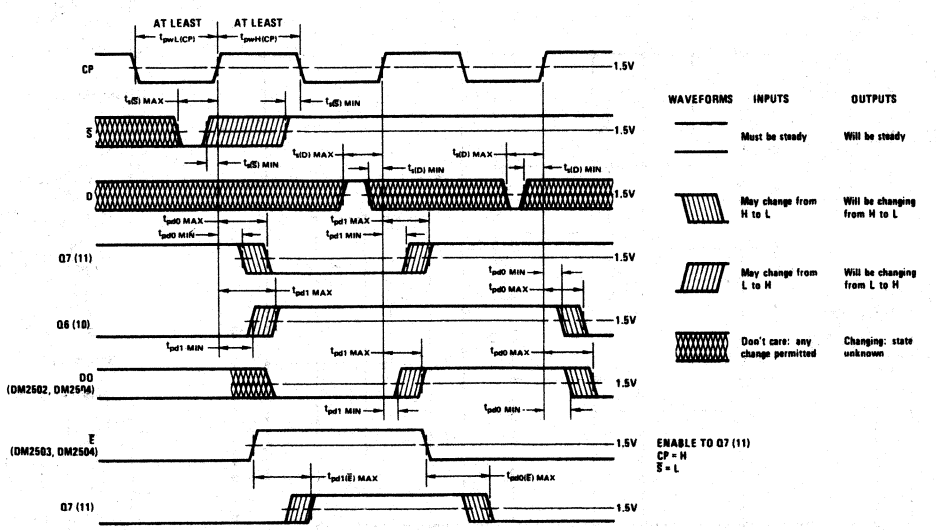
Fast Precision Analog-to-Digital Converter



INPUT RANGES

Unipolar	Bipolar	Connect	Equiv. DAC Z_{OUT}
0 to 10	±5	Input to A	2.36 kΩ
0 to 5	±2.5	Input to A	1.90 kΩ
0 to 20	±10	Input to B B to DAC OUT	3.08 kΩ

Switching Time Waveforms



National Semiconductor

Successive Approximation Registers/Comparators

LF111/LF211/LF311 Voltage Comparators

General Description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

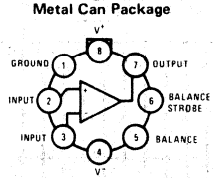
Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents. See the "application hints" of the LM311 for application help.

Advantages

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

Connection Diagram

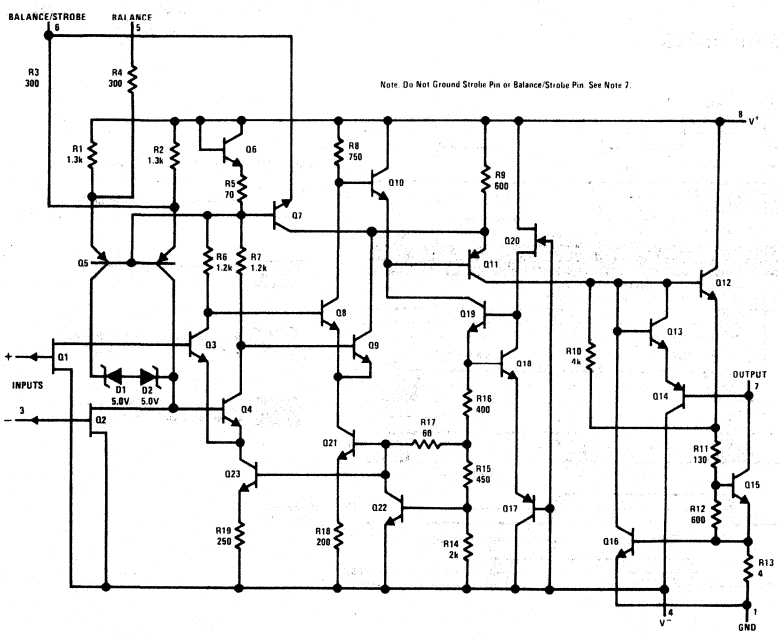
Metal Can Package

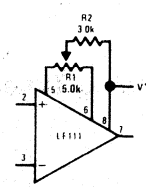


NOTE: Pin 4 connected to case.
TOP VIEW

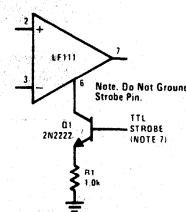
Order Number LF111H, LF211H or LF311H
See NS Package H08C

Schematic Diagram and Auxiliary Circuits

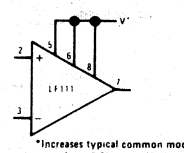




Offset Balancing



Strobing



*Increases typical common mode slew from 7.0V μs to 18V μs.

Increasing Input Stage Current*

Absolute Maximum Ratings

	LF111/LF211	LF311
Total Supply Voltage (V_{84})	36V	36V
Output to Negative Supply Voltage (V_{74})	50V	40V
Ground to Negative Supply Voltage (V_{14})	30V	30V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Power Dissipation (Note 2)	500 mW	500 mW
Output Short Circuit Duration	10 seconds	10 seconds
Operating Temperature Range		
LF111	−55°C to +125°C	
LF211	−25°C to +85°C	
LF311		0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (LF111/LF211) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, R_S		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	25	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		20	50	pA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5.0$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5.0$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)				6.0	mV
Input Offset Current (Note 4)	$V_S = ±15V$, $V_{CM} = 0$ (Note 6)		2.0	3.0	nA
Input Bias Current	$V_S = ±15V$, $V_{CM} = 0$ (Note 6)		5.0	7.0	nA
Input Voltage Range		−13.5	±14	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6.0$ mV, $I_{SINK} \leq 8.0$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5.0$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3: These specifications apply for $V_S = ±15V$, and the Ground pin at ground, and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Electrical Characteristics (LF311) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	10	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	75	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		25	150	pA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			15	mV
Input Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		1.0		nA
Input Bias Current	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		3.0		nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8.0$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 mV supply up to ±15V supplies.

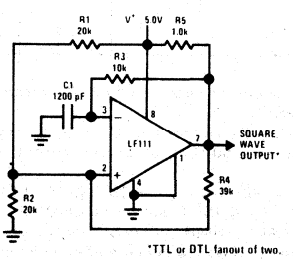
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

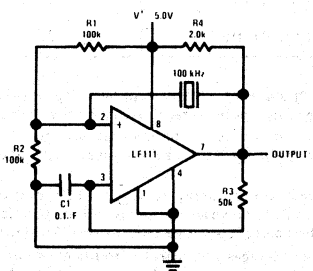
Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Typical Applications



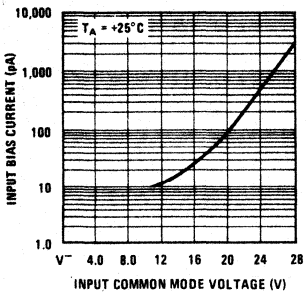
100 kHz Free Running Multivibrator



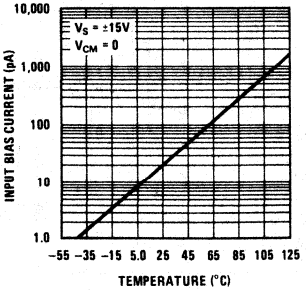
Crystal Oscillator

Typical Performance

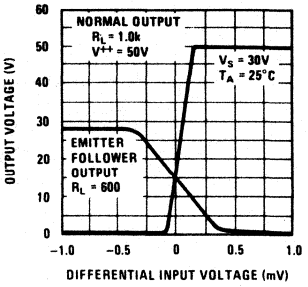
Input Bias Current vs Common Mode



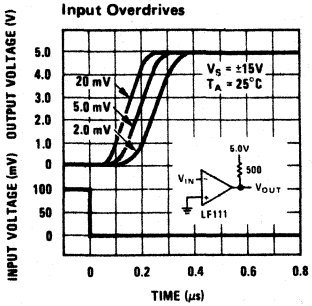
Input Bias Current vs Temperature



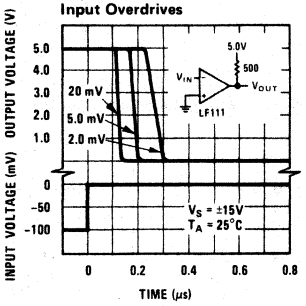
Transfer Function



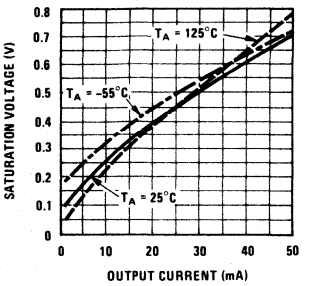
Response Time for Various Input Overdrives



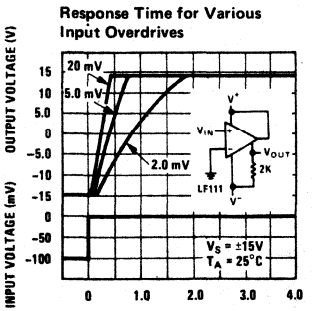
Response Time for Various Input Overdrives



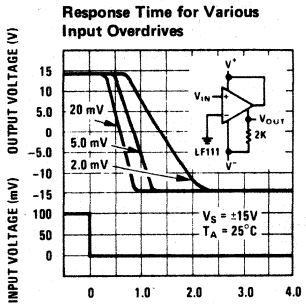
Output Saturation Voltage



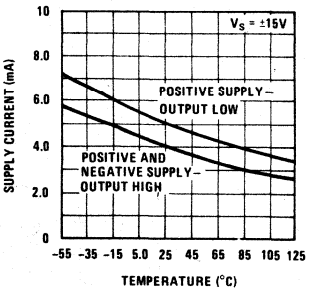
Response Time for Various Input Overdrives



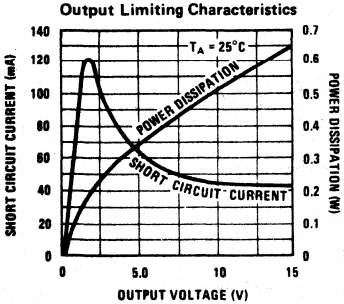
Response Time for Various Input Overdrives



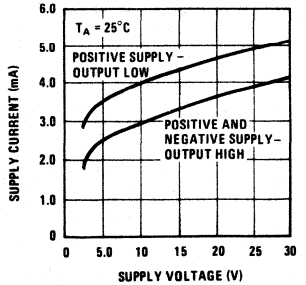
Supply Current



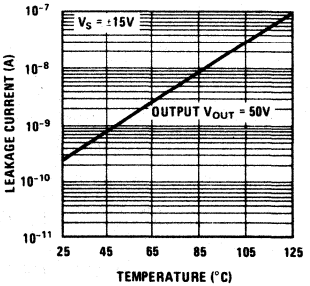
Output Limiting Characteristics



Supply Current

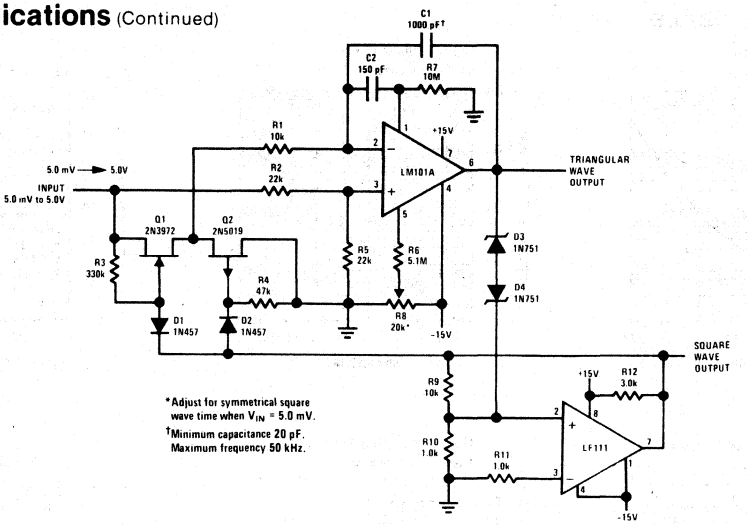


Leakage Currents

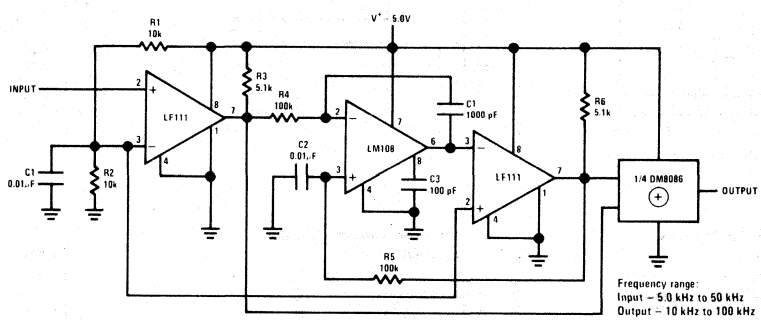


13

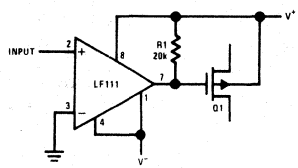
Typical Applications (Continued)



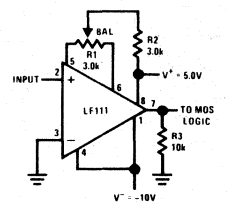
10 Hz to 10 kHz Voltage Controlled Oscillator



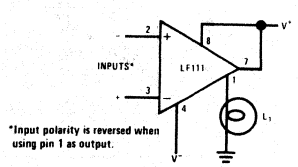
Frequency Doubler



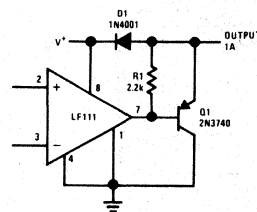
Zero Crossing Detector Driving MOS Switch



Zero Crossing Detector Driving MOS Logic

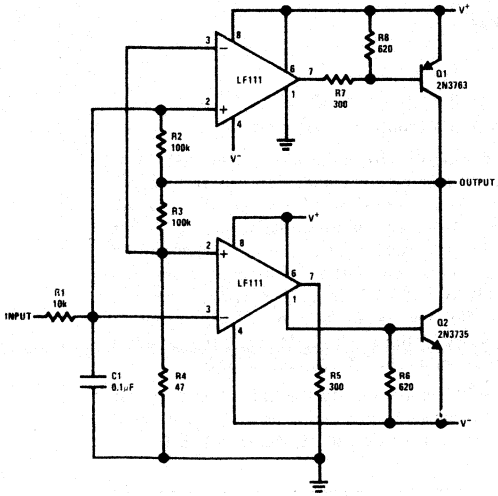


Driving Ground-Referred Load

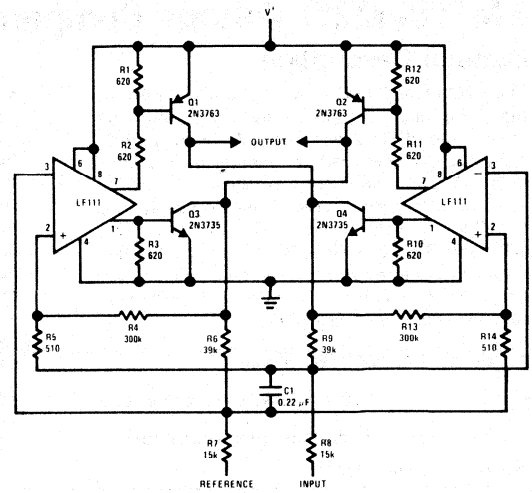


Comparator and Solenoid Driver

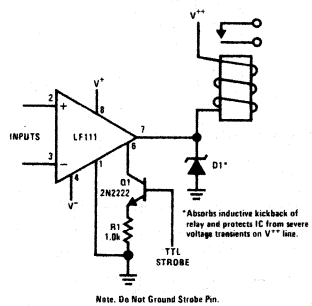
Typical Applications (Continued)



Switching Power Amplifier

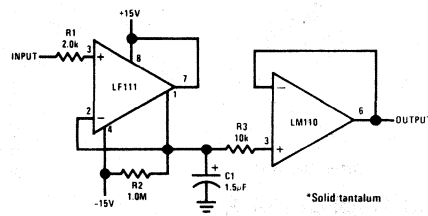


Switching Power Amplifier

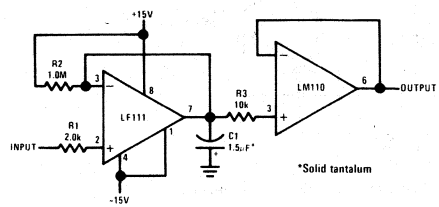


Note. Do Not Ground Strobe Pin.

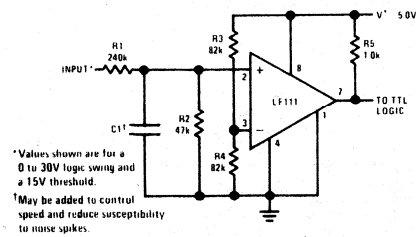
Relay Driver with Strobe



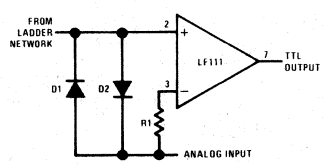
Positive Peak Detector



Negative Peak Detector



TTL Interface with High Level Logic



Using Clamp Diodes to Improve Response

13

National Semiconductor

Successive Approximation Registers/Comparators

LM111/LM211 Voltage Comparator †

General Description

The LM111 and LM211 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA. Outstanding characteristics include:

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

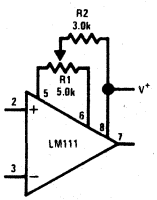
Both the inputs and the outputs of the LM111 or the LM211 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

The LM211 is identical to the LM111, except that its performance is specified over a −25°C to 85°C temperature range instead of −55°C to 125°C.

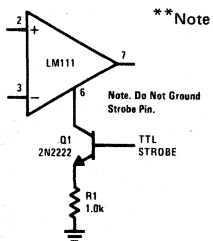
†See application hints LM311

Auxiliary Circuits**

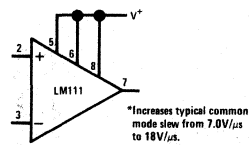
**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.



Offset Balancing

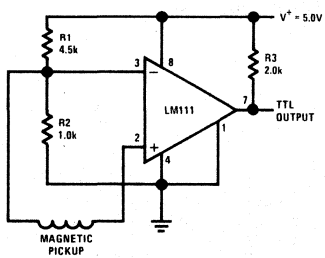


Strobing

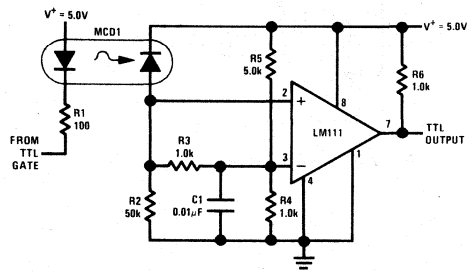


Increasing Input Stage Current*

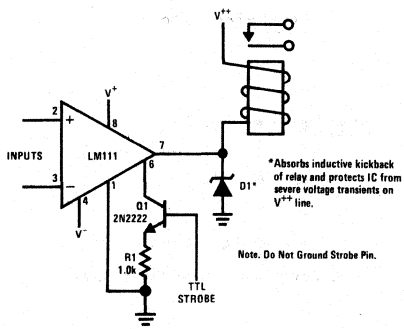
Typical Applications**



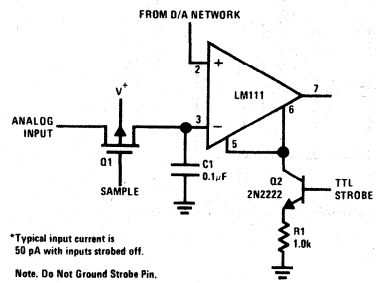
Detector for Magnetic Transducer



Digital Transmission Isolator



Relay Driver with Strobe*



Strobing off Both Input* and Output Stages

Absolute Maximum Ratings

Total Supply Voltage (V_{84})		36V
Output to Negative Supply Voltage (V_{74})		50V
Ground to Negative Supply Voltage (V_{14})		30V
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Power Dissipation (Note 2)		500 mW
Output Short Circuit Duration		10 sec
Operating Temperature Range	LM111	−55°C to 125°C
	LM211	−25°C to 85°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (soldering, 10 sec)		300°C
Voltage at Strobe Pin		V^+−5V

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current (Note 6)	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range	$V^+ = 15V$, $V^- = -15V$, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,−14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for V_S = ±15V and Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

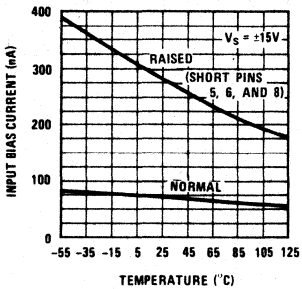
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

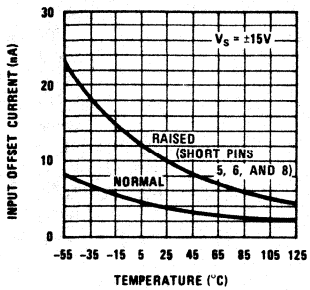
Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Typical Performance Characteristics

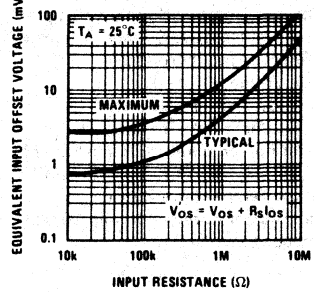
Input Bias Current



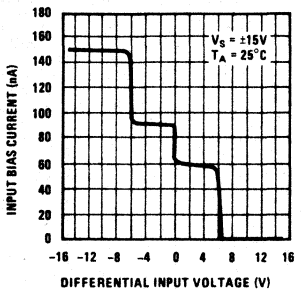
Input Offset Current



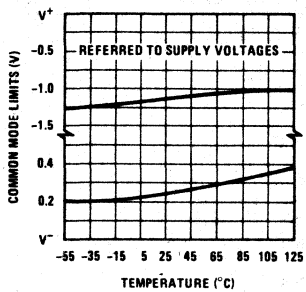
Offset Error



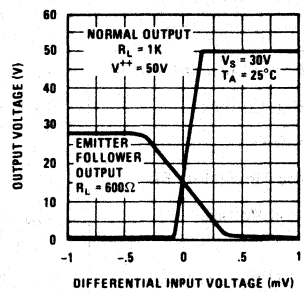
Input Characteristics



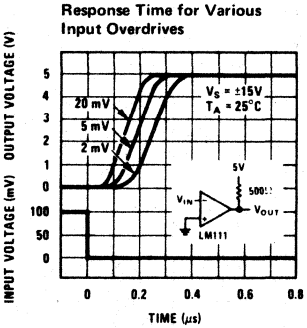
Common Mode Limits



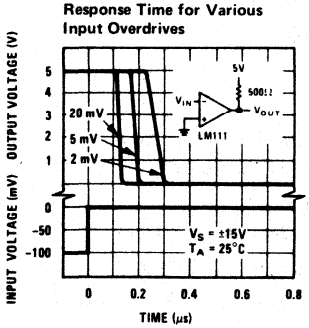
Transfer Function



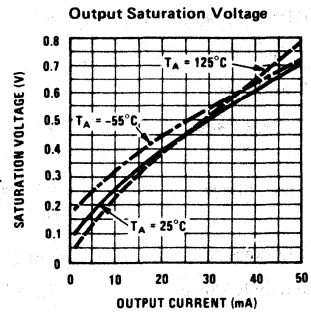
Response Time for Various Input Overdrives



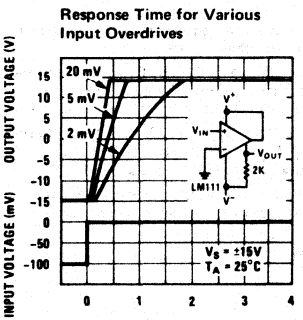
Response Time for Various Input Overdrives



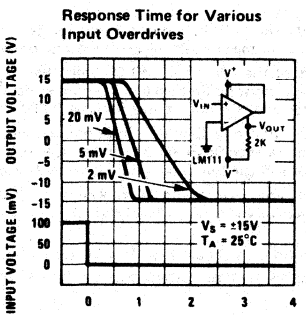
Output Saturation Voltage



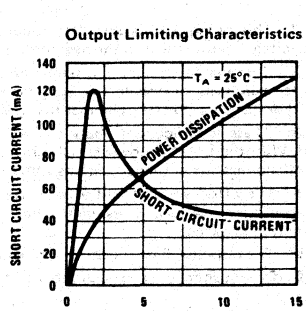
Response Time for Various Input Overdrives



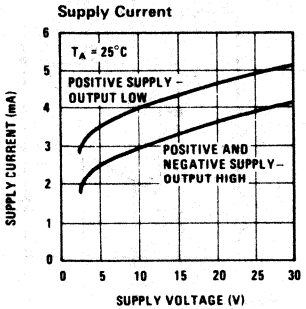
Response Time for Various Input Overdrives

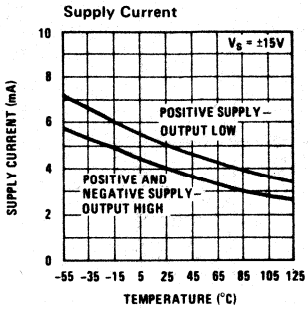


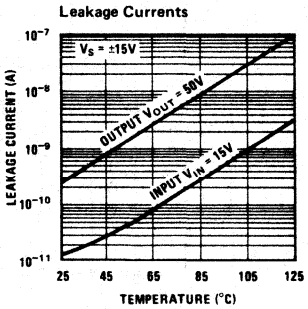
Output Limiting Characteristics



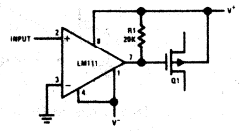
Typical Performance Characteristics (Continued)



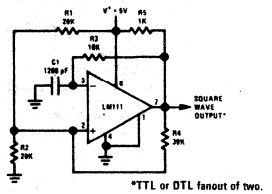




Typical Applications (Continued)

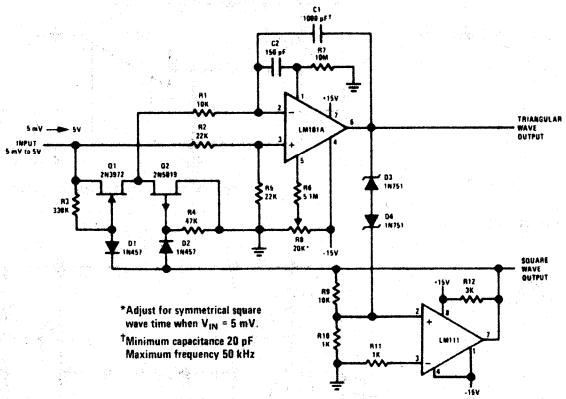


Zero Crossing Detector Driving MOS Switch



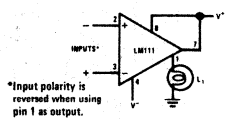
*TTL or DTL fanout of two.

100 kHz Free Running Multivibrator



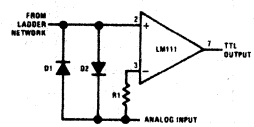
*Adjust for symmetrical square wave time when V_{IN} = 5 mV.
†Minimum capacitance 20 pF
Maximum frequency 50 kHz

10 Hz to 10 kHz Voltage Controlled Oscillator

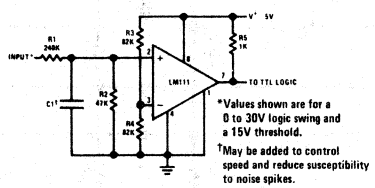


*Input polarity is reversed when using pin 1 as output.

Driving Ground-Referred Load

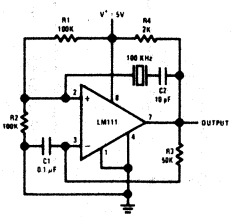


Using Clamp Diodes to Improve Response

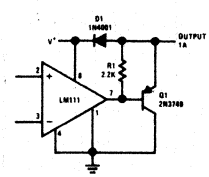


*Values shown are for a 0 to 30V logic swing and a 15V threshold.
†May be added to control speed and reduce susceptibility to noise spikes.

TTL Interface with High Level Logic

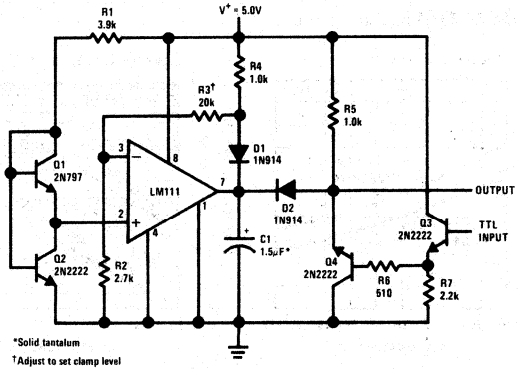


Crystal Oscillator

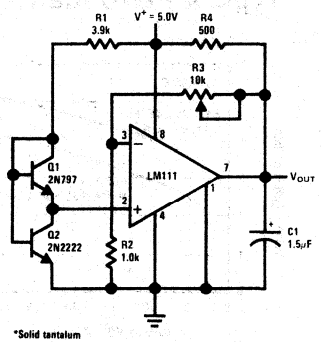


Comparator and Solenoid Driver

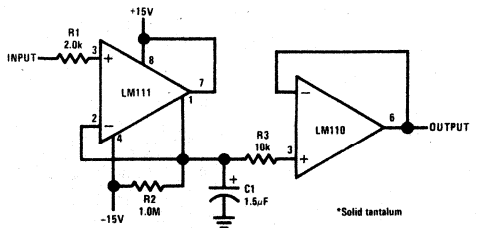
Typical Applications (Continued)



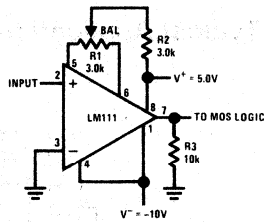
Precision Squarer



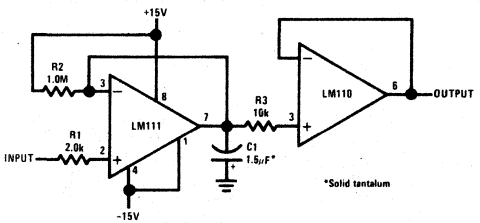
Low Voltage Adjustable Reference Supply



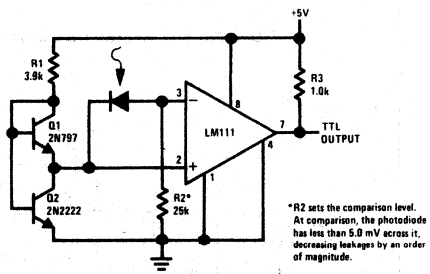
Positive Peak Detector



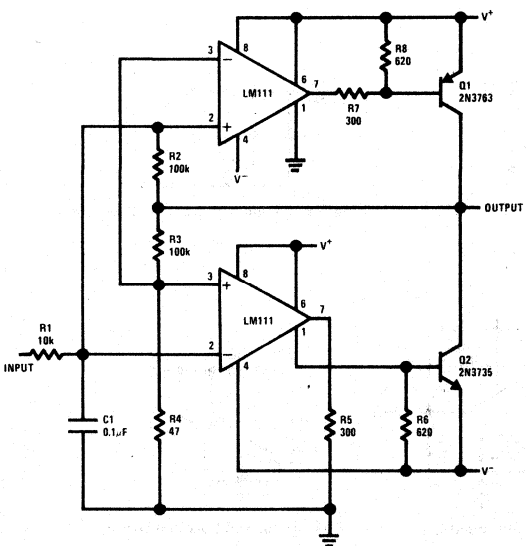
Zero Crossing Detector driving MOS logic



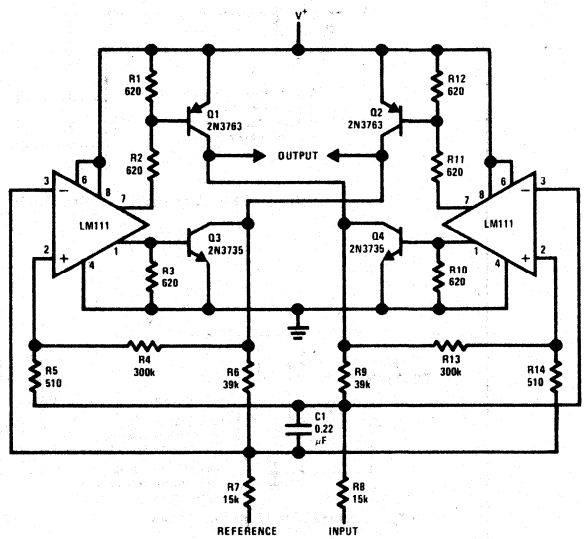
Negative Peak Detector



Precision Photodiode Comparator

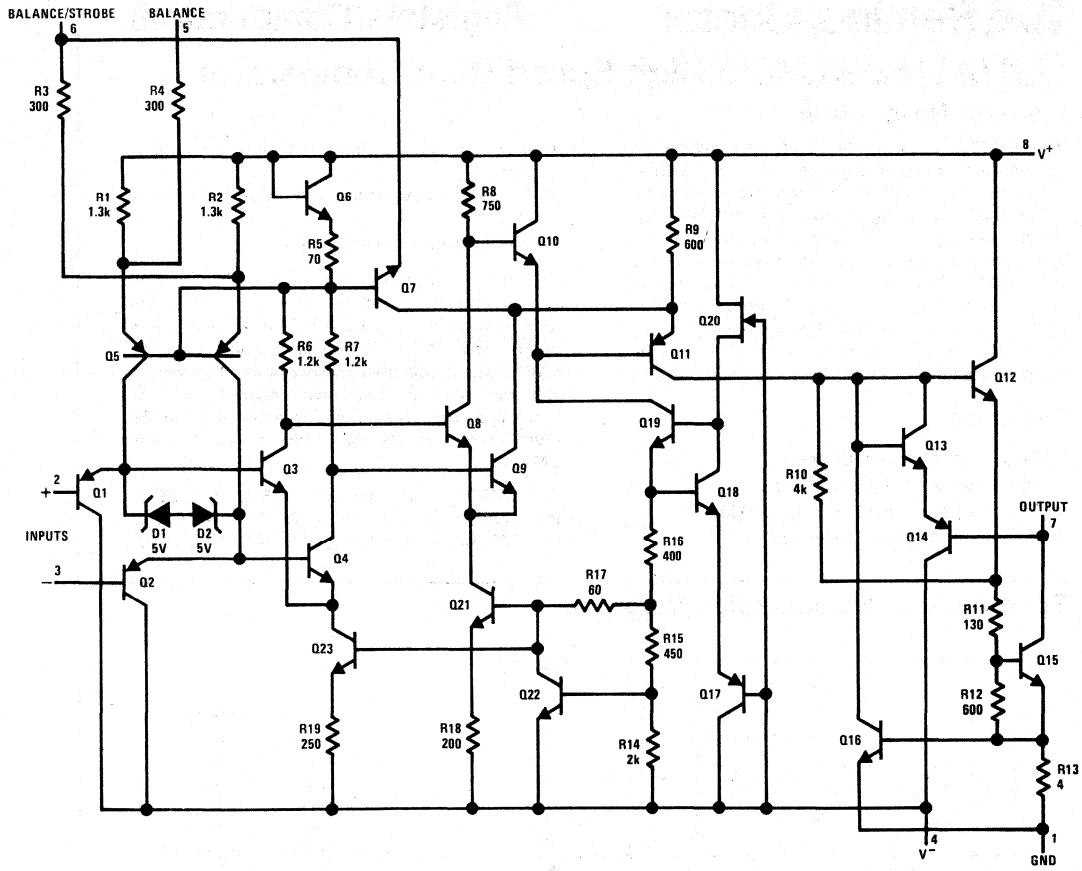


Switching Power Amplifier



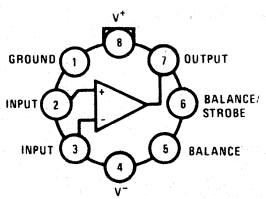
Switching Power Amplifier

Schematic Diagram



Connection Diagrams *

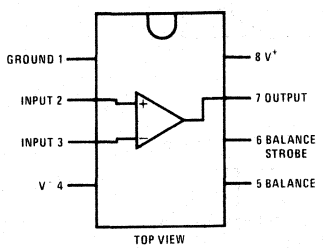
Metal Can Package



NOTE: Pin 4 connected to case.
TOP VIEW

Order Number LM111H or LM211H
See NS Package H08C

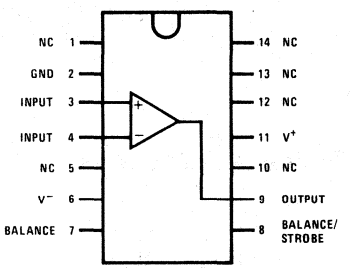
8-Pin Dual-In-Line Package



TOP VIEW

Order Number LM111J-8
or LM211J-8
See NS Package J08A

14-Pin Dual-In-Line Package



Note: Pin 6 connected to bottom of package.
TOP VIEW

Order Number LM111J or LM211J
See NS Package J14A

*Pin connections shown are for metal can.

National Semiconductor

Successive Approximation Registers/Comparators

LM119/LM219/LM319 High Speed Dual Comparator

General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA. Outstanding features include:

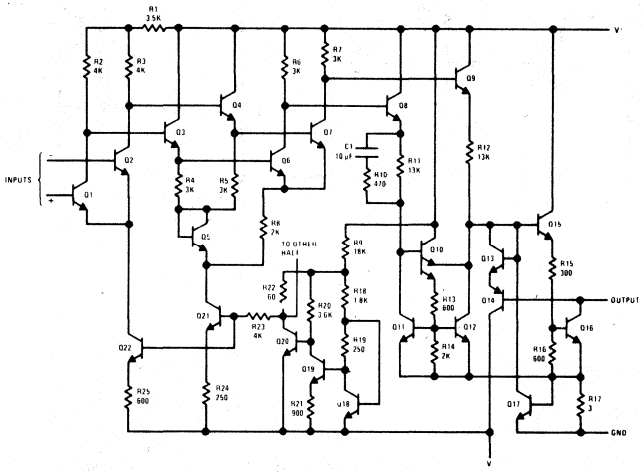
Features

- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

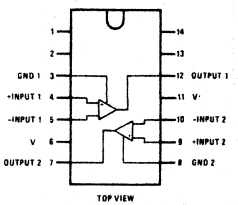
Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

Schematic and Connection Diagrams



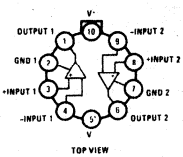
Dual-In-Line-Package



Order Number LM319N
See NS Package N14A

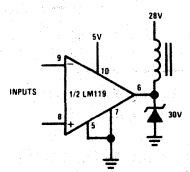
Order Number LM119J, LM219J or LM319J
See NS Package J14A

Metal Can Package

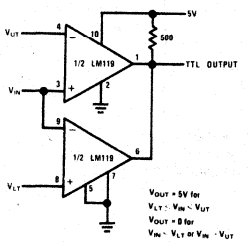


Order Number LM119H, LM219H or LM319H
See NS Package H10C

Typical Applications



Relay Driver



Window Detector

Absolute Maximum Ratings LM119/LM219

Total Supply Voltage	36V	Power Dissipation (Note 2)	500 mW
Output to Negative Supply Voltage	36V	Output Short Circuit Duration	10 sec
Ground to Negative Supply Voltage	25V	Operating Temperature Range LM119	−55°C to 125°C
Ground to Positive Supply Voltage	18V	LM219	−25°C to 85°C
Differential Input Voltage	±5V	Storage Temperature Range	−65°C to 150°C
Input Voltage (Note 1)	±15V	Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		30	75	nA
Input Bias Current	$T_A = 25°C$		150	500	nA
Voltage Gain	$T_A = 25°C$	10	40		V/mV
Response Time (Note 5)	$T_A = 25°C$ $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 25$ mA				
	$T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$				
	$T_A = 25°C$		0.2	2	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			7	mV
Input Offset Current (Note 4)				100	nA
Input Bias Current				1000	nA
Input Voltage Range	$V_S = \pm 15V$		±13		V
	$V^+ = 5V$, $V^- = 0$	1		3	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$				
	$V_{IN} \leq -6$ mV, $I_{SINK} \leq 3.2$ mA				
	$T_A \geq 0°C$		0.23	0.4	V
	$T_A \leq 0°C$			0.6	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$, $V_{GND} = 0V$		1	10	μA
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		8	11.5	mA
Negative Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		3	4.5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM119 is 150°C, while that of the LM219 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM219, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Absolute Maximum Ratings LM319

Total Supply Voltage	36V	Power Dissipation (Note 2)	500 mW
Output to Negative Supply Voltage	36V	Output Short Circuit Duration	10 sec
Ground to Negative Supply Voltage	25V	Operating Temperature Range LM319	0°C to 70°C
Ground to Positive Supply Voltage	18V	Storage Temperature Range	-65°C to 150°C
Differential Input Voltage	±5V	Lead Temperature (Soldering, 10 sec)	300°C
Input Voltage (Note 1)	±15V		

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		2.0	8.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		80	200	nA
Input Bias Current	$T_A = 25°C$		250	1000	nA
Voltage Gain	$T_A = 25°C$	8	40		V/mV
Response Time (Note 5)	$T_A = 25°C$ $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$, $T_A = 25°C$		0.2	10	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			10	mV
Input Offset Current (Note 4)				300	nA
Input Bias Current				1200	nA
Input Voltage Range	$V_S = \pm 15V$		±13		V
	$V^+ = 5V$, $V^- = 0$	1		3	V
Saturation Voltage	$V^+ > 4.5V$, $V^- = 0$		0.3	0.4	V
	$V_{IN} \leq -10$ mV, $I_{SINK} \leq 3.2$ mA				
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		8	12.5	mA
Negative Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		3	5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM319 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

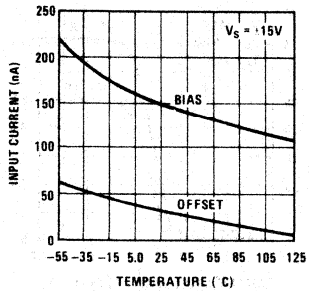
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

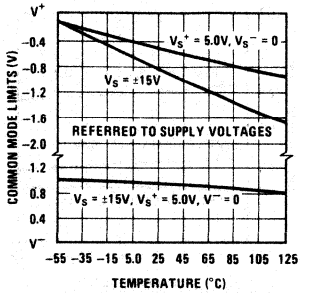
Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Typical Performance Characteristics LM119/LM219

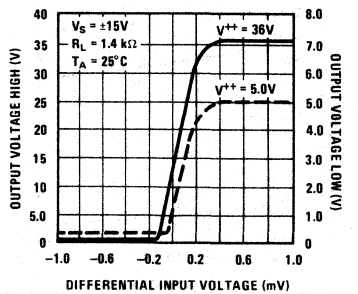
Input Currents



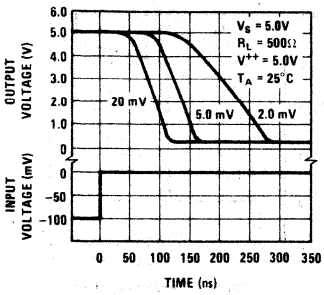
Common Mode Limits



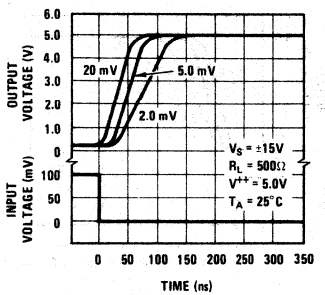
Transfer Function



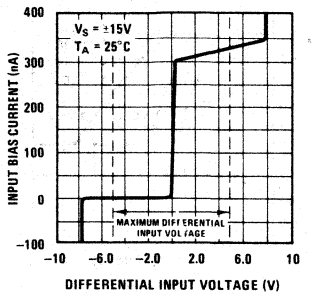
Response Time for Various Input Overdrives



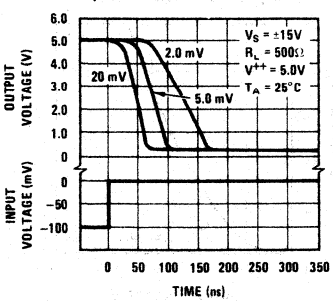
Response Time for Various Input Overdrives



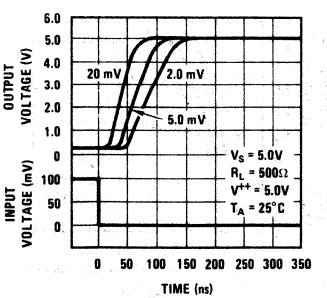
Input Characteristics



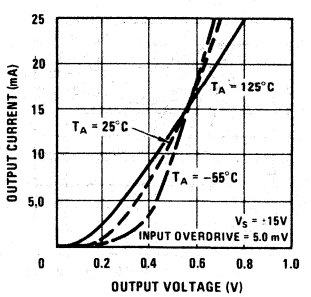
Response Time for Various Input Overdrives



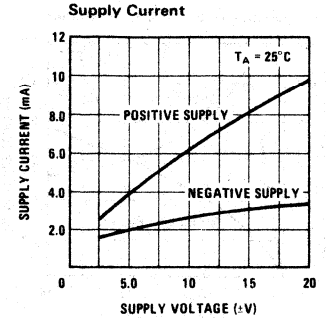
Response Time for Various Input Overdrives



Output Saturation Voltage



Supply Current



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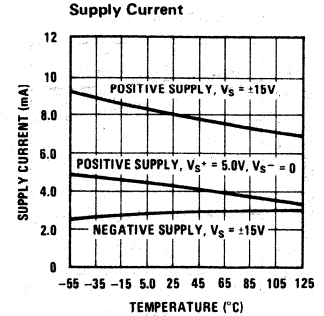
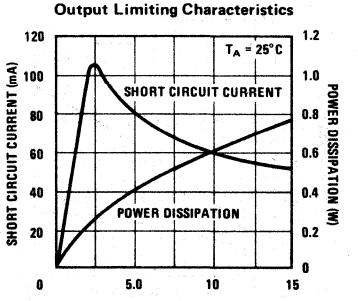


Output Limiting Characteristics



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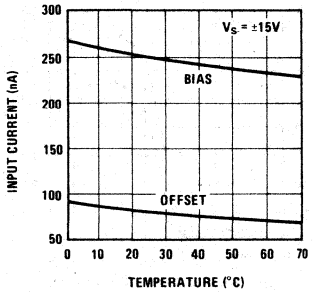
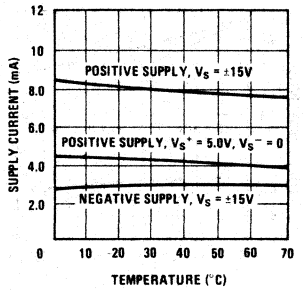
Typical Performance Characteristics LM319

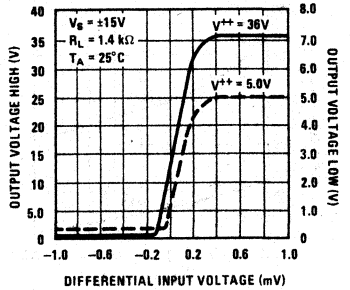
Input Currents



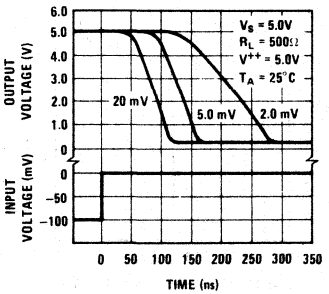
Supply Currents



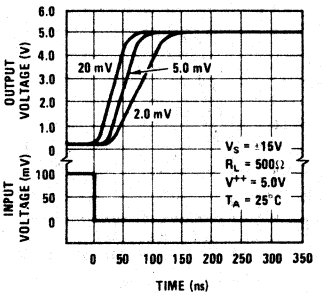
Transfer Function



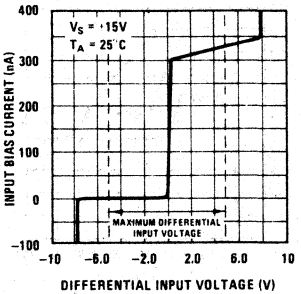
Response Time for Various Input Overdrives



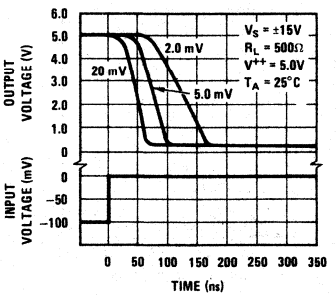
Response Time for Various Input Overdrives



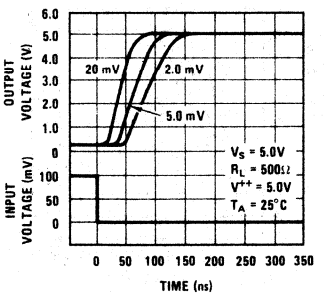
Input Characteristics



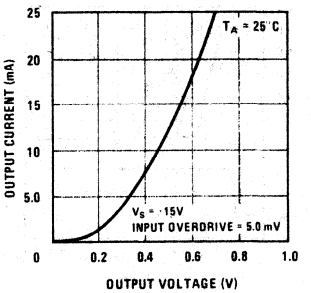
Response Time for Various Input Overdrives



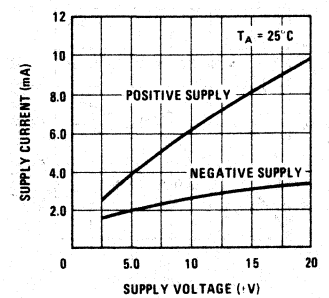
Response Time for Various Input Overdrives



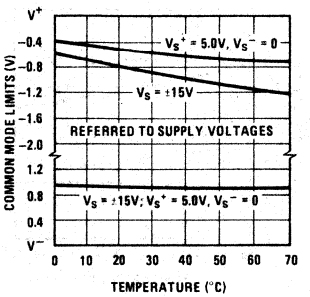
Output Saturation Voltage



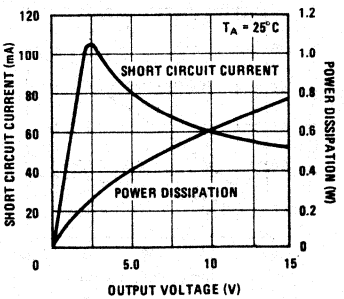
Supply Current



Common Mode Limits



Output Limiting Characteristics



National Semiconductor

Successive Approximation Registers/Comparators

LM139/239/339, LM139A/239A/339A, LM2901,LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic– where the low power drain of the LM339 is a distinct advantage over standard comparators.

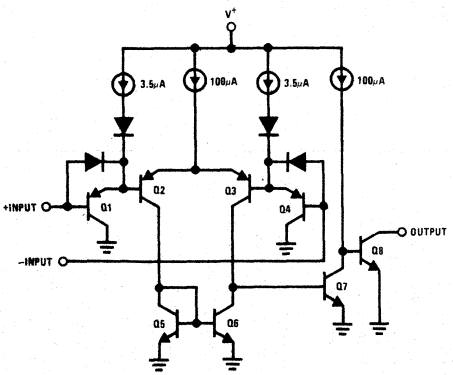
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near gnd
- Compatible with all forms of logic
- Power drain suitable for battery operation

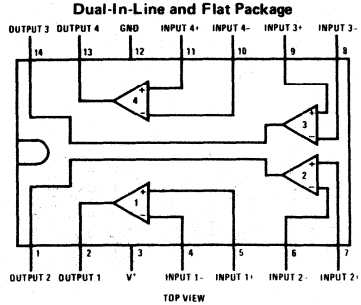
Features

- Wide single supply voltage range or dual supplies
  LM139 series, 2 V_{DC} to 36 V_{DC} or
  LM139A series, LM2901 ±1 V_{DC} to ±18 V_{DC}
  LM3302 2 V_{DC} to 28 V_{DC}
  or ±1 V_{DC} to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage (2 mW/comparator at +5 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and offset voltage ±3 mV
- Input common-mode voltage range includes gnd
- Differential input voltage range equal to the power supply voltage
- Low output 250 mV at 4 mA
  saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



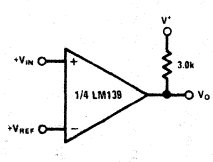
Dual-In-Line and Flat Package



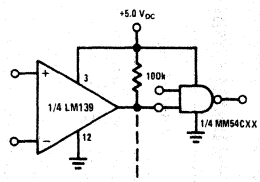
Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
See NS Package J14A

Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package N14A

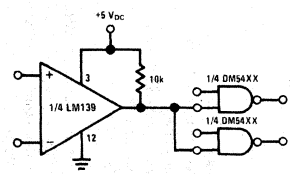
Typical Applications (V^+ = 5.0 V_{DC})



Basic Comparator



Driving CMOS



Driving TTL

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Absolute Maximum Ratings

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	800 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$), (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM339A	0°C to +70°C	−40°C to +85°C
LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics ($V^+ = 5\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3	±20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $T_A = 25°C$, (Note 5)		25	100		25	250		25	100		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5	±50		±3	±100	nA_{DC}
Input Common-Mode Voltage Range	$T_A = 25°C$, (Note 6)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators, $T_A = 25°C$		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2	mA_{DC}
	$R_L = \infty$, $V^+ = 30V$, $T_A = 25°C$														1	2.5				mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$ (To Support Large V_O Swing), $T_A = 25°C$	50	200		50	200			200			200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC}, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300			300			300			300			300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5\ V_{DC}$, $T_A = 25°C$	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = 25°C$		250	400		250	400		250	400		250	400			400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$, $T_A = 25°C$		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 9)			4.0			4.0			9.0			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150			±100			±150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range		0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			V^+			V^+			36			36	0		V^+			V_{CC}	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$.

Note 4: These specifications apply for $V^+ = 5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to $+30\ V_{DC}$ without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

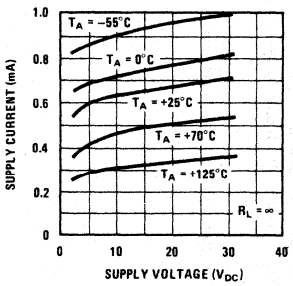
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$).

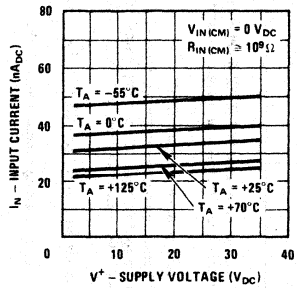
Note 10: For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

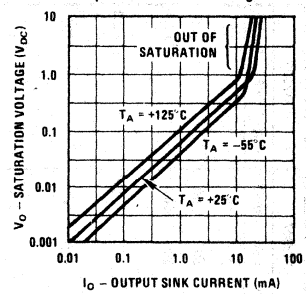
Supply Current



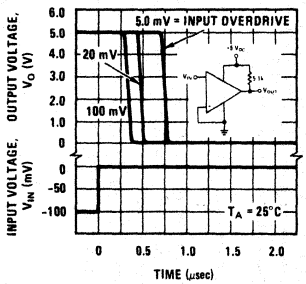
Input Current



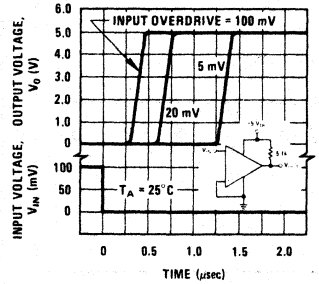
Output Saturation Voltage



Response Time for Various Input Overdrives – Negative Transition

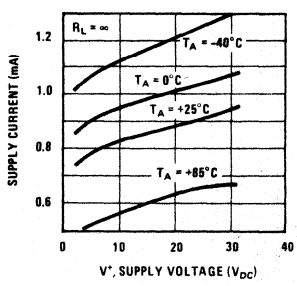


Response Time for Various Input Overdrives – Positive Transition

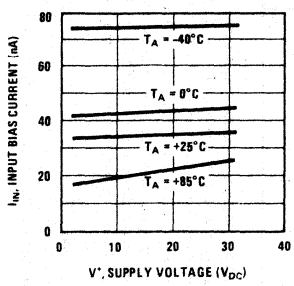


Typical Performance Characteristics LM2901

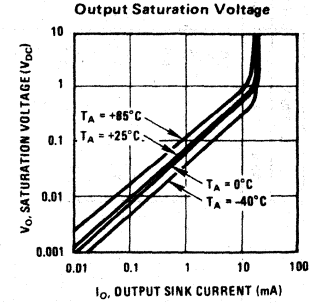
Supply Current



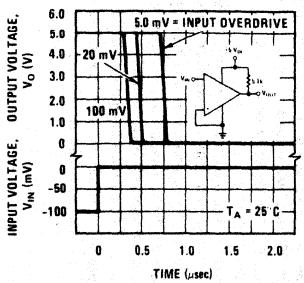
Input Current



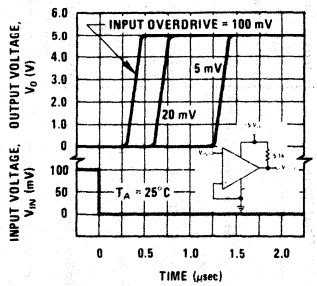
Output Saturation Voltage



Response Time for Various Input Overdrives–Negative Transition



Response Time for Various Input Overdrives–Positive Transition



Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

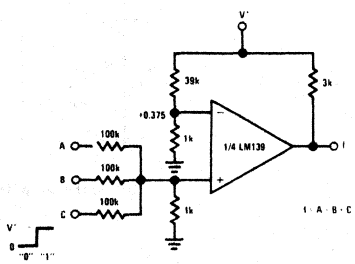
The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

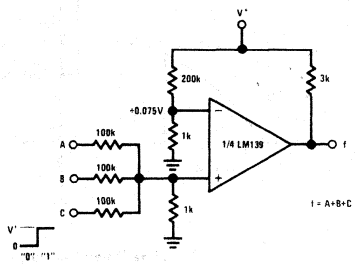
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

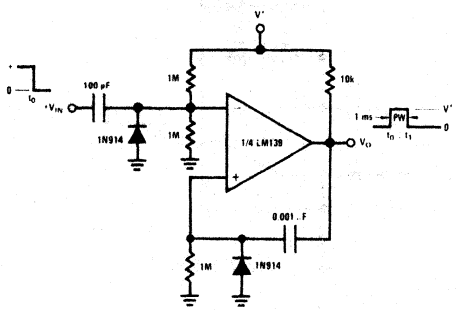
Typical Applications ($V^+ = 15\ V_{DC}$)



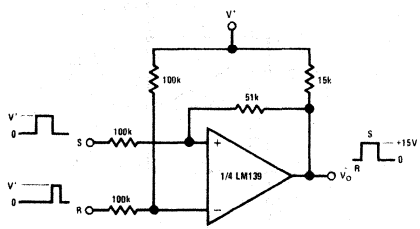
AND Gate



OR Gate

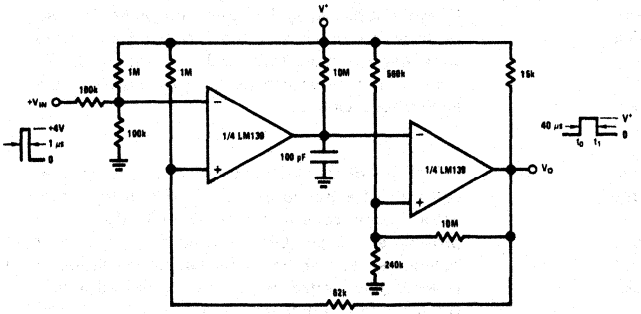


One-Shot Multivibrator

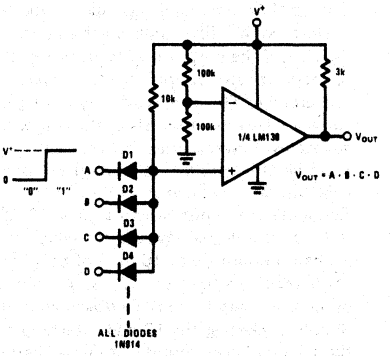


Bi-Stable Multivibrator

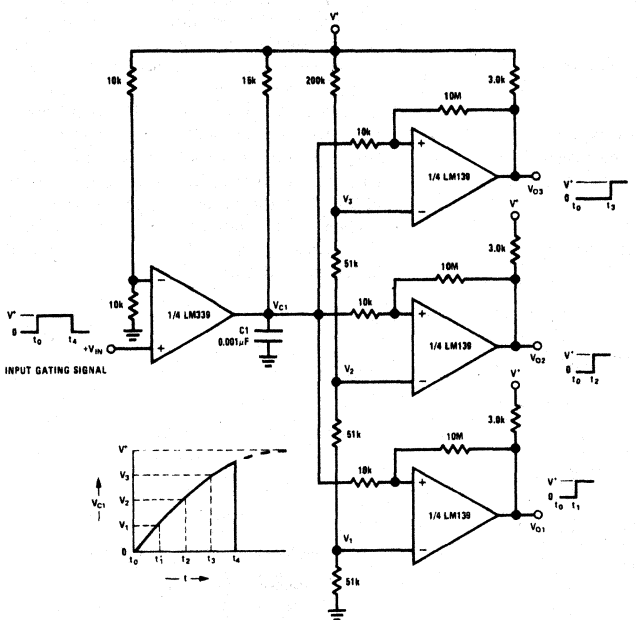
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



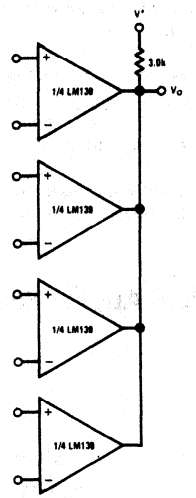
One-Shot Multivibrator with Input Lock Out



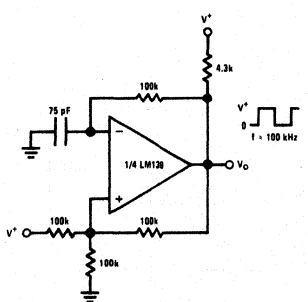
Large Fan-in AND Gate



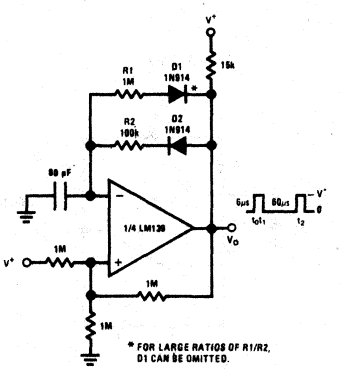
Time Delay Generator



ORing the Outputs

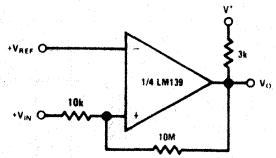


Squarewave Oscillator

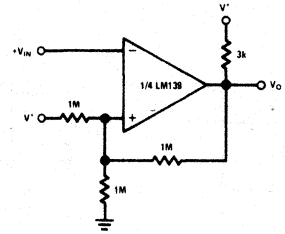


Pulse Generator

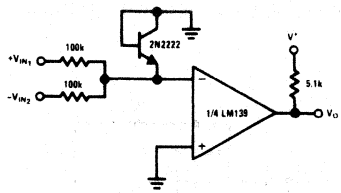
Typical Applications (Continued) ($V^+ = 5\ V_{DC}$)



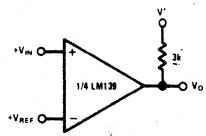
Non-Inverting Comparator with Hysteresis



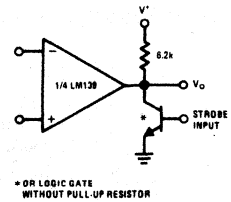
Inverting Comparator with Hysteresis



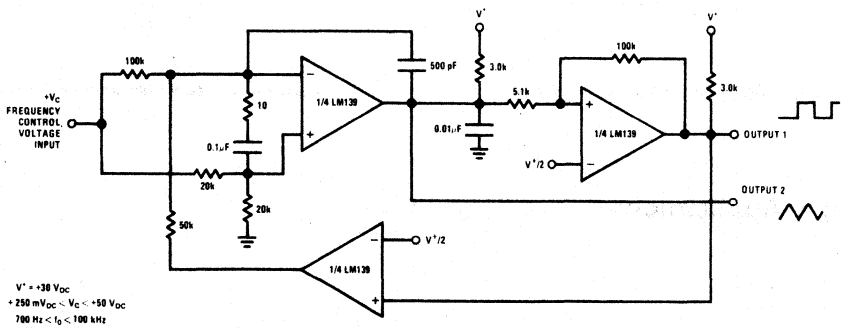
Comparing Input Voltages of Opposite Polarity



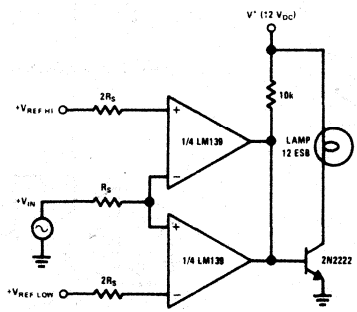
Basic Comparator



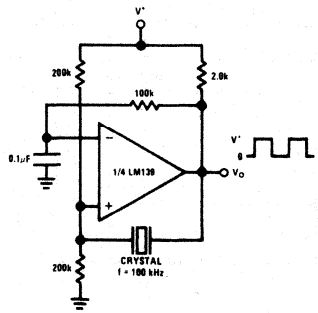
Output Strobing



Two-Decade High-Frequency VCO

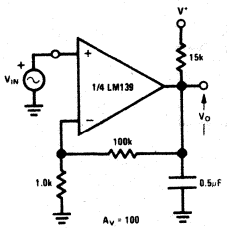


Limit Comparator

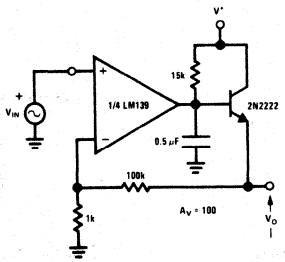


Crystal Controlled Oscillator

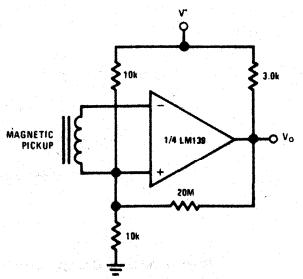
Typical Applications (Continued) ($V^+ = 5\ V_{DC}$)



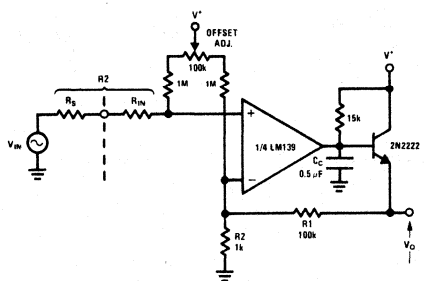
Low Frequency Op Amp



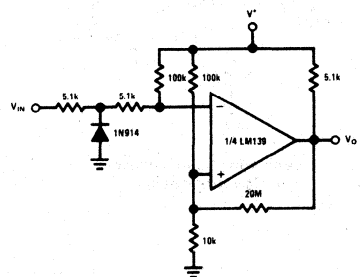
Low Frequency Op Amp
(V_O = 0V for V_{IN} = 0V)



Transducer Amplifier

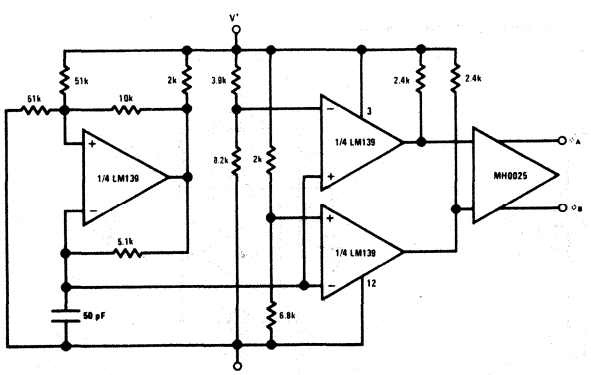


Low Frequency Op Amp with Offset Adjust

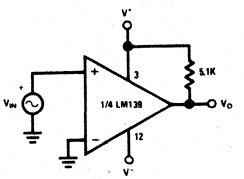


Zero Crossing Detector (Single Power Supply)

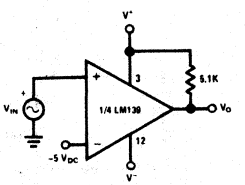
Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)



MOS Clock Driver



Zero Crossing Detector



Comparator With a Negative Reference

National Semiconductor

Successive Approximation Registers/Comparators

LM160/LM260/LM360 High Speed Differential Comparator

General Description

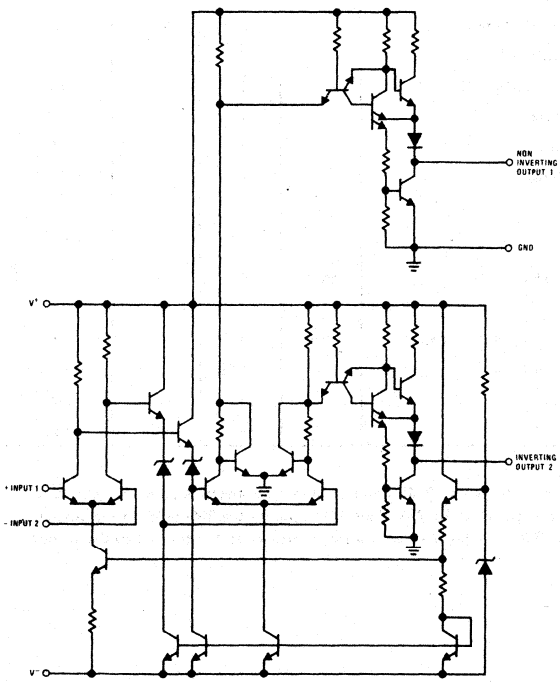
The LM160/LM260/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 500 mV.

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disc file systems.

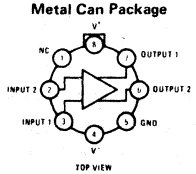
Features

- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

Schematic and Connection Diagrams

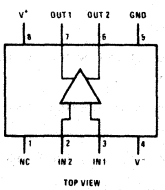


Metal Can Package



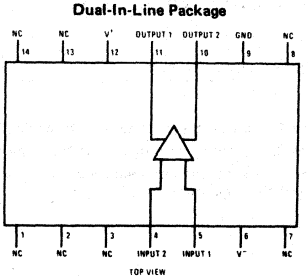
Order Number LM160H, LM260H or LM360H
See NS Package H08C

Dual-In-Line Package



Order Number LM360N
See NS Package N08B

Dual-In-Line Package



Order Number LM360N-14
See NS Package N14A

Order Number LM160J-14, LM260J-14
See NS Package J14A

Absolute Maximum Ratings

Positive Supply Voltage	+8V	Operating Temperature Range	
Negative Supply Voltage	−8V	LM160	−55°C to +125°C
Peak Output Current	20 mA	LM260	−25°C to +85°C
Differential Input Voltage	±5V	LM360	0°C to +70°C
Input Voltage	$V^+ \geq V_{IN} \geq V^-$	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

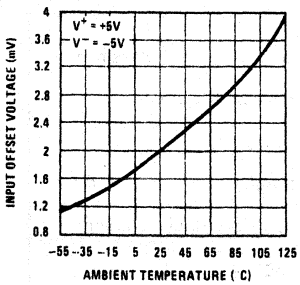
Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Conditions					
Supply Voltage V_{CC}^+		4.5	5	6.5	V
Supply Voltage V_{CC}^-		−4.5	−5	−6.5	V
Input Offset Voltage	$R_S \leq 200\Omega$		2	5	mV
Input Offset Current			.5	3	μA
Input Bias Current			5	20	μA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	$T_A = 25°C$, $V_S = \pm5V$ (Note 1)		13	25	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Note 2)		12	20	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Note 3)		14		ns
Response Time Difference Between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		μV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	$V_S = \pm6.5V$	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	$I_{OUT} = -320\mu A$, $V_S = \pm4.5V$	2.4	3		V
Output Low Voltage (Either Output)	$I_{SINK} = 6.4$ mA		.25	.4	V
Positive Supply Current	$V_S = \pm6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm6.5V$		−9	−16	mA

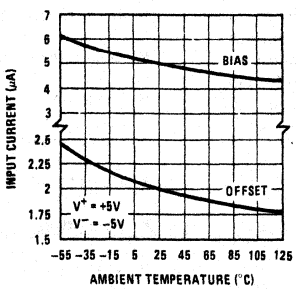
Note 1: Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
Note 2: Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.
Note 3: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Typical Performance Characteristics

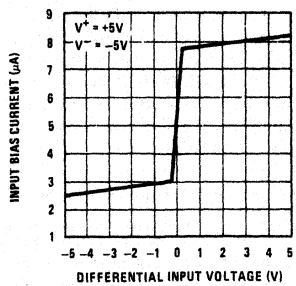
Offset Voltage



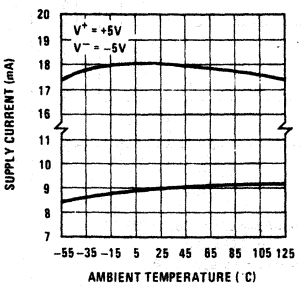
Input Currents vs Ambient Temperature



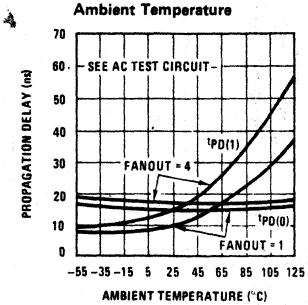
Input Characteristics



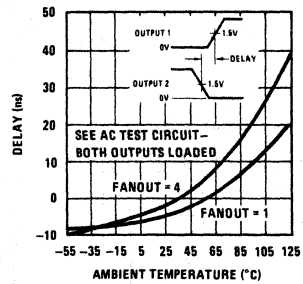
Supply Current vs Ambient Temperature



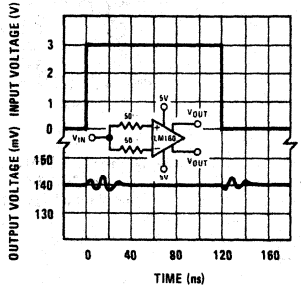
Propagation Delay vs Ambient Temperature



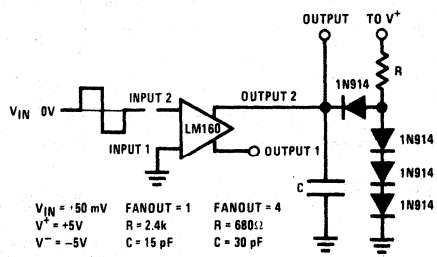
Delay of Output 1 With Respect to Output 2 vs Ambient Temperature



Common-Mode Pulse Response



AC Test Circuit



National Semiconductor

Successive Approximation Registers/Comparators

LM161/LM261/LM361 High Speed Differential Comparators

General Description

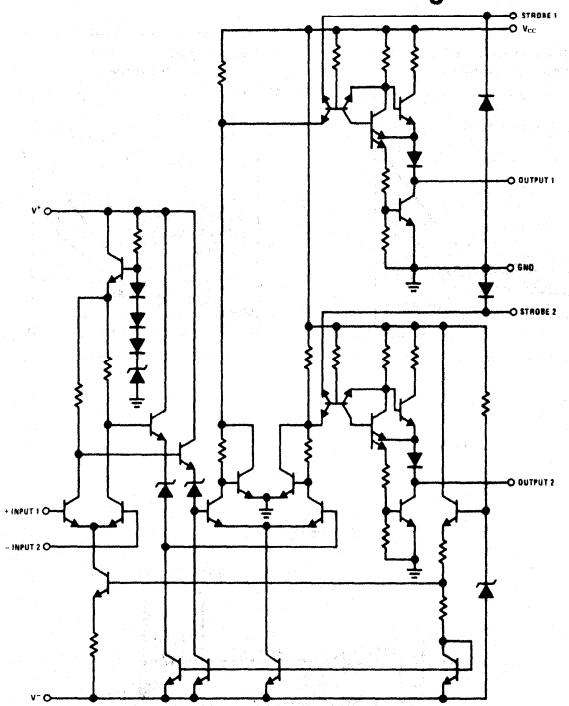
The LM161/LM261/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disc file systems.

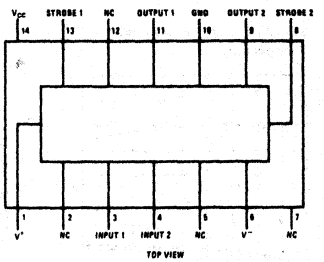
Features

- Independent strobes
- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

Schematic and Connection Diagrams



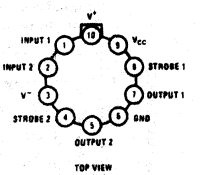
Dual-In-Line Package



Order Number LM161J, LM261J or LM361J
See NS Package J14A

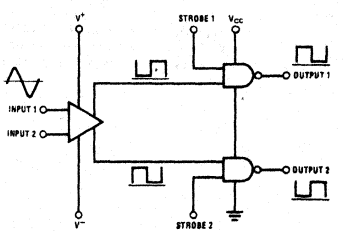
Order Number LM361N
See NS Package N14A

Metal Can Package



Order Number LM161H, LM261H or LM361H
See NS Package H10C

Logic Diagram



Absolute Maximum Ratings

Positive Supply Voltage, V^+	+16V
Negative Supply Voltage, V^-	−16V
Gate Supply Voltage, V_{CC}	+7V
Output Voltage	+7V
Differential Input Voltage	±5V
Input Common Mode Voltage	±6V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	T_{MIN} T_{MAX}
LM161	−55°C to +125°C
LM261	−25°C to +85°C
LM361	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

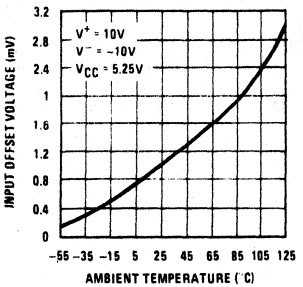
	MIN	TYP	MAX
Supply Voltage V^+			
LM161/LM261	5V		15V
LM361	5V		15V
Supply Voltage V^-			
LM161/LM261	−6V		−15V
LM361	−6V		−15V
Supply Voltage V_{CC}			
LM161/LM261	4.5V	5V	5.5V
LM361	4.75V	5V	5.25V

Electrical Characteristics ($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless noted)

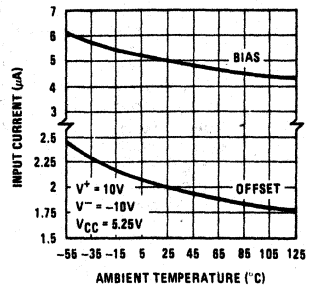
PARAMETER	CONDITIONS	LIMITS						UNITS
		LM161/LM261			LM361			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			1	3		1	5	mV
Input Bias Current	$T_A = 25°C$		5			10		µA
				20			30	µA
Input Offset Current	$T_A = 25°C$		2			2		µA
				3			5	µA
Voltage Gain	$T_A = 25°C$		3			3		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		20			20		kΩ
Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{SOURCE} = -.5$ mA	2.4	3.3		2.4	3.3		V
Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{SINK} = 6.4$ mA			.4			.4	V
Strobe Input "1" Current	$V_{CC} = 5.25V$, $V_{STROBE} = 2.4V$			200			200	µA
Strobe Input "0" Current	$V_{CC} = 5.25V$, $V_{STROBE} = .4V$			1.6			−1.6	mA
Strobe Input "0" Voltage	$V_{CC} = 4.75V$			.8			.8	V
Strobe Input "1" Voltage	$V_{CC} = 4.75V$	2			2			V
Output Short Circuit Current	$V_{CC} = 5.25V$, $V_{OUT} = 0V$	18		55	18		−55	mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			4.5				mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						5	mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $55°C < T_A < 125°C$			10				mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						10	mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			18				mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						20	mA
TRANSIENT RESPONSE	$V_{IN} = 50$ mV Overdrive							
Propagation Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		14	20		14	20	ns
Propagation Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		14	20		14	20	ns
Delay Between Output A and B	$T_A = 25°C$		2	5		2	5	ns
Strobe Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		8			8		ns
Strobe Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		8			8		ns

Typical Performance Characteristics

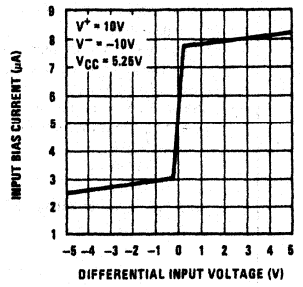
Offset Voltage



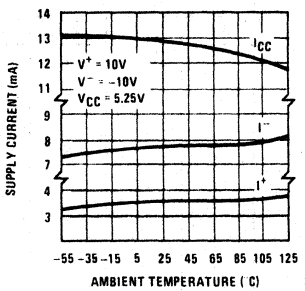
Input Currents vs Ambient Temperature



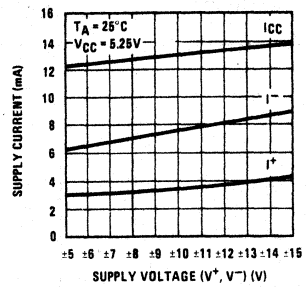
Input Characteristics



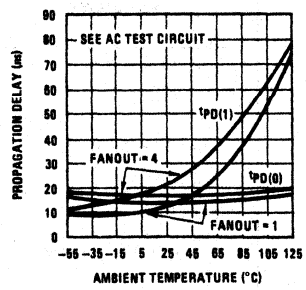
Supply Current vs Ambient Temperature



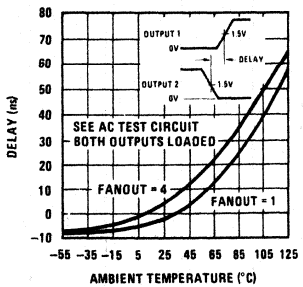
Supply Current vs Supply Voltage



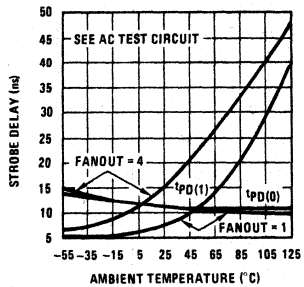
Propagation Delay vs Ambient Temperature



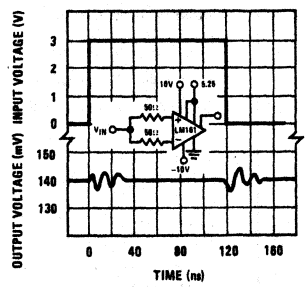
Delay of Output 1 With Respect to Output 2 vs Ambient Temperature



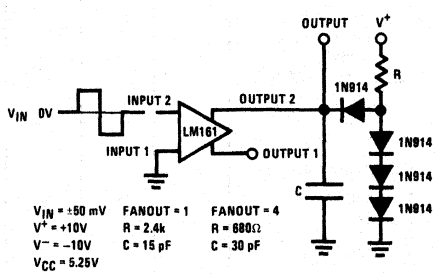
Strobe Delay vs Ambient Temperature



Common-Mode Pulse Response



AC Test Circuit



V_{IN} = ±50 mV	FANOUT = 1	FANOUT = 4
V^+ = +10V	R = 2.4k	R = 680Ω
V^- = −10V	C = 15 pF	C = 30 pF
V_{CC} = 5.25V		

National Semiconductor

Successive Approximation Registers/Comparators

LM193/LM293/LM393, LM193A/LM293A/LM393A, LM2903 Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

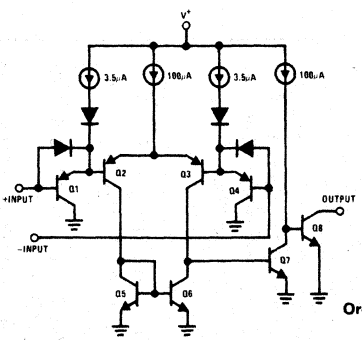
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

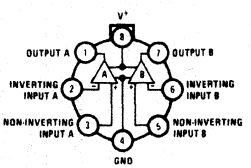
Features

- Wide single supply
  Voltage range 2.0 V_{DC} to 36 V_{DC}
  or dual supplies ±1.0 V_{DC} to ±18 V_{DC}
- Very low supply current drain (0.8 mA)—independent of supply voltage (1.0 mW/comparator at 5.0 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams

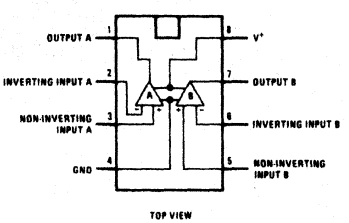


Metal Can Package



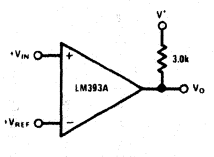
Order Number LM193H, LM193AH, LM293H, LM293AH, LM393H or LM393AH
See NS Package H08C

Dual-In-Line Package

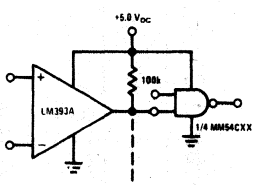


Order Number LM393N, LM393AN or LM2903N
See NS Package N08B

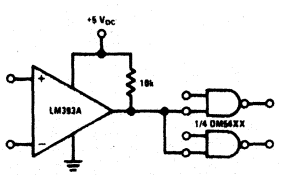
Typical Applications ($V^+ = 5.0\ V_{DC}$)



Basic Comparator



Driving CMOS



Driving TTL

Absolute Maximum Ratings

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Molded DIP	570 mW
Metal Can	830 mW
Output Short-Circuit to Ground, (Note 2)	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$), (Note 3)	50 mA
Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics ($V^+ = 5\ V_{DC}$) (Note 4)

PARAMETER	CONDITIONS	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 9)		±1.0	±2.0		±1.0	±2.0		±1.0	±5.0		±1.0	±5.0		±2.0	±7.0	mV_{DC}
Input Bias Current	I_{IN+} or I_{IN-} with Output In Linear Range, $T_A = 25°C$, (Note 5)		25	100		25	250		25	100		25	250		25	250	nA_{DC}
Input Offset Current	$I_{IN+} - I_{IN-}$, $T_A = 25°C$		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5.0	±50	nA_{DC}
Input Common-Mode Voltage Range	$T_A = 25°C$, (Note 6)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$ on All Comparators, $T_A = 25°C$		0.4	1		0.4	1		0.4	1		0.4	1		0.4	1.0	mA_{DC}
	$R_L = \infty$ on All Amps, $V^+ = 30\ V_{DC}$		1	2.5		1	2.5			2.5			2.5		1	2.5	mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, $T_A = 25°C$, $V^+ = 15\ V_{DC}$ (To Support Large V_O Swing)	50	200		50	200		50	200		50	200		25	100		V/μV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$ $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300			300			300			300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 7)		1.3			1.3			1.3			1.3			1.5		μs
Output Sink Current	$V_{IN-} \geq 1\ V_{DC}$, $V_{IN+} = 0$, $V_O \leq 1.5\ V_{DC}$, $T_A = 25°C$	6.0	16		6.0	16		6.0	16		6.0	16		6	16		mA_{DC}
Saturation Voltage	$V_{IN-} \geq 1\ V_{DC}$, $V_{IN+} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = 25°C$		250	400		250	400		250	400		250	400			400	mV_{DC}
Output Leakage Current	$V_{IN-} = 0$, $V_{IN+} \geq 1\ V_{DC}$, $V_O = 5\ V_{DC}$, $T_A = 25°C$		0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 9)			4.0			4.0			9			9		9	15	mV_{DC}
Input Offset Current	$I_{IN+} - I_{IN-}$			±100			±150			±100			±150		50	200	nA_{DC}
Input Bias Current	I_{IN+} or I_{IN-} with Output in Linear Range			300			400			300			400		200	500	nA_{DC}
Input Common-Mode Voltage Range		0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		V^+-20	V_{DC}
Saturation Voltage	$V_{IN-} \geq 1\ V_{DC}$, $V_{IN+} = 0$, $I_{SINK} \leq 4$ mA,			700			700			700			700		400	700	mV_{DC}
Output Leakage Current	$V_{IN-} = 0$, $V_{IN+} \geq 1\ V_{DC}$, $V_O = 30\ V_{DC}$,			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep All V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if Used), (Note 8)			V^+			V^+			V^+			V^+			V^+	V_{DC}

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$.

Note 4: These specifications apply for $V^+ = 5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5$V, but either or both inputs can go to $30\ V_{DC}$ without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

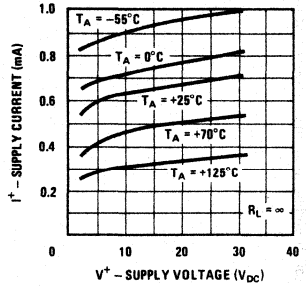
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$).

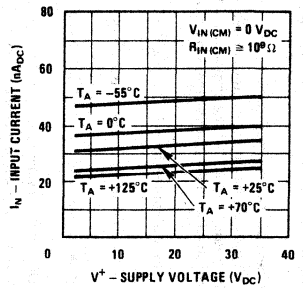
Note 10: For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

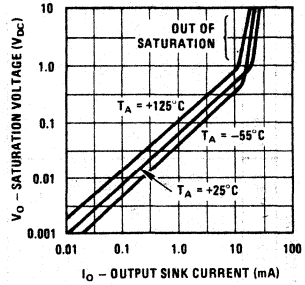
Supply Current



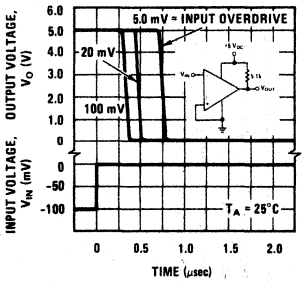
Input Current



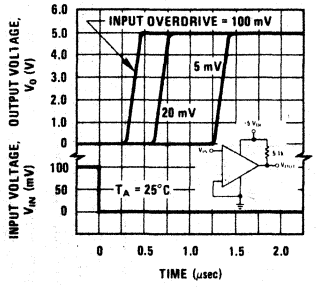
Output Saturation Voltage



Response Time for Various Input Overdrives – Negative Transition

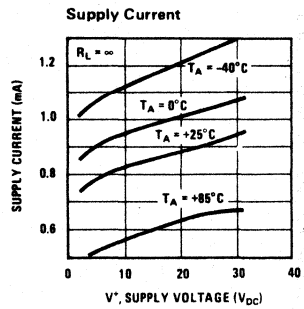


Response Time for Various Input Overdrives – Positive Transition

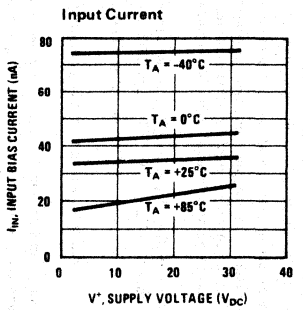


Typical Performance Characteristics LM2903

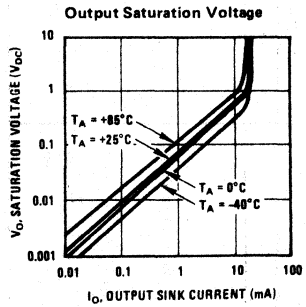
Supply Current



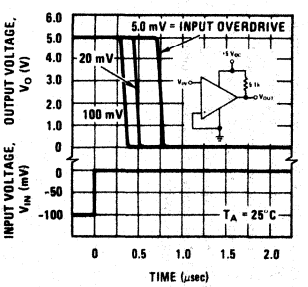
Input Current



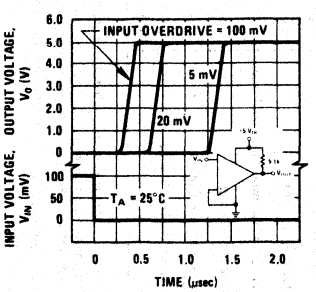
Output Saturation Voltage



Response Time for Various Input Overdrives–Negative Transition



Response Time for Various Input Overdrives–Positive Transition



Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

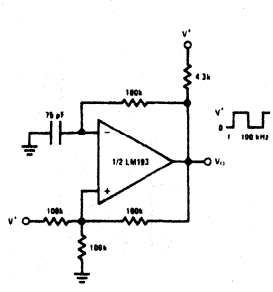
The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

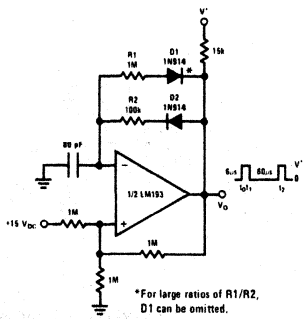
The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

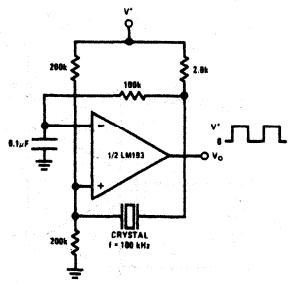
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



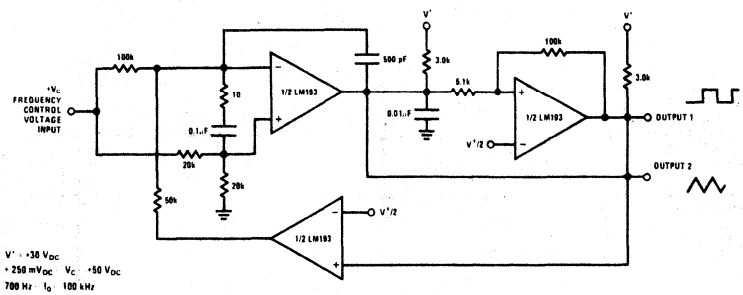
Squarewave Oscillator



Pulse Generator

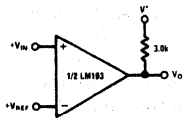


Crystal Controlled Oscillator

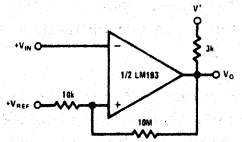


Two-Decade High-Frequency VCO

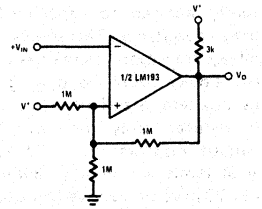
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



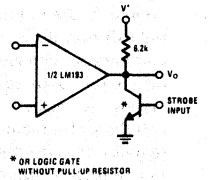
Basic Comparator



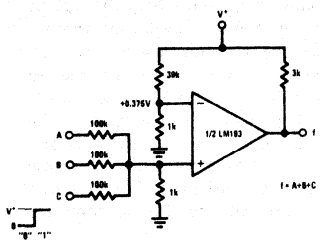
Non-Inverting Comparator with Hysteresis



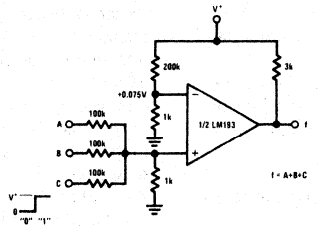
Inverting Comparator with Hysteresis



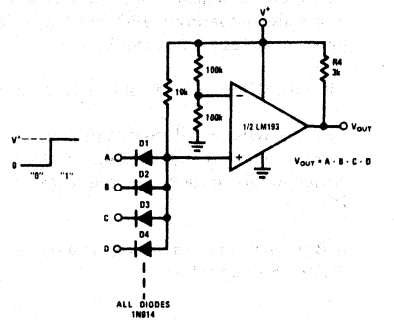
Output Strobing



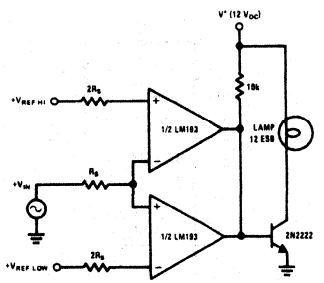
AND Gate



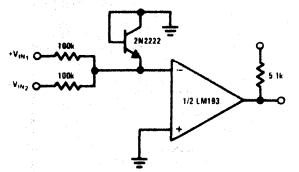
OR Gate



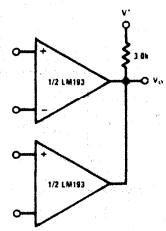
Large Fan-in AND Gate



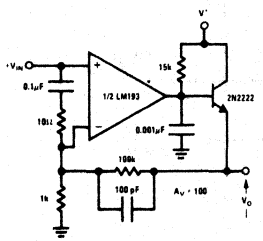
Limit Comparator



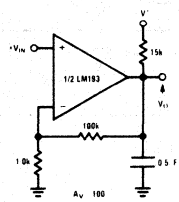
Comparing Input Voltages of Opposite Polarity



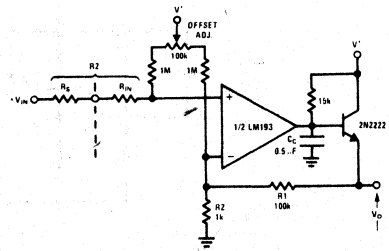
ORing the Outputs



Improved Op Amp

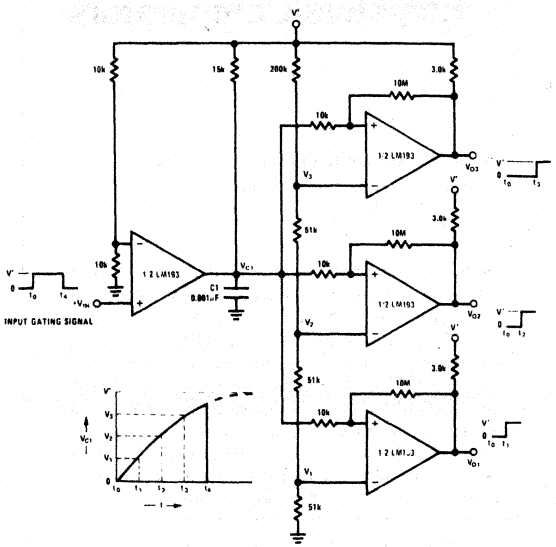


Low Frequency Op Amp

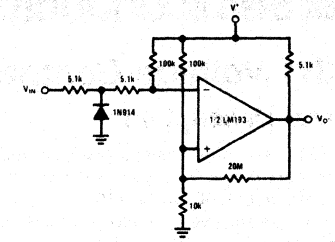


Low Frequency Op Amp with Offset Adjust

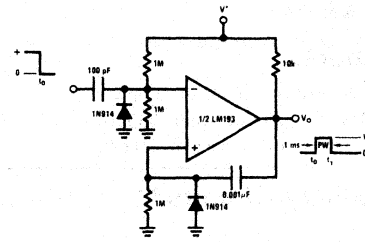
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



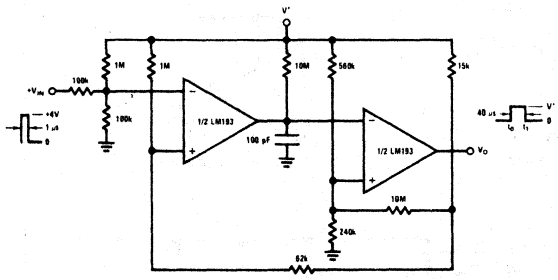
Time Delay Generator



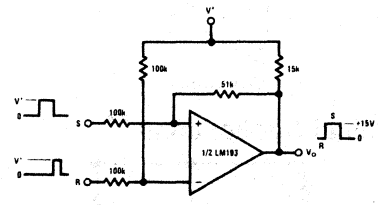
Zero Crossing Detector (Single Power Supply)



One-Shot Multivibrator

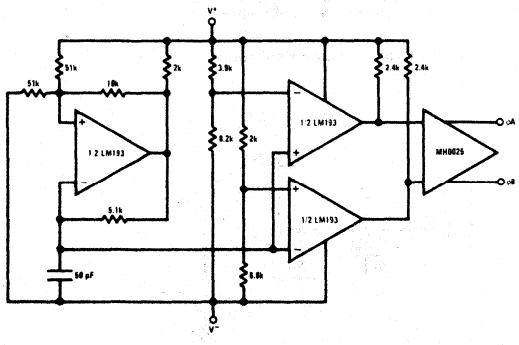


One-Shot Multivibrator with Input Lock Out

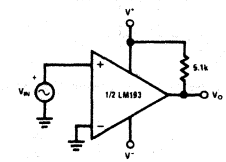


Bi-Stable Multivibrator

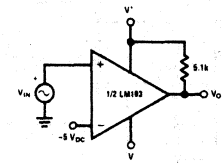
Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)



MOS Clock Driver



Zero Crossing Detector



Comparator With a Negative Reference

13

National Semiconductor

Successive Approximation Registers/Comparators

LM311 Voltage Comparator

General Description

The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

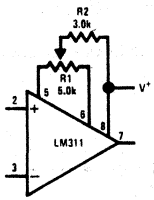
Features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

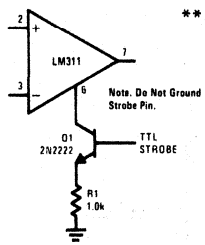
Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C. See the "application hints" of the LM311 for application help.

Auxiliary Circuits**

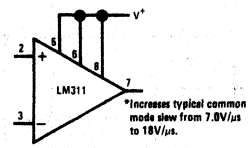
**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.



Offset Balancing

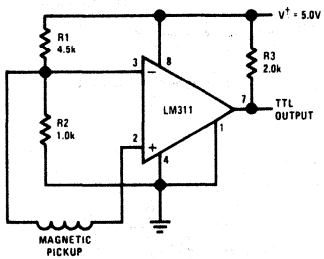


Strobing

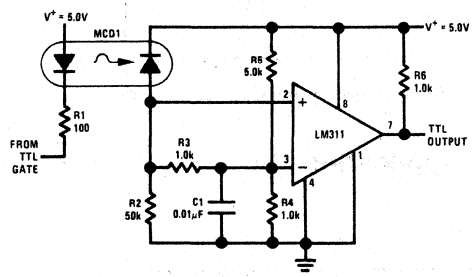


Increasing Input Stage Current*

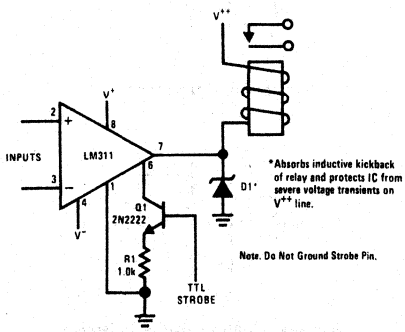
Typical Applications**



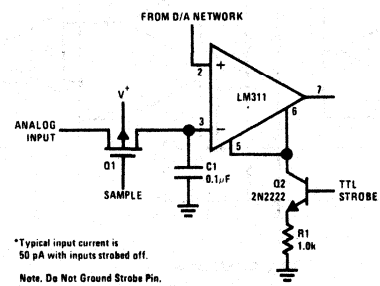
Detector for Magnetic Transducer



Digital Transmission Isolator



Relay Driver with Strobe



Strobing off Both Input* and Output Stages

Absolute Maximum Ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Voltage at Strobe Pin	V^+−5V

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8,−14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and the Ground pin at ground, and $0°C < T_A < +70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

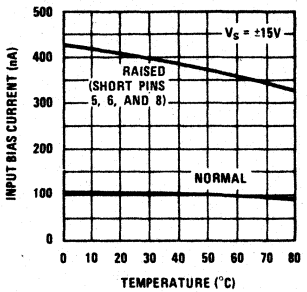
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

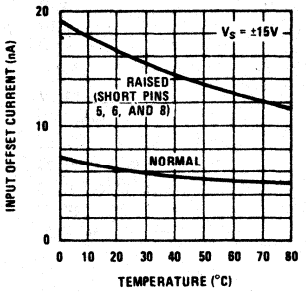
Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Typical Performance Characteristics

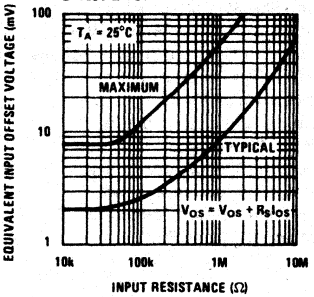
Input Bias Current



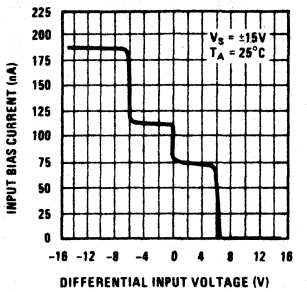
Input Offset Current



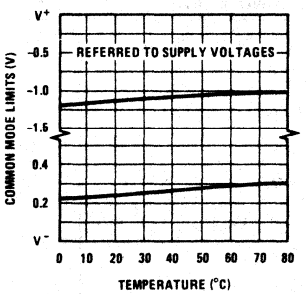
Offset Error



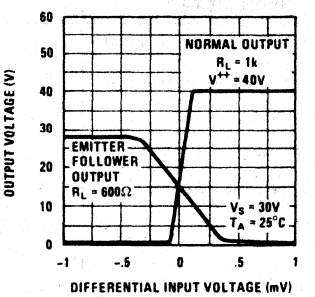
Input Characteristics



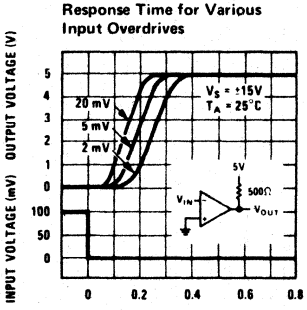
Common Mode Limits



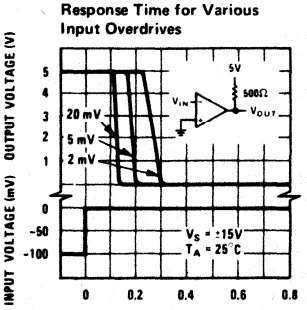
Transfer Function



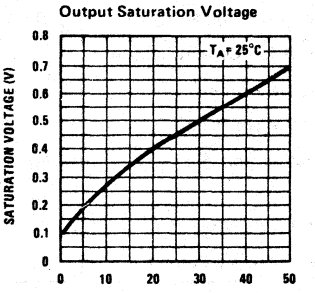
Response Time for Various Input Overdrives



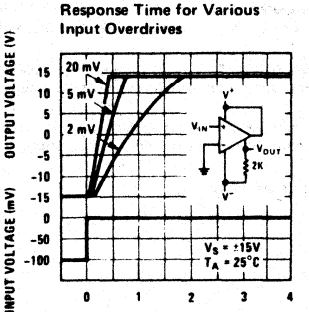
Response Time for Various Input Overdrives



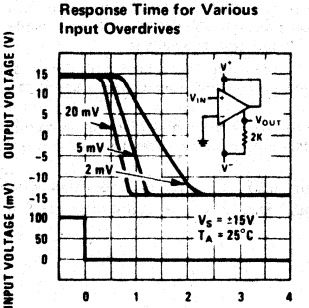
Output Saturation Voltage



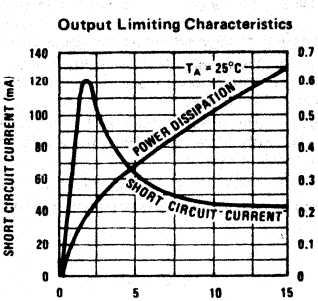
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

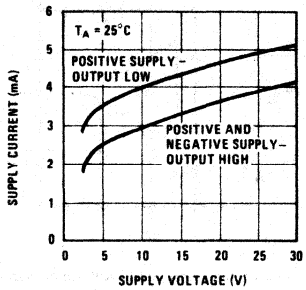


Output Limiting Characteristics

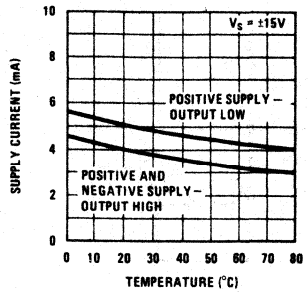


Typical Performance Characteristics (Continued)

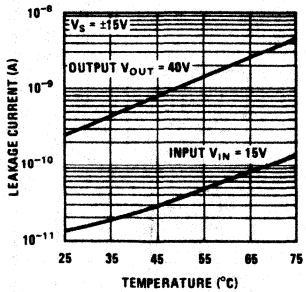
Supply Current



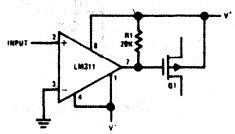
Supply Current



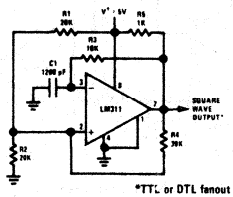
Leakage Currents



Typical Applications

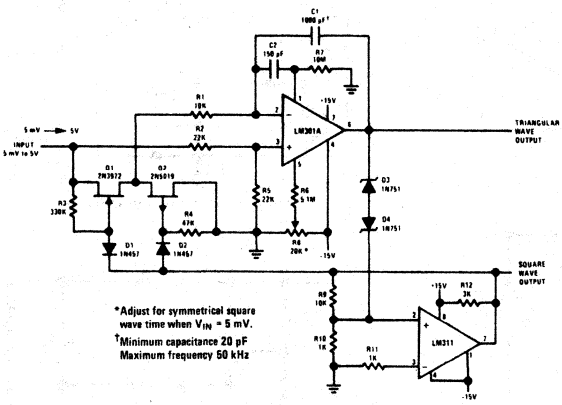


Zero Crossing Detector Driving MOS Switch



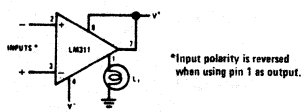
*TTL or DTL fanout of two.

100 kHz Free Running Multivibrator



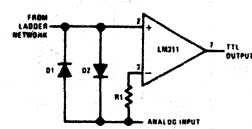
*Adjust for symmetrical square wave time when V_{IN} = 5 mV.
†Minimum capacitance 20 pF
Maximum frequency 50 kHz

10 Hz to 10 kHz Voltage Controlled Oscillator

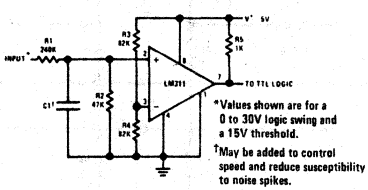


*Input polarity is reversed when using pin 1 as output.

Driving Ground-Referred Load

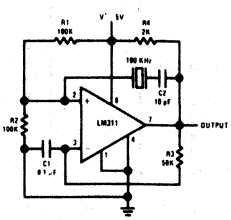


Using Clamp Diodes to Improve Response

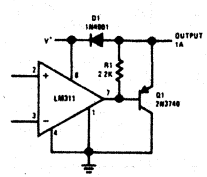


*Values shown are for a 0 to 30V logic swing and a 15V threshold.
†May be added to control speed and reduce susceptibility to noise spikes.

TTL Interface with High Level Logic

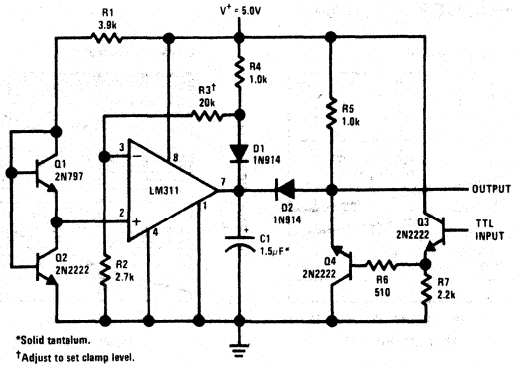


Crystal Oscillator



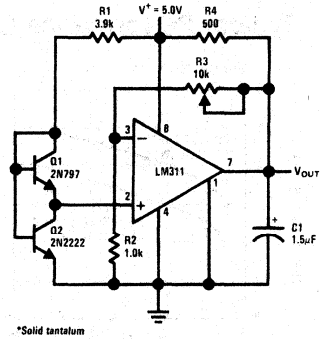
Comparator and Solenoid Driver

Typical Applications (Continued)



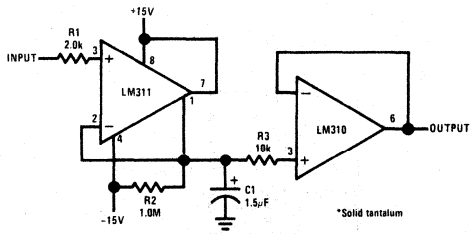
*Solid tantalum.
†Adjust to set clamp level.

Precision Squarer

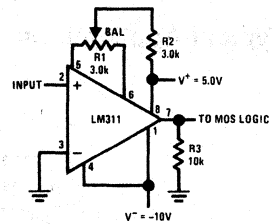


*Solid tantalum

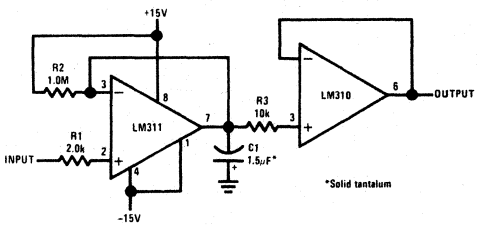
Low Voltage Adjustable Reference Supply



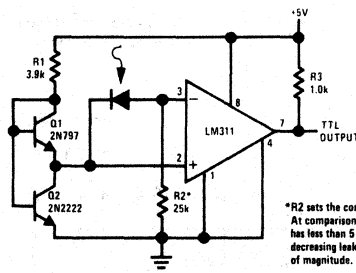
Positive Peak Detector



Zero Crossing Detector driving MOS logic

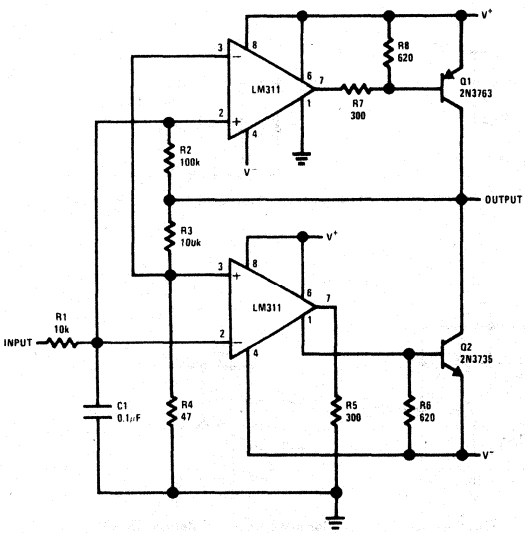


Negative Peak Detector

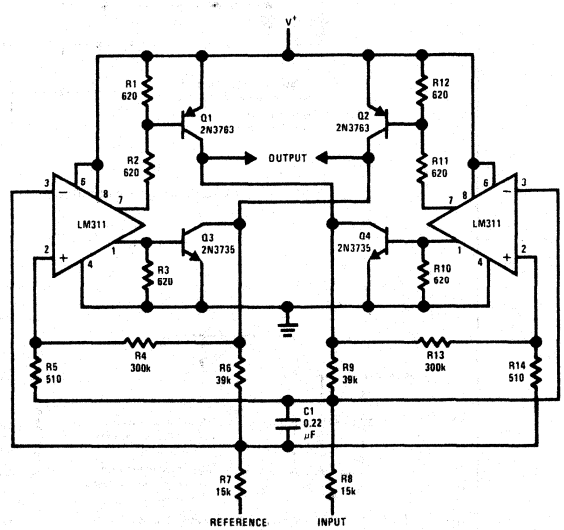


*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

Precision Photodiode Comparator

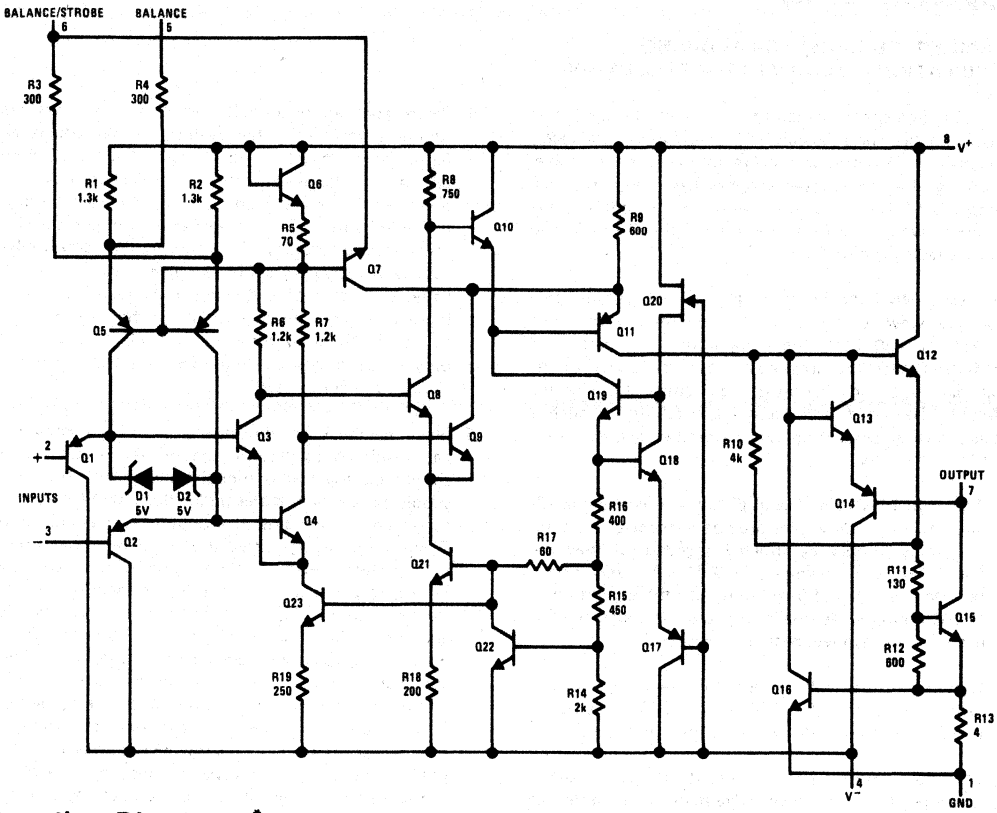


Switching Power Amplifier



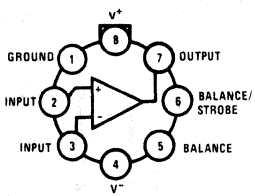
Switching Power Amplifier

Schematic Diagram



Connection Diagrams *

Metal Can Package

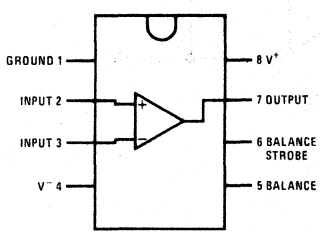


NOTE: Pin 4 connected to case.

TOP VIEW

Order Number LM311H
See NS Package H08C

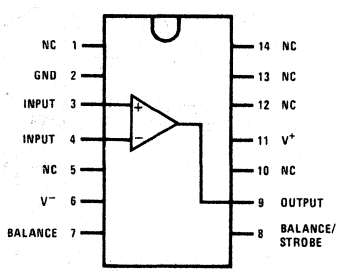
Dual-In-Line Package



TOP VIEW

Order Number LM311N
See NS Package N08B
Order Number LM311J-8
See NS Package J08A

Dual-In-Line Package



Note: Pin 6 connected to bottom of package.

Order Number LM311N-14
See NS Package N14A
Order Number LM311J
See NS Package J14A

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Application Hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

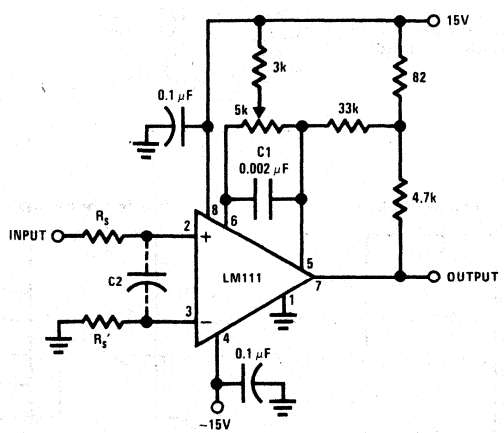
1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.

2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.

3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.

4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

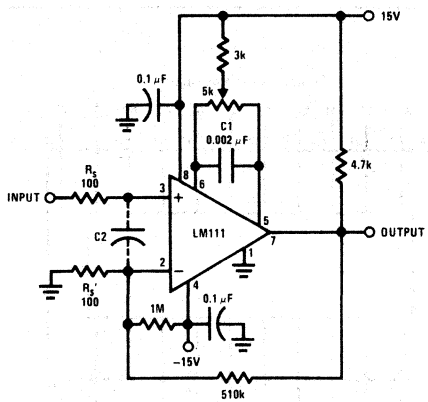
FIGURE 1. Improved Positive Feedback

Application Hints (Continued)

6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2,* the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.

7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.

8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 2. Conventional Positive Feedback

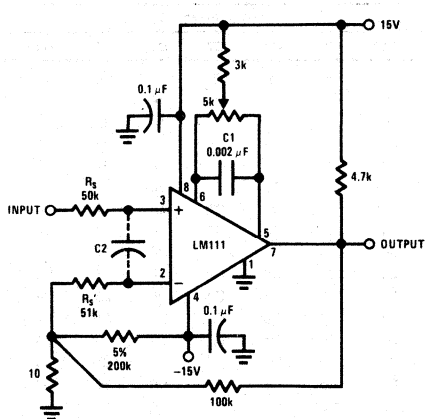


FIGURE 3. Positive Feedback With High Source Resistance

National Semiconductor

Successive Approximation Registers/Comparators

MM54C905/MM74C905 12-Bit Successive Approximation Register

General Description

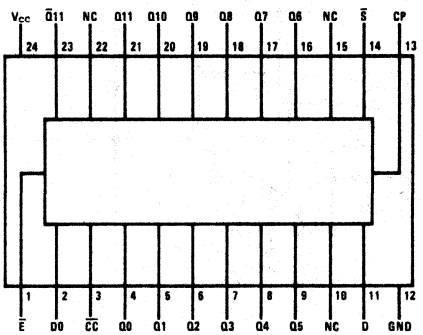
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

Connection Diagram

Dual-In-Line Package



Order Number MM54C905D or MM74C905D
See NS Package D24A

Order Number MM74C905N
See NS Package N18A

Truth Table

TIME	INPUTS			OUTPUTS													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C905	−55°C to +125°C
MM74C905	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C905	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C905	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C905	V_{CC} = 4.5V			0.8	V
MM74C905	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C905	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C905	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C905	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C905	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA
Q11–Q0 Outputs	V_{CC} = 10V ±5%				
R_{SOURCE}	V_{OUT} = V_{CC} − 0.3V, T_A = 25°C	150		350	Ω
R_{SINK}	V_{CC} = 10V ±5%, V_{OUT} = 0.3V, T_A = 25°C	80		230	Ω

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From Clock Input To Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$		200	350	ns
	$V_{CC} = 10V$		80	150	ns
Propagation Delay Time From Clock Input To D_O ($t_{pd(D_O)}$)	$V_{CC} = 5.0V$		180	325	ns
	$V_{CC} = 10V$		70	125	ns
Propagation Delay Time From Register Enable ($\overline{E}$) To Output (Q11) ($t_{pd(\overline{E})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	150	ns
Propagation Delay Time From Clock To $\overline{CC}$ ($t_{pd(\overline{CC})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	0.50	ns
Data Input Set-Up Time (t_{DS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Start Input Set-Up Time (t_{SS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Minimum Clock Pulse Width (t_{PWL}, t_{PWH})	$V_{CC} = 5.0V$	250	125		ns
	$V_{CC} = 10V$	100	50		ns
Maximum Clock Rise and Fall Time (t_r, t_f)	$V_{CC} = 5.0V$			15	μs
	$V_{CC} = 10V$			5	μs
Maximum Clock Frequency (f_{MAX})	$V_{CC} = 5.0V$	2	4		MHz
	$V_{CC} = 10V$	5	10		MHz
Clock Input Capacitance (C_{CLK})	Clock Input (Note 2)		10		pF
Input Capacitance (C_{IN})	Any Other Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	(Note 3)		100		pF

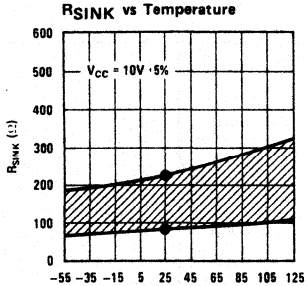
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

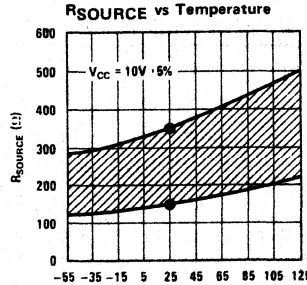
Typical Performance Characteristics

R_{SINK} vs Temperature



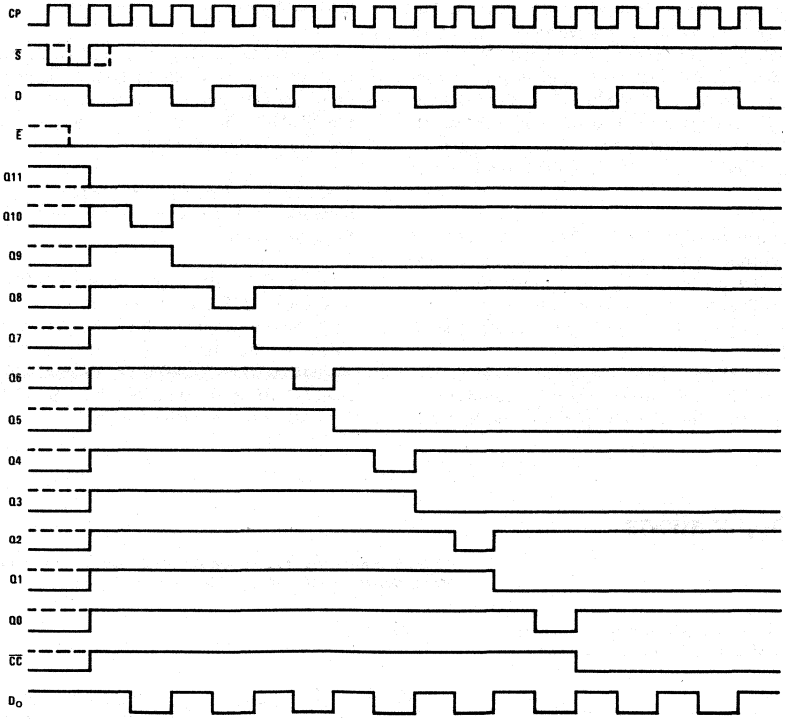
● These points are guaranteed by automatic testing.

R_{SOURCE} vs Temperature

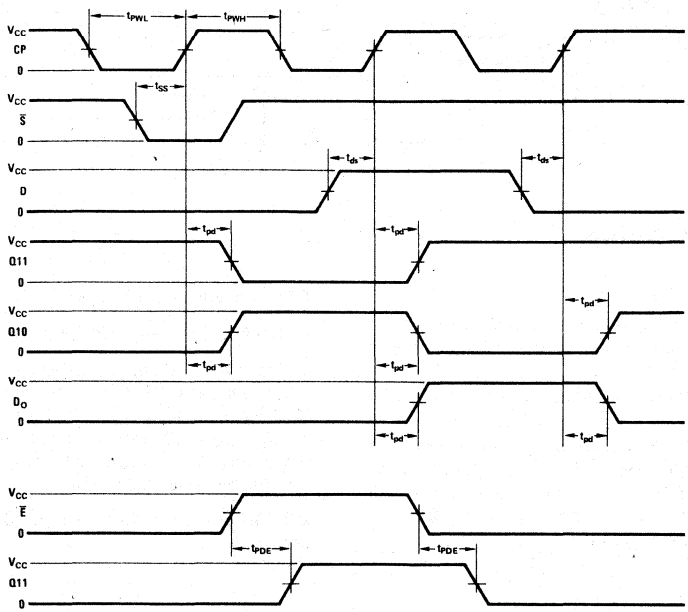


● These points are guaranteed by automatic testing.

Timing Diagram



Switching Time Waveforms



USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +1/2 LSB and using the complement of the MSB Q11 as the sign bit.

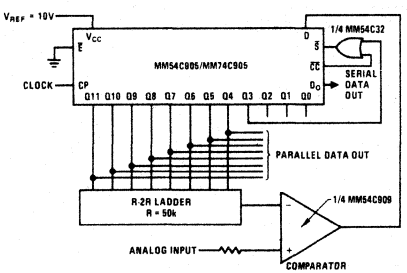
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

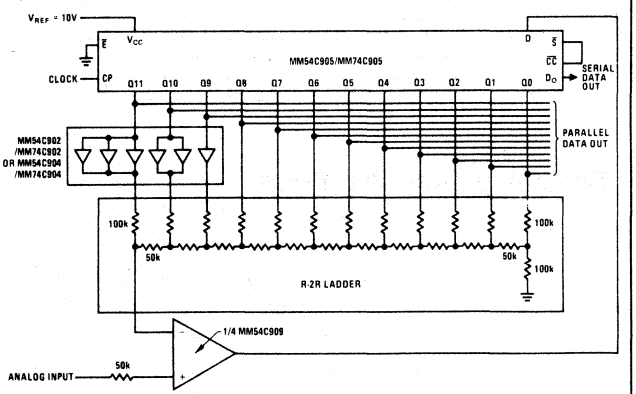
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

Typical Applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



Definition of Terms

CP: Register *clock* input.

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q11}$: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

Section 14

Voltage References

14

Section Contents

National Semiconductor

LH0070 Series Precision BCD Buffered Reference
LH0071 Series Precision Binary Buffered Reference

General Description

The LH0070 and LH0071 are precision, three terminal, voltage references consisting of a temperature compensated zener diode driven by a current regulator and a buffer amplifier. The devices provide an accurate reference that is virtually independent of input voltage, load current, temperature and time. The LH0070 has a 10.000V nominal output to provide equal step sizes in BCD applications. The LH0071 has a 10.240V nominal output to provide equal step sizes in binary applications.

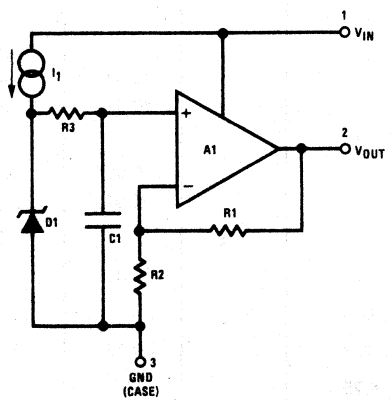
The output voltage is established by trimming ultra-stable, low temperature drift, thin film resistors under actual operating circuit conditions. The devices are short-circuit proof in both the current sourcing and sinking directions.

The LH0070 and LH0071 series combine excellent long term stability, ease of application, and low cost, making them ideal choices as reference voltages in precision D to A and A to D systems.

Features

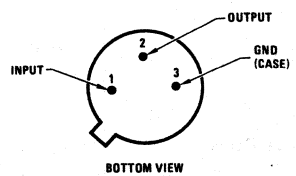
- Accurate output voltage
  - LH0070 — 10V ±0.01%
  - LH0071 — 10.24V ±0.01%
- Single supply operation — 12.5V to 40V
- Low output impedance — 0.1Ω
- Excellent line regulation — 0.1 mV/V
- Low zener noise — 100 μVp-p
- 3-lead TO-5 (pin compatible with the LM109)
- Short circuit proof
- Low standby current — 3 mA

Equivalent Schematic



Connection Diagram

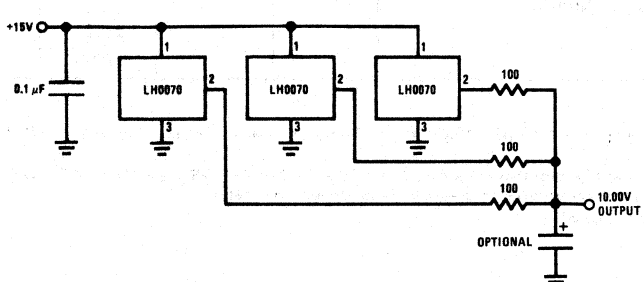
TO-39 Metal Can Package



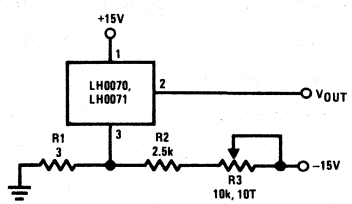
BOTTOM VIEW

Order Number LH0070-1H, LH0071-1H, LH0070-2H or LH0071-2H
See NS Package H03A

Typical Applications



Statistical Voltage Standard



*Note. The output of the LH0070 and LH0071 may be adjusted to a precise voltage by using the above circuit since the supply current of the devices is relatively small and constant with temperature and input voltage. For the circuit shown, supply sensitivities are degraded slightly to 0.01%/V change in V_{OUT} for changes in V_{IN} and V^-

An additional temperature drift of 0.0001%/°C is added due to the variation of supply current with temperature of the LH0070 and LH0071. Sensitivity to the value of R1, R2 and R3 is less than 0.001%/%.

***Output Voltage Fine Adjustment**

Absolute Maximum Ratings

Supply Voltage	40V
Power Dissipation (See Curve)	600 mW
Short Circuit Duration	Continuous
Output Current	±20 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_A = 25°C$				
LH0070			10.000		V
LH0071			10.240		V
Output Accuracy	$T_A = 25°C$				
−0, −1			±0.03	±0.1	%
−2			±0.02	±0.05	%
Output Accuracy					
−0, −1				±0.3	%
−2				±0.2	%
Output Voltage Change With Temperature	(Note 2)				
−0				± 0.2	%
−1			±0.02	± 0.1	%
−2			±0.01	±0.04	%
Line Regulation	$13V \leq V_{IN} \leq 33V$, $T_C = 25°C$				
−0, −1			0.02	0.1	%
−2			0.01	0.03	%
Input Voltage Range		12.5		40	V
Load Regulation	$0\ mA \leq I_{OUT} \leq 5\ mA$		0.01	0.03	%
Quiescent Current	$13V \leq V_{IN} \leq 33V$, $I_{OUT} = 0\ mA$	2	3	5	mA
Change In Quiescent Current	ΔV_{IN} = 20V From 13V To 33V		0.75	1.5	mA
Output Noise Voltage	BW = 0.1 Hz To 10 Hz, $T_A = 25°C$		20		μVp-p
Ripple Rejection	f = 120 Hz		0.01		%/Vp-p
Output Resistance			0.2	1	Ω
Long Term Stability	$T_A = 25°C$, (Note 3)				
−0, −1				±0.2	%/yr.
−2				±0.05	%/yr.

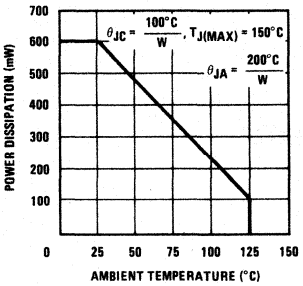
Note 1: Unless otherwise specified, these specifications apply for V_{IN} = 15.0V, R_L = 10 kΩ, and over the temperature range of $-55°C \leq T_A \leq +125°C$.

Note 2: This specification is the difference in output voltage measured at $T_A = 85°C$ and $T_A = 25°C$ or $T_A = 25°C$ and $T_A = -25°C$ with readings taken after test chamber and device-under-test stabilization at temperature using a suitable precision voltmeter.

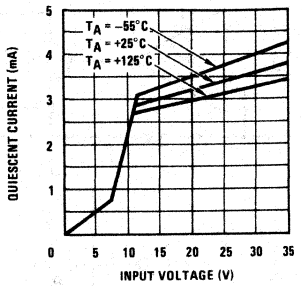
Note 3: This parameter is guaranteed by design and not tested.

Typical Performance Characteristics

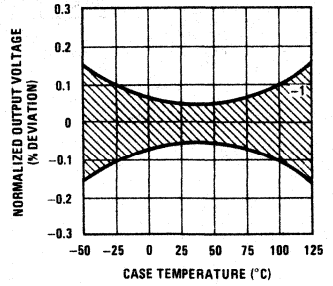
Maximum Power Dissipation



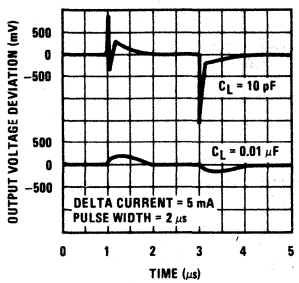
Quiescent Current vs Input Voltage



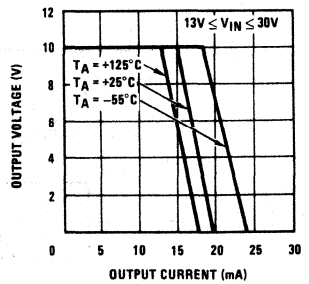
Normalized Output Voltage vs Temperature



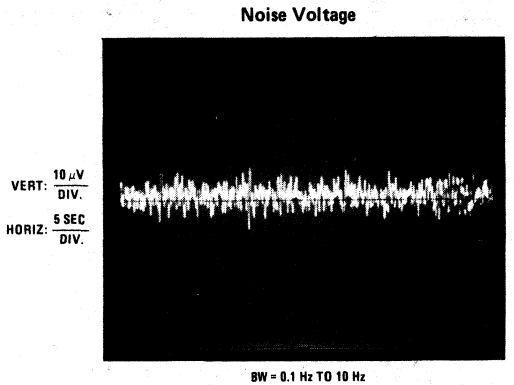
Step Load Response



Output Short Circuit Characteristics

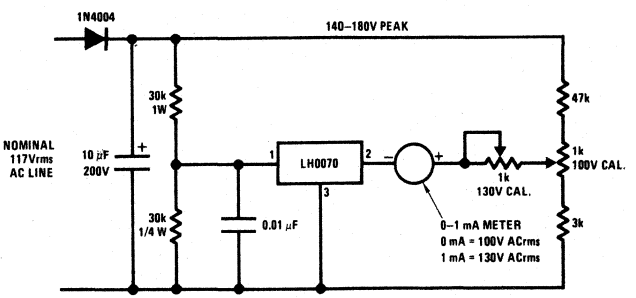


Noise Voltage



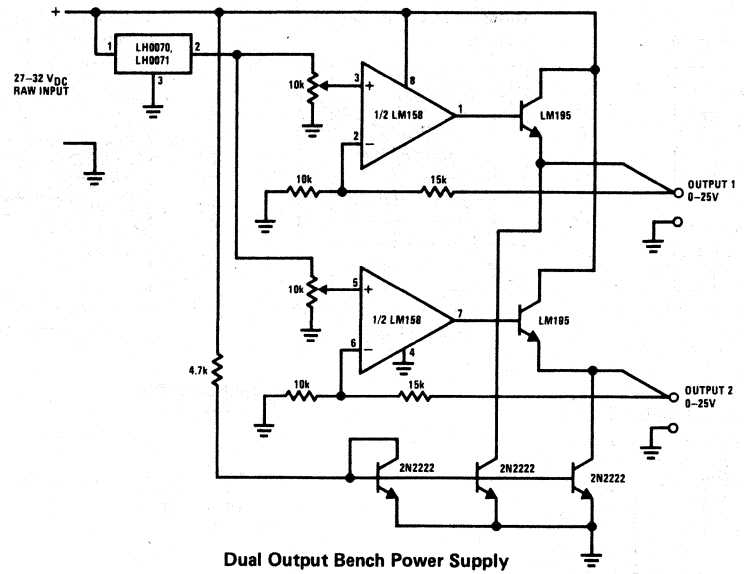
BW = 0.1 Hz TO 10 Hz

Typical Applications (Continued)

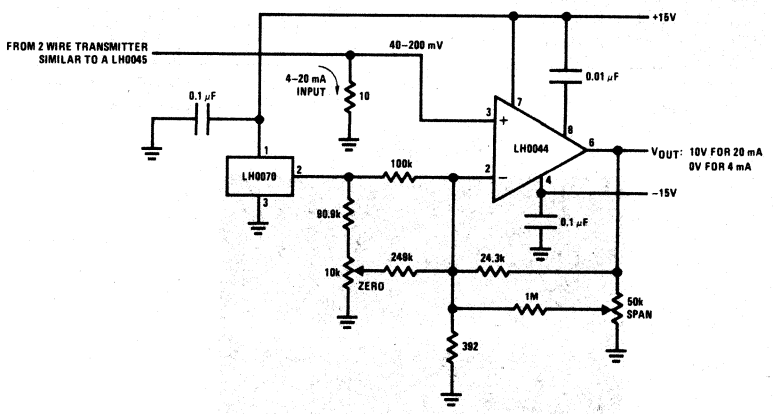


Expanded Scale AC Voltmeter

Typical Applications (Continued)



Dual Output Bench Power Supply



Precision Process Control Interface

National Semiconductor

LH0075 Positive Precision Programmable Regulator

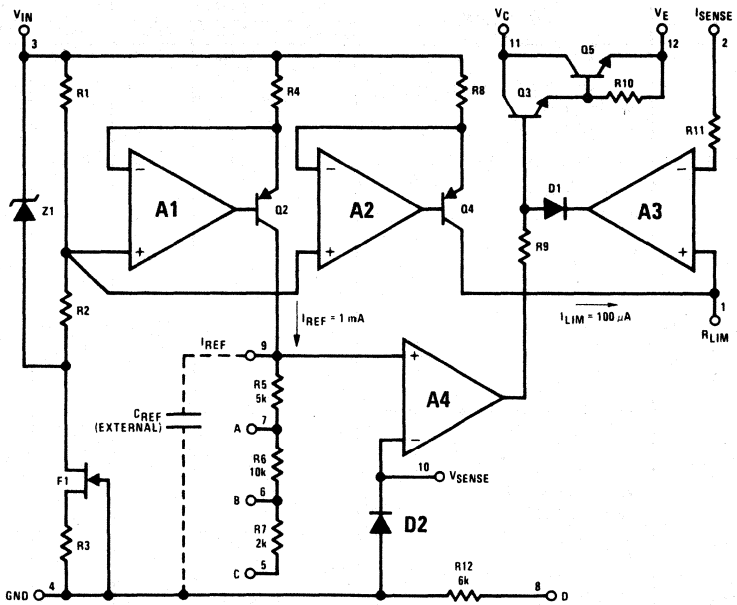
General Description

The LH0075 is a precision programmable regulator for positive voltages. Regulated output voltages from 0 to 27V may be obtained using one external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (5V, 6V, 10V, 12V and 15V). The output current limit is adjustable from 0 to 200 mA using two external resistors. These features provide an inventory of precision regulated values in one package.

Features

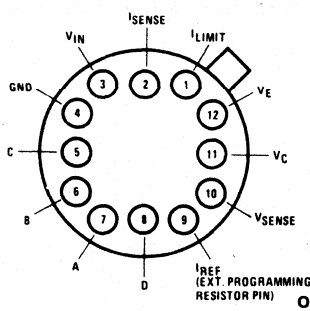
- Output adjustable to 0V
- Line regulation typically 0.008%/V
- Load regulation typically 0.075%
- Remote voltage sensing
- Ripple rejection of 80 dB
- Adjustable precision current limit
- Output currents to 200 mA
- Popular voltages available without external resistors

Schematic Diagram



Connection Diagram

TO-8 Metal Can Package

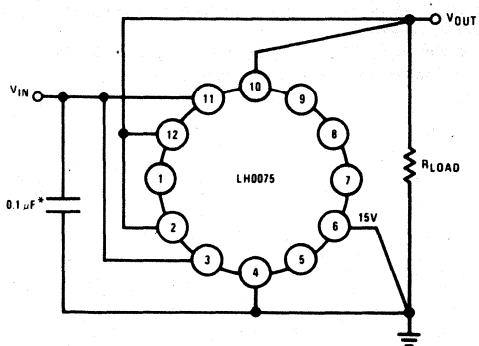


Case is electrically isolated

Order Number
LH0075G
LH0075CG
See Package H12B

Typical Applications

Precision 15V Reference Supply without Current Limit



*Needed if device is far from filter capacitors

Absolute Maximum Ratings

Input Voltage	32V
Output Voltage	27V
Output Current	200 mA
Power Dissipation	See Curve
Operating Temperature Range	T_{MIN} T_{MAX}
LH0075	−55°C to +125°C
LH0075C	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics Unless otherwise specified conditions are for $T_{MIN} \leq T_A \leq T_{MAX}$

PARAMETER	CONDITIONS	LH0075			LH0075C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	T_A = 25°C		0.008	0.02		0.008	0.04	%/V
Load Regulation	T_A = 25°C, 1 mA < I_{LOAD} < 200 mA							
	$V_{OUT} \leq$ 5V		2.5	7.5		2.5	15	mV
	$V_{OUT} \geq$ 5V		0.055	0.15		0.055	0.3	%
Reference Current (I_{REF})	T_A = 25°C, V_{IN} = 15V	0.998	1.000	1.002	0.995	1.00	1.005	mA
Load Regulation	1 mA < I_{LOAD} < 200 mA							
	$V_{OUT} \leq$ 5V		4	15		4	25	mV
	$V_{OUT} \geq$ 5V		0.075	0.3		0.075	0.5	%
Reference Current Drift ($\Delta I_{REF}/\Delta$Temp)	V_{IN} = 15V		−0.0065			−0.0065		%/°C
Minimum Load Current(I_{LIM})	(Note 1)	98	100	102	95	100	105	μA
Output Voltage Range		0		27	0		27	V
Minimum Input Voltage		8			8			V
Input–Output Differential Voltage	T_A = 25°C, 1 mA < I_{LOAD} < 200 mA		3.0	3.2		3.0	3.5	V
Quiescent Supply Current			6	6.5		6.5	8	mA
Ripple Rejection	V_{OUT} = 5V, f = 120 Hz		65			65		dB
	C_{REF} = 2.2 μF		80			80		dB
Initial Output Voltage Tolerance	(Note 2)		±0.1	±0.5		±0.1	±1.0	%
Output Voltage Change with Temperature ($\Delta V_{OUT}/\Delta$Temp)	(Note 3)		0.003			0.003		%/°C

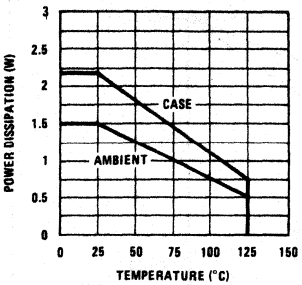
Note 1: Minimum load current is established by I_{LIM}, the current from Q4. (See schematic). I_{LIM} goes directly to the output if the current limit feature is used.

Note 2: For V_{IN} = 15V and V_{OUT} obtained by using R5, R6, R7 and R12 individually.

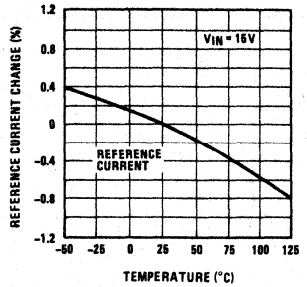
Note 3: Total change over specified temperature range.

Typical Performance Characteristics

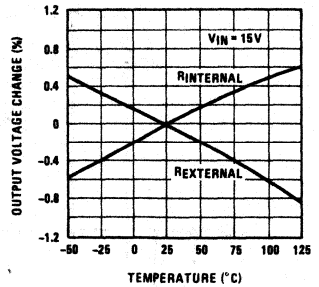
Maximum Power Dissipation



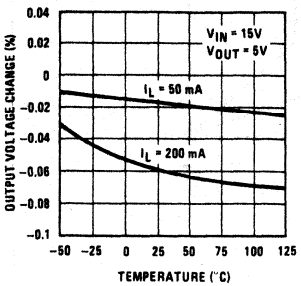
Reference Current Change with Temperature (Normalized)



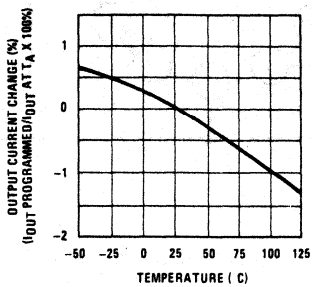
Temperature Stability



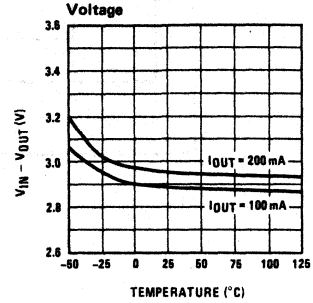
Output Voltage Change with Temperature (Normalized)



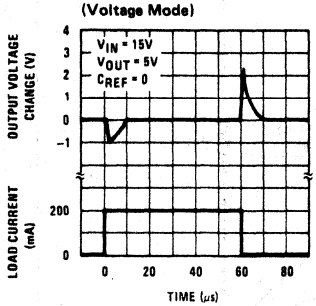
Current Limit



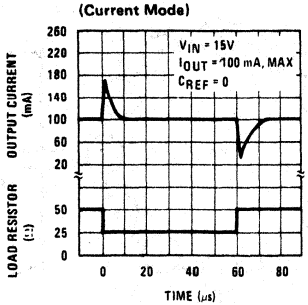
Input–Output Differential Voltage



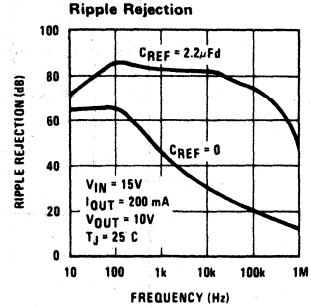
Load Transient Response (Voltage Mode)



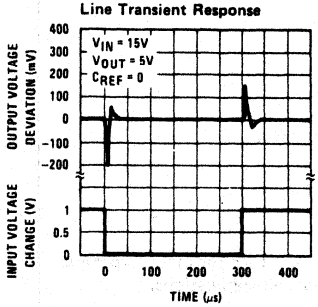
Load Transient Response (Current Mode)



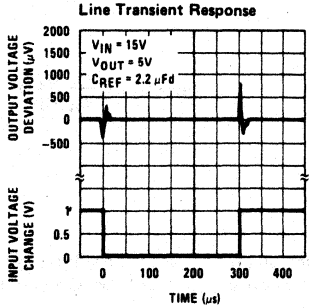
Ripple Rejection



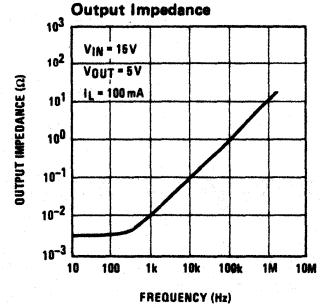
Line Transient Response



Line Transient Response

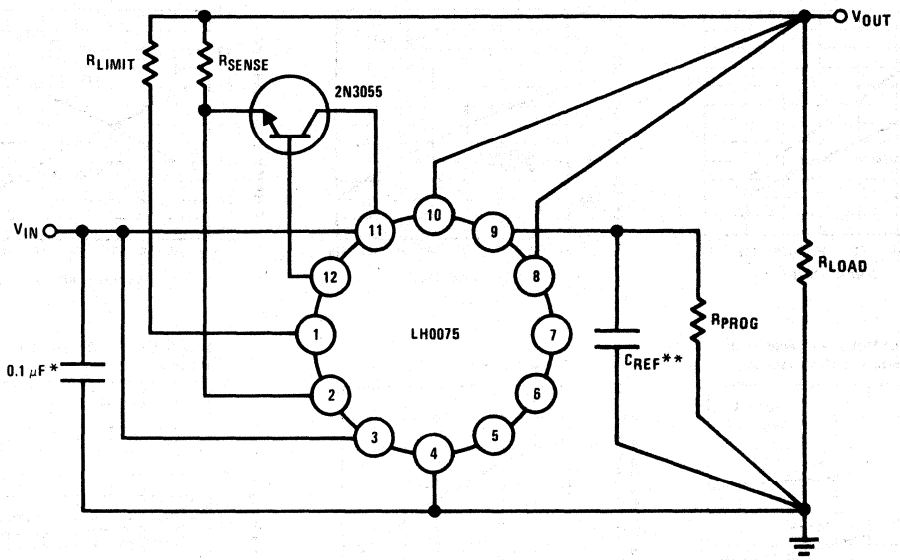


Output Impedance

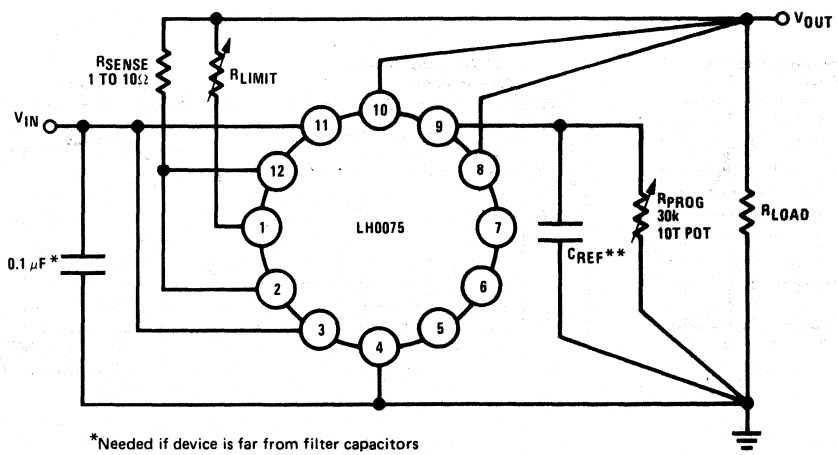


Typical Applications (Continued)

2A Regulator with Current Limit



Variable Voltage Reference with Current Limit



*Needed if device is far from filter capacitors
**Optional—improves transient response

$$R_{PROG} = \frac{V_{OUT\ Desired}}{1\ mA} \qquad I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\,\mu A$$

$I_{OUT} \leq 200$ mA

Applications Information

The LH0075 does not require capacitors for stable operation, but an input bypass is recommended if device is far from filter capacitors. A 0.1 μF for input bypassing should be adequate for almost all applications.

Applications Information (Continued)

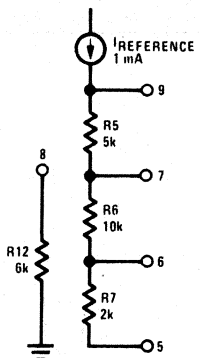
DESCRIPTION OF OPTIONS

Ripple Rejection Compensation. (Increases Ripple Rejection Typically to 80 dB)

The ripple rejection may be improved by connecting an external capacitor between pin 9 and ground. (The typical performance curves show the rejection with a capacitance of 2.2 μFd.)

Internal Voltage Programming

The LH0075 provides various precision output voltages simply by using one or more of the internal resistors. A particular voltage may be obtained by external connections as shown in Table I.



R5, R6, R7 and R12 are precision-trimmed to 0.1%.

FIGURE 1

External Voltage Programming

An external resistance can be connected between pin 9 and ground to obtain any voltage from 0 to 27V using the following equation:

$$R_{EXT} = \frac{V_{OUT}\ \text{Desired}}{1\ \text{mA}}$$

The reference current (I_{REF}) has a typical temperature coefficient of −65 ppm/°C. Choosing a resistive material with a temperature coefficient of 65 ppm/°C will compensate the negative temperature coefficient, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is Nichrome, which has a typical temperature coefficient of 80 ppm/°C.

Since a current source is used as a reference, this makes remote voltage programming possible.

Current Limit Programming

The maximum current output of the device may be limited by adding two external resistors as shown below. The resistor values are easily calculated with the following equation:

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\,\mu A$$

where R_{SENSE} = 1 to 10Ω

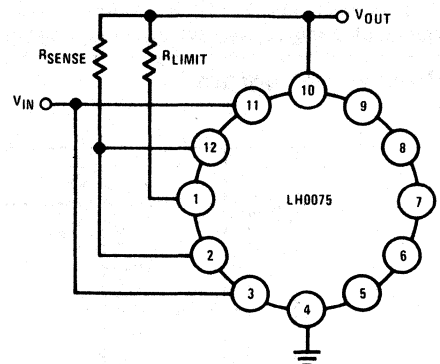


FIGURE 2. Current Limit Programming

This programmable current limit feature can be extended to make the LH0075 a programmable constant current source. This can be done by leaving pin 9 open and setting R_{LIMIT} and R_{SENSE} as desired.

For applications where the current limit is used, a minimum load current of 100 μA is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 μA, and it goes directly to the output of the LH0075. If the total current drawn from the output is less than the minimum, the output will rise.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. R_{SENSE} must be placed as close to the output of the LH0075 as possible, but R_{LIMIT} can be a fixed resistor or potentiometer located remotely from the device.

TABLE I. Connection Scheme for Internal Available Output Voltages

OUTPUT VOLTAGE (V)	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9
5			Gnd		
6				●	●
8	●	●		●	●
10		Gnd	●	●	●
12	Gnd		●	●	●
15		Gnd			
18	●		●	●	●

National Semiconductor

LH0076 Negative Precision Programmable Regulator

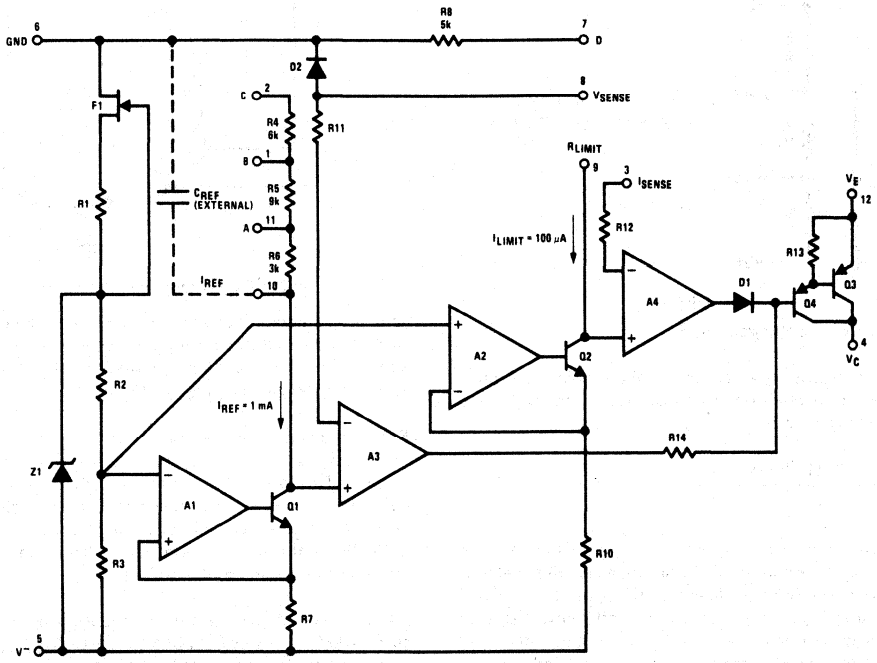
General Description

The LH0076 is a precision programmable regulator for negative voltages. Regulated output voltages from 0 to −27V may be obtained by using 1 external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (−3V, −5V, −6V, −8V, −9V, −12V, −15V and −18V). The output current limit is adjustable from 0 to 200 mA using 2 external resistors. These features provide an inventory of precision regulated values in 1 package.

Features

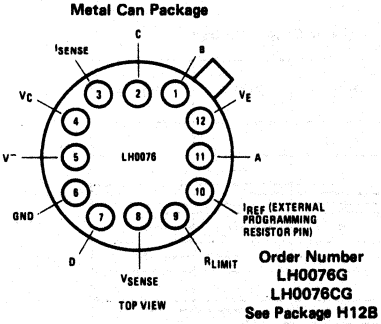
- Line regulation typically 0.005%/V
- Load regulation typically 0.02%
- Remote voltage sensing
- Ripple rejection—70 dB
- Output Adjustable to 0V
- Adjustable precision current limit
- Output current to 200 mA

Schematic Diagram



Connection Diagram

Metal Can Package

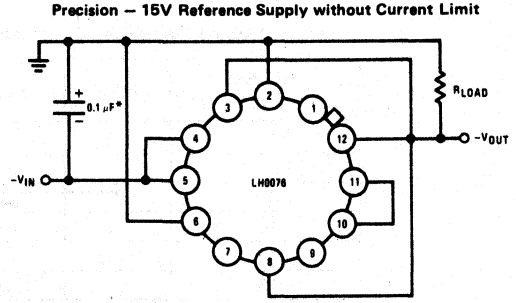


Order Number
LH0076G
LH0076CG
See Package H12B

Case is electrically isolated

Typical Application

Precision — 15V Reference Supply without Current Limit



*Recommended if device is far from filter capacitors

Absolute Maximum Ratings

Input Voltage	−32V
Output Voltage	−27V
Output Current	200 mA
Power Dissipation	See Curve
Operating Temperature	
LH0076	−55°C to +125°C
LH0076C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics Conditions are for $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

PARAMETER	CONDITIONS	LH0076			LH0076C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$T_A = 25°C$		0.005	0.02		0.005	0.04	%/V
Load Regulation	$T_A = 25°C$, 1 mA < I_{LOAD} < 200 mA							
	$V_{OUT} \geq -5V$			7.5			15	mV
	$V_{OUT} \leq -5V$		0.02	0.15		0.02	0.3	%
Reference Current (I_{REF})	$T_A = 25°C$, $V_{IN} = -15V$	0.998	1.000	1.002	0.995	1.000	1.005	mA
Reference Current Drift (ΔI_{REF}/ ΔTemp)	$V_{IN} = -15V$		−0.0065			−0.0065		%/°C
Minimum Load Current (I_{LIM})	(Note 1)	98	100	102	95	100	105	μA
Output Voltage Range		0		−27	0		−27	V
Minimum Input Voltage		−8			−8			V
Input-Output Differential Voltage	$T_A = 25°C$, 1 mA < I_{LOAD} < 200 mA		2.7	3.2		2.7	3.5	V
Quiescent Supply Current			9	10		9	11	mA
Ripple Rejection	$V_{OUT} = -5V$, f = 120 Hz		70			70		dB
Initial Output Voltage Tolerance	$T_A = 25°C$, (Note 2)		±0.1	±0.5		±0.1	±1.0	%
Output Voltage Change with Temperature	(Note 3)		0.003			0.003		%/°C

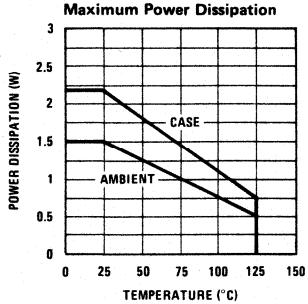
Note 1: Minimum load current is established by I_{LIM}, the current to Q2 (see schematic). I_{LIMIT} draws directly from the output if current limit feature is used.

Note 2: For $V_{IN} = -15V$ and V_{OUT} obtained by using R4, R5, R6 and R8 individually.

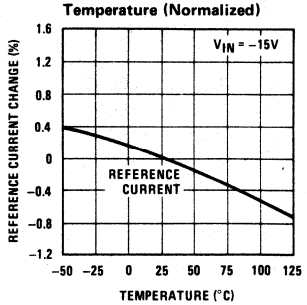
Note 3: Total change over specified temperature range.

Typical Performance Characteristics

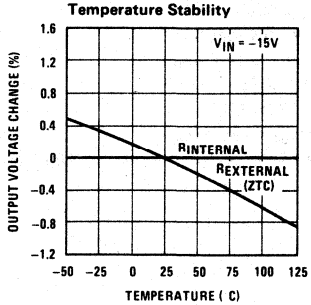
Maximum Power Dissipation



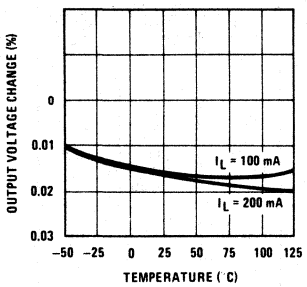
Reference Current Change with Temperature (Normalized)



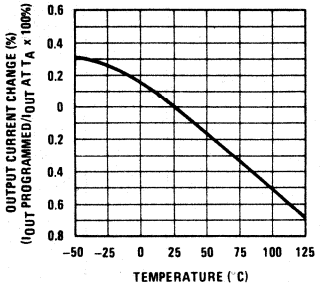
Temperature Stability



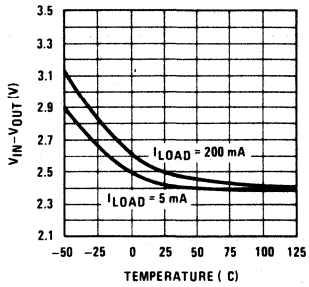
Output Voltage Change with Temperature (Normalized)



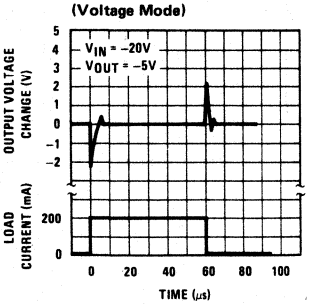
Current Limit



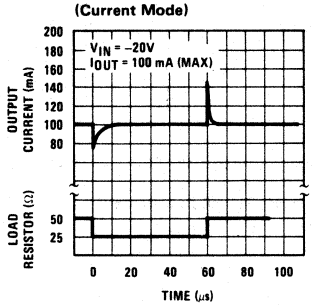
Input-Output Differential Voltage



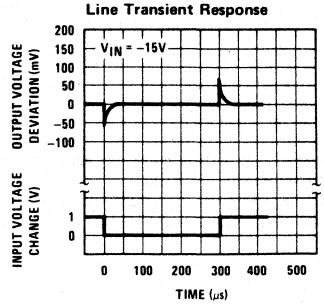
Load Transient Response (Voltage Mode)



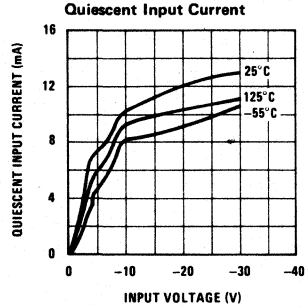
Load Transient Response (Current Mode)



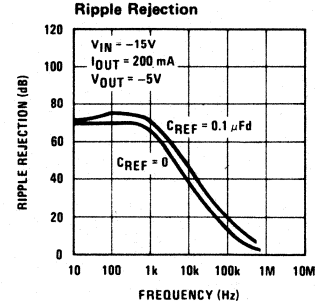
Line Transient Response



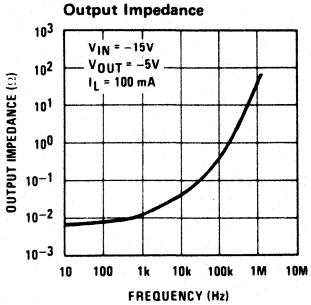
Quiescent Input Current



Ripple Rejection

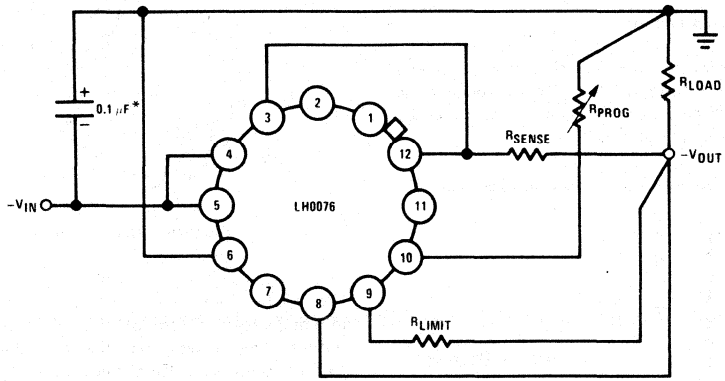


Output Impedance

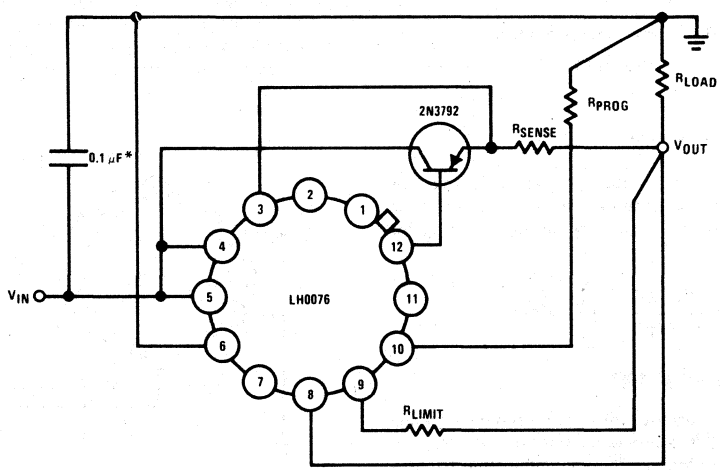


Typical Application (Continued)

Variable Voltage Reference with Current Limit



2-Amp Regulator with Current Limit



*Recommended if device is far from filter capacitors

Application Information

The LH0076 does not require external capacitors for stable operation. However, an input bypass is recommended if the device is far from filter capacitors. A 0.1 μF for input bypassing should be adequate for most applications.

DESCRIPTION OF OPTIONS

External Voltage Programming

An external resistance can be connected between pin 10 and ground to obtain any voltage from 0 to −27V using the following equation:

$$R_{EXT} = \frac{V_{OUT\ desired}}{-1\ mA}$$

The reference current (I_{REF}) has a typical temperature coefficient of −60 ppm/°C. Choosing a resistive material with a temperature coefficient of 60 ppm/°C will compensate the negative tempco of the reference current, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is nichrome, which has a typical tempco of 80 ppm/°C. Nichrome is the resistive material used in the LH0076, resulting in output voltage drift of 20 ppm/°C typically.

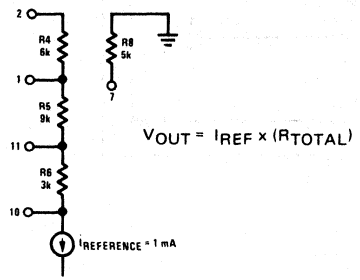
Application Information (Continued)

Because a current source is used as a reference, remote voltage programming is possible.

Internal Voltage Programming

The LH0076 provides various precision output voltages simply by using 1 or more of the internal programming resistors. These voltages may be obtained by using the connections as shown in Table I.

R_{TOTAL} is the total resistance between pin 10 and ground



R4, R5, R6 and R8 are precision trimmed to 0.1%

FIGURE 1

Current Limit Programming

The maximum current output of the device may be limited by adding 2 external resistors as shown in *Figure 2*. The resistor values are calculated using the following equation:

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\mu A$$

where R_{SENSE} = 1 to 10Ω

This programming current limit feature can be extended to make the LH0076 a programmable current sink. This can be done by leaving pin 10 open and setting R_{LIMIT} and R_{SENSE} as desired. (See *Figure 3*).

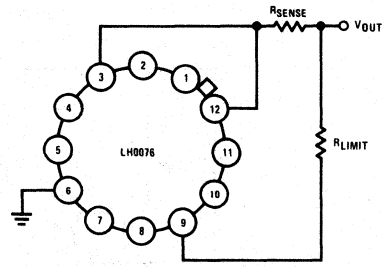


FIGURE 2. Current Limit Programming

For applications where the current limit is used, a minimum load current of 100 μA is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 μA, and it comes directly from the output of the LH0076. If the total load current is less than this minimum current, the output will drop.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. R_{SENSE} should be placed as close to the output of the LH0076 as possible, but R_{LIMIT} can be a resistor or potentiometer located remotely from the device.

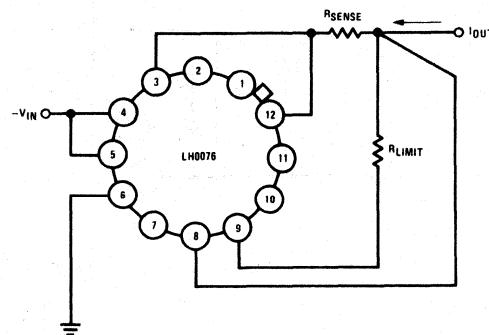


FIGURE 3. Precision Current Sink

TABLE I. Connection Scheme for Internally Available Output Voltages

OUTPUT VOLTAGE (V)	PIN 1	PIN 2	PIN 7	PIN 10	PIN 11
−3					Gnd
−5			•	•	
−6	•	Gnd		•	
−8			•	•	•
−9	Gnd			•	•
−12	Gnd				
−15		Gnd		•	•
−18		Gnd			

LM103 Reference Diode**

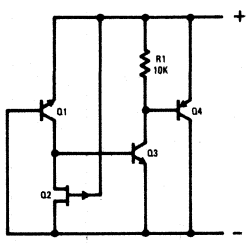
General Description

The LM103 is a two-terminal monolithic reference diode electrically equivalent to a breakdown diode. The device makes use of the reverse punch-through of double-diffused transistors, combined with active circuitry, to produce a breakdown characteristic which is ten times sharper than single-junction zener diodes at low voltages. Breakdown voltages from 1.8V to 5.6V are available; and, although the design is optimized for operation between 100 μA and 1 mA, it is completely specified from 10 μA to 10 mA. Noteworthy features of the device are:

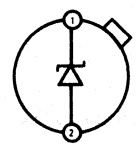
- Exceptionally sharp breakdown
- Low dynamic impedance from 10 μA to 10 mA
- Performance guaranteed over full military temperature range
- Planar, passivated junctions for stable operation
- Low capacitance.

The LM103, packaged in a hermetically sealed, modified TO-46 header is useful in a wide range of circuit applications from level shifting to simple voltage regulation. It can also be employed with operational amplifiers in producing breakpoints to generate nonlinear transfer functions. Finally, its unique characteristics recommend it as a reference element in low voltage power supplies with input voltages down to 4V.

Schematic and Connection Diagrams



Metal Can Package



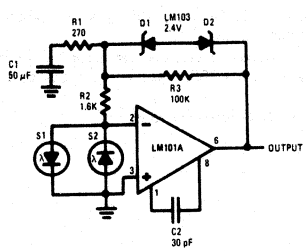
Note: Pin 2 connected to case.

TOP VIEW

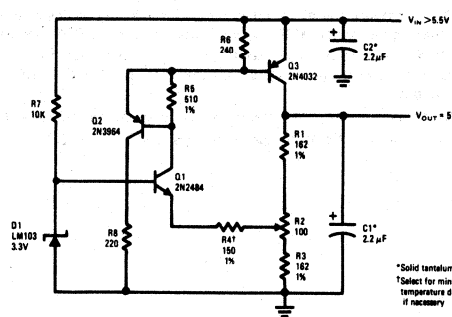
Order Number LM103H
See NS Package H02A

Typical Applications

Saturating Servo Preamplifier with Rate Feedback



200 mA Positive Regulator



**Covered by U.S. Patent Number 3,571,630

Absolute Maximum Ratings

Power Dissipation (note 1)	250 mW
Reverse Current	20 mA
Forward Current	100 mA
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 60 sec)	300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Breakdown Voltage Change	$10\ \mu A \leq I_R \leq 100\ \mu A$		60	120	mV
	$100\ \mu A \leq I_R \leq 1\ mA$		15	50	mV
	$1\ mA \leq I_R \leq 10\ mA$		50	150	mV
Reverse Dynamic Impedance (Note 3)	$I_R = 3\ mA$		5	25	Ω
	$I_R = 0.3\ mA$		15	60	Ω
Reverse Leakage Current	$V_R = V_Z - 0.2V$		2	5	μA
Forward Voltage Drop	$I_F = 10\ mA$	0.7	0.8	1.0	V
Peak-to-Peak Broadband Noise Voltage	$10\ Hz \leq f \leq 100\ kHz$, $I_R = 1\ mA$		300		μV
Reverse Breakdown Voltage Change with Current (Note 4)	$10\ \mu A \leq I_R \leq 100\ \mu A$			200	mV
	$100\ \mu A \leq I_R \leq 1\ mA$			60	mV
	$1\ mA \leq I_R \leq 10\ mA$			200	mV
Breakdown Voltage Temperature Coefficient (Note 4)	$100\ \mu A \leq I_R \leq 1\ mA$		−5.0		mV/°C

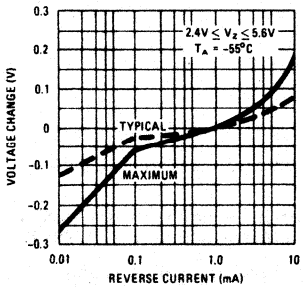
Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to case or 440°C/W junction to ambient (see curve).

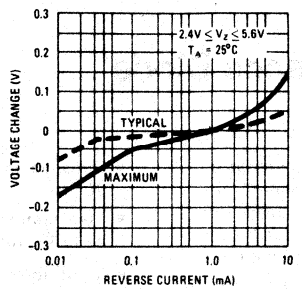
Note 2: These specifications apply for $T_A = 25°C$ and $1.8V < V_Z < 5.6V$ unless stated otherwise. The diode should not be operated with shunt capacitances between 100 pF and 0.01 μF, unless isolated by at least a 300Ω resistor, as it may oscillate at some currents.

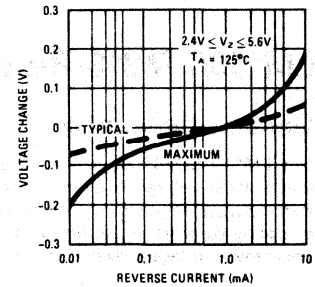
Note 3: Measured with the peak-to peak change of reverse current equal to 10% of the DC reverse current.

Note 4: These specifications apply for $-55°C < T_A < +125°C$.

Guaranteed Reverse Characteristics

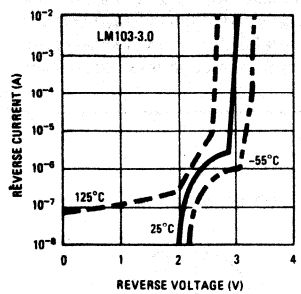




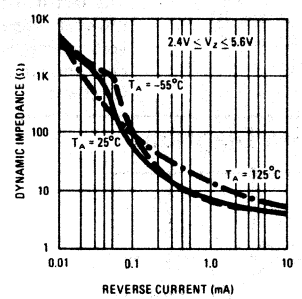


Typical Performance Characteristics

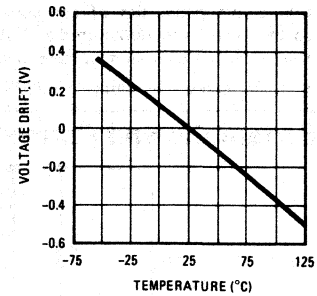
Reverse Characteristics



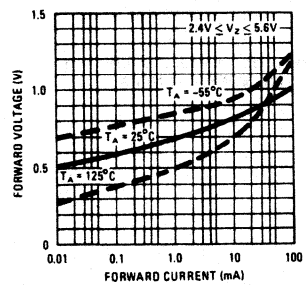
Reverse Dynamic Impedance



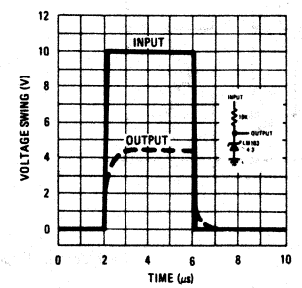
Temperature Drift



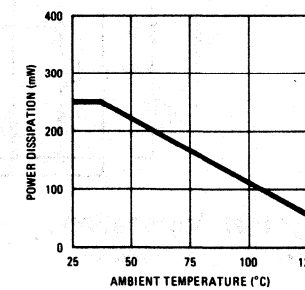
Forward Characteristics



Response Time



Maximum Power Dissipation



BREAKDOWN VOLTAGE*	PART NUMBER
1.8	LM103H-1.8
2.0	LM103H-2.0
2.2	LM103H-2.2
2.4	LM103H-2.4
2.7	LM103H-2.7
3.0	LM103H-3.0
3.3	LM103H-3.3
3.6	LM103H-3.6
3.9	LM103H-3.9
4.3	LM103H-4.3
4.7	LM103H-4.7
5.1	LM103H-5.1
5.6	LM103H-5.6

*Measured at I_R = 1 mA.
Standard tolerance is ±10%.

National Semiconductor

LM113/LM313 Reference Diode

General Description

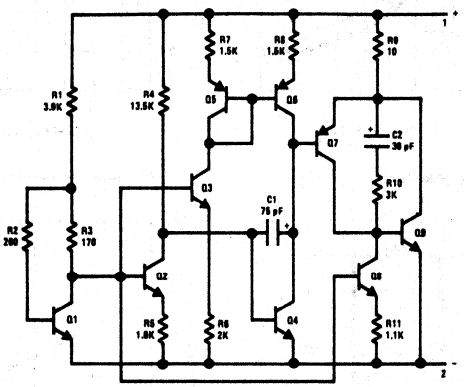
The LM113/LM313 are temperature compensated, low voltage reference diodes. They feature extremely-tight regulation over a wide range of operating currents in addition to an unusually-low breakdown voltage and good temperature stability.

The diodes are synthesized using transistors and resistors in a monolithic integrated circuit. As such, they have the same low noise and long term stability as modern IC op amps. Further, output voltage of the reference depends only on highly-predictable properties of components in the IC; so they can be manufactured and supplied to tight tolerances. Outstanding features include:

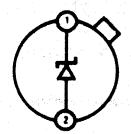
- Low breakdown voltage: 1.220V
- Dynamic impedance of 0.3Ω from 500 μA to 20 mA
- Temperature stability typically 1% over −55°C to 125°C range (LM113), 0°C to 70°C (LM313)
- Tight tolerance: ±5% standard, ±2% and ±1% on special order.

The characteristics of this reference recommend it for use in bias-regulation circuitry, in low-voltage power supplies or in battery powered equipment. The fact that the breakdown voltage is equal to a physical property of silicon—the energy-band-gap voltage—makes it useful for many temperature-compensation and temperature-measurement functions.

Schematic and Connection Diagrams



Metal Can Package

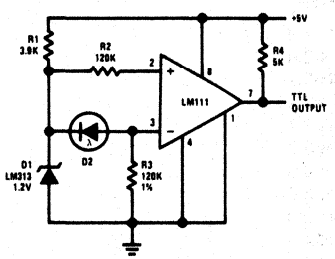


Note: Pin 2 connected to case.
TOP VIEW

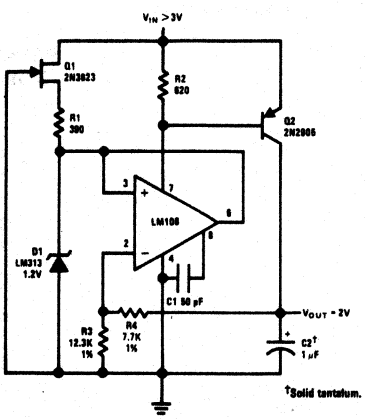
Order Number LM113H or LM313H
See NS Package H02A

Typical Applications

Level Detector for Photodiode



Low Voltage Regulator



Absolute Maximum Ratings

Power Dissipation (Note 1)	100 mW
Reverse Current	50 mA
Forward Current	50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Temperature (T_A)			
LM113	−55	+125	°C
LM313	0	70	°C

Electrical Characteristics (Note 2)

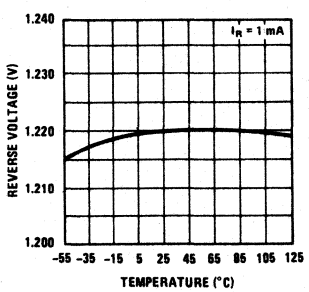
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage					
LM113/LM313	I_R = 1 mA	1.160	1.220	1.280	V
LM113-1		1.210	1.22	1.232	V
LM113-2		1.195	1.22	1.245	V
Reverse Breakdown Voltage Change	0.5 mA ≤ I_R ≤ 20 mA		6.0	15	mV
Reverse Dynamic Impedance	I_R = 1 mA		0.2	1.0	Ω
	I_R = 10 mA		0.25	0.8	Ω
Forward Voltage Drop	I_F = 1.0 mA		0.67	1.0	V
RMS Noise Voltage	10 Hz ≤ f ≤ 10 kHz, I_R = 1 mA		5		μV
Reverse Breakdown Voltage Change with Current	0.5 mA ≤ I_R ≤ 10 mA, T_{MIN} ≤ T_A ≤ T_{MAX}			15	mV
Breakdown Voltage Temperature Coefficient	1.0 mA ≤ I_R ≤ 10 mA, T_{MIN} ≤ T_A ≤ T_{MAX}		0.01		%/°C

Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction and a thermal resistance of 80°C/W junction to case or 440°C/W junction to ambient.

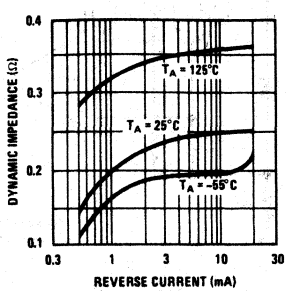
Note 2: These specifications apply for T_A = 25°C, unless stated otherwise. At high currents, breakdown voltage should be measured with lead lengths less than 1/4 inch. Kelvin contact sockets are also recommended. The diode should not be operated with shunt capacitances between 200 pF and 0.1 μF, unless isolated by at least a 100 Ω resistor, as it may oscillate at some currents.

Typical Performance Characteristics

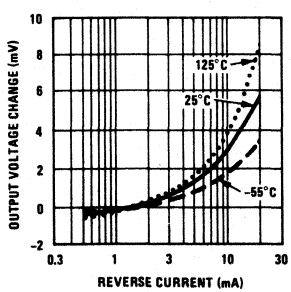
Temperature Drift



Reverse Dynamic Impedance

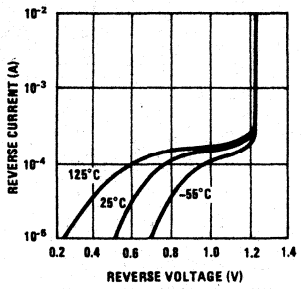


Reverse Characteristics

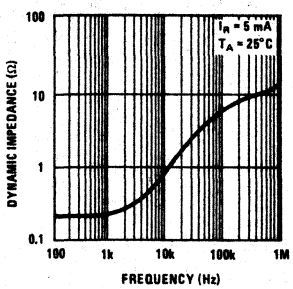


Typical Performance Characteristics (Continued)

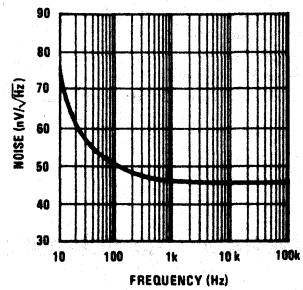
Reverse Characteristics



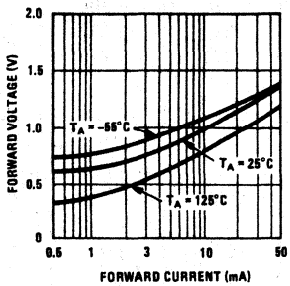
Reverse Dynamic Impedance



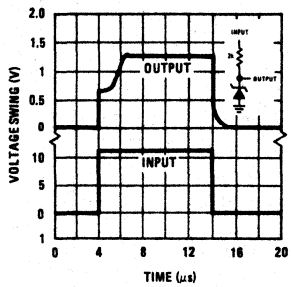
Noise Voltage



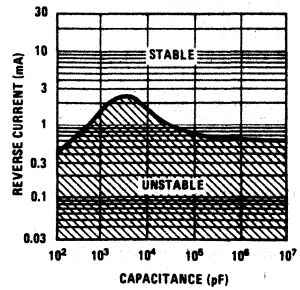
Forward Characteristics



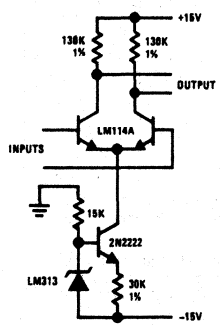
Response Time



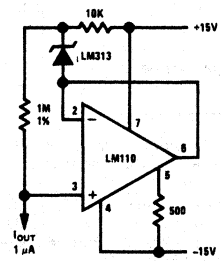
Maximum Shunt Capacitance



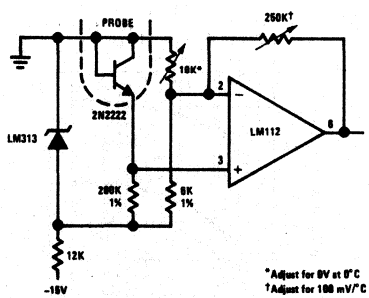
Typical Applications (Continued)



Amplifier Biasing for Constant Gain with Temperature



Constant Current Source



Thermometer

National Semiconductor

LM129/LM329 Precision Reference

General Description

The LM129 and LM329 family are precision multi-current temperature compensated 6.9V zener references with dynamic impedances a factor of 10 to 100 less than discrete diodes. Constructed in a single silicon chip, the LM129 uses active circuitry to buffer the internal zener allowing the device to operate over a 0.5 mA to 15 mA range with virtually no change in performance. The LM129 and LM329 are available with selected temperature coefficients of 0.001, 0.002, 0.005 and 0.01%/°C. These new references also have excellent long term stability and low noise.

A new subsurface breakdown zener used in the LM129 gives lower noise and better long term stability than conventional IC zeners. Further the zener and temperature compensating transistor are made by a planar process so they are immune to problems that plague ordinary zeners. For example, there is virtually no voltage shifts in zener voltage due to temperature cycling and the device is insensitive to stress on the leads.

The LM129 can be used in place of conventional zeners with improved performance. The low dynamic impedance simplifies biasing and the wide operating current allows the replacement of many zener types.

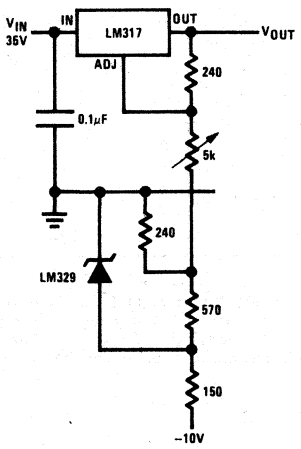
The LM129 is packaged in a 2-lead TO-46 package and is rated for operation over a −55°C to +125°C temperature range. The LM329 for operation over 0–70°C is available in both a hermetic TO-46 package and a TO-92 epoxy package.

Features

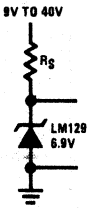
- 0.6 mA to 15 mA operating current
- 0.6Ω dynamic impedance at any current
- Available with temperature coefficients of 0.001%/°C
- 7μV wideband noise
- 5% initial tolerance
- 0.002% long term stability
- Low cost
- Subsurface zener

Typical Applications

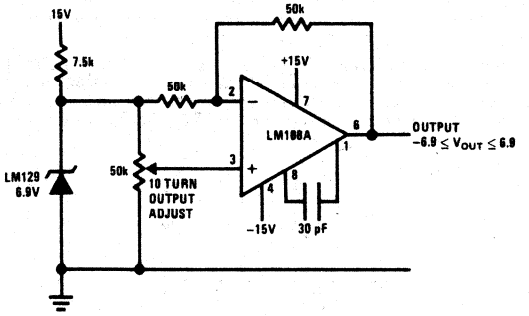
Low Cost 0–25V Regulator



Simple Reference



Adjustable Bipolar Output Reference



Absolute Maximum Ratings

Reverse Breakdown Current	30 mA
Forward Current	2 mA
Operating Temperature Range	
LM129	−55°C to +125°C
LM329	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

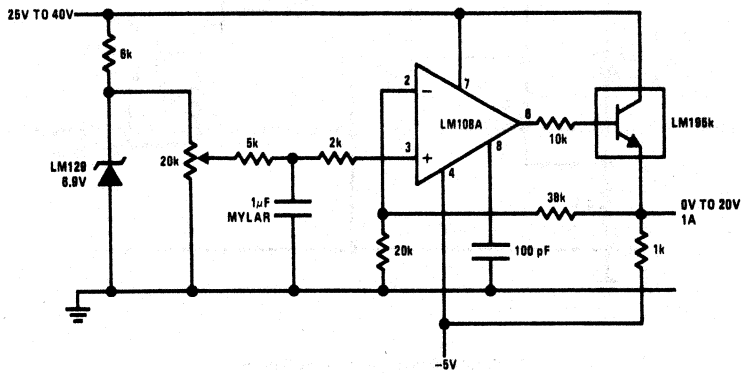
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM129A, B, C			LM329B, C, D			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$T_A = 25°C$, $0.6\ mA \leq I_R \leq 15\ mA$	6.7	6.9	7.2	6.6	6.9	7.25	V
Reverse Breakdown Change with Current	$T_A = 25°C$, $0.6\ mA \leq I_R \leq 15\ mA$		9	14		9	20	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1\ mA$		0.6	1		0.8	2	Ω
RMS Noise	$T_A = 25°C$, $10\ Hz \leq F \leq 10\ kHz$		7	20		7	100	μV
Long Term Stability	$T_A = 45°C \pm 0.1°C$, $I_R = 1\ mA \pm 0.3\%$		20			20		ppm
Temperature Coefficient	$I_R = 1\ mA$							
LM129A, LM329A			6	10		6	10	ppm/°C
LM129B, LM329B			15	20		15	20	ppm/°C
LM129C, LM329C			30	50		30	50	ppm/°C
LM329D						50	100	ppm/°C
Change In Reverse Breakdown Temperature Coefficient	$1\ mA \leq I_R \leq 15\ mA$		1			1		ppm/°C
Reverse Breakdown Change with Current	$1\ mA \leq I_R \leq 15\ mA$		12			12		mV
Reverse Dynamic Impedance	$1\ mA \leq I_R \leq 15\ mA$		0.8			1		Ω

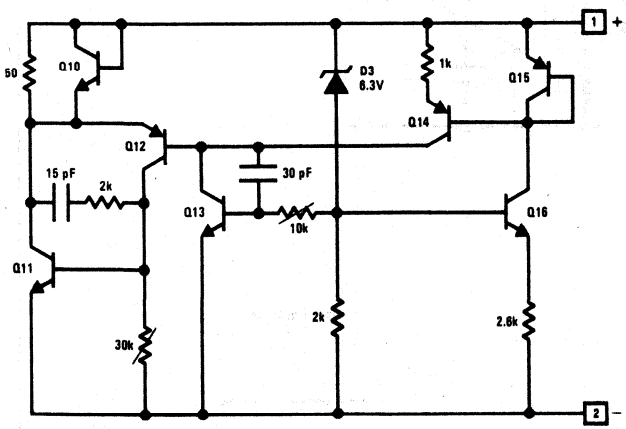
Note 1: These specifications apply for $-55°C \leq T_A \leq +125°C$ for the LM129 and $0°C \leq T_A \leq +70°C$ for the LM329 unless otherwise specified. The maximum junction temperature for an LM129 is 150°C and LM329 is 100°C. For operating at elevated temperature, devices in TO-46 package must be derated based on a thermal resistance of 440°C/W junction to ambient or 80°C/W junction to case. For the TO-92 package, the derating is based on 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

Typical Applications (Continued)

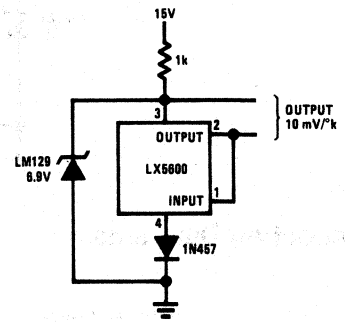
0V to 20V Power Reference



Reference



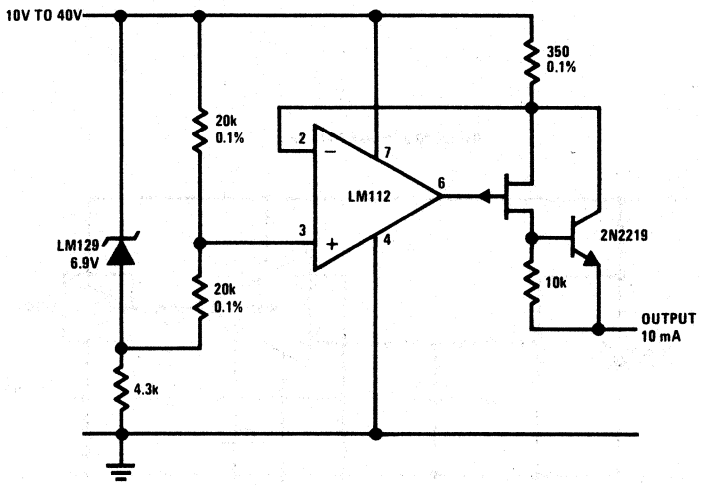
External Reference for Temperature Transducer



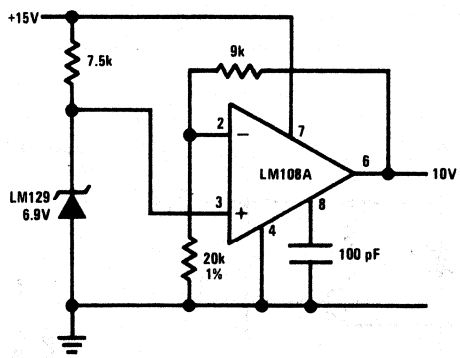
14

Typical Applications (Continued)

Positive Current Source

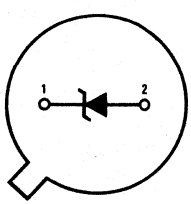


Buffered Reference with Single Supply



Connection Diagrams

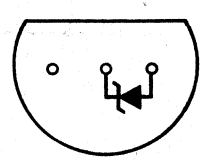
Metal Can Package



BOTTOM VIEW

Order Number LM129AH, LM129BH
LM129CH, LM329AH, LM329BH, LM329CH
or LM329DH
See NS Package H02A

Plastic Package

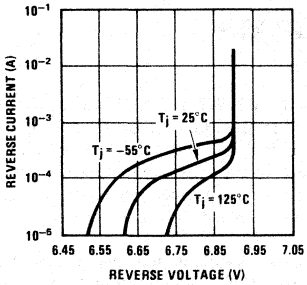


BOTTOM VIEW

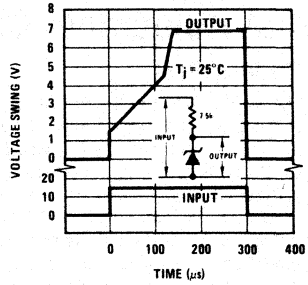
Order Number LM329BZ, LM329CZ
or LM329DZ
See NS Package Z03A

Typical Performance Characteristics

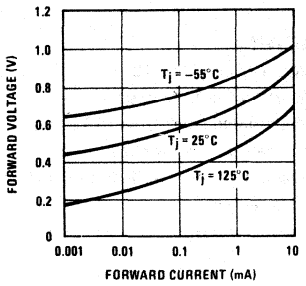
Reverse Characteristics



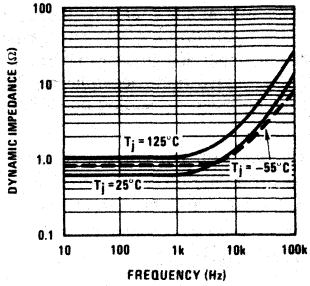
Response Time



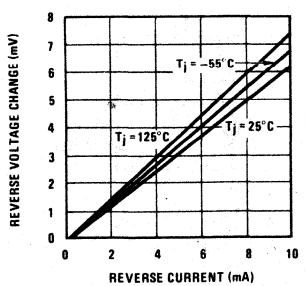
Forward Characteristics



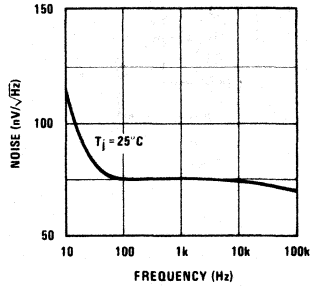
Dynamic Impedance



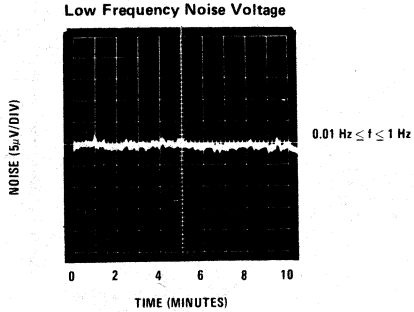
Reverse Voltage Change



Zener Noise Voltage



Low Frequency Noise Voltage



National Semiconductor

LM134/LM234/LM334
3-Terminal Adjustable Current Sources

General Description

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64 mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈+0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the new current sources include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The LM134-3/LM234-3 and LM134-6/LM234-6 are specified as true temperature sensors with guaranteed initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

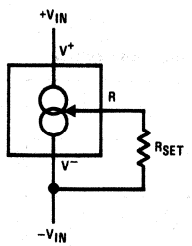
The LM134 is guaranteed over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO-46 hermetic and TO-92 plastic packages.

Features

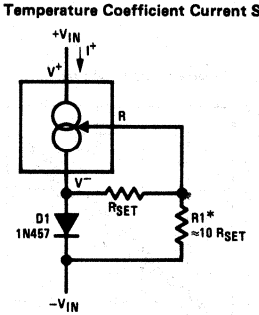
- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1 μA to 10 mA
- True 2-terminal operation
- Available as fully specified temperature sensor
- ±3% initial accuracy

Typical Applications

Basic 2-Terminal Current Source

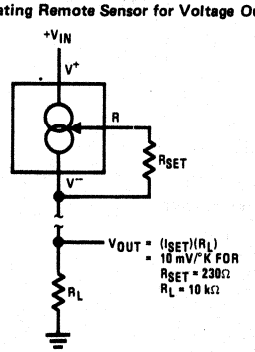


Zero Temperature Coefficient Current Source

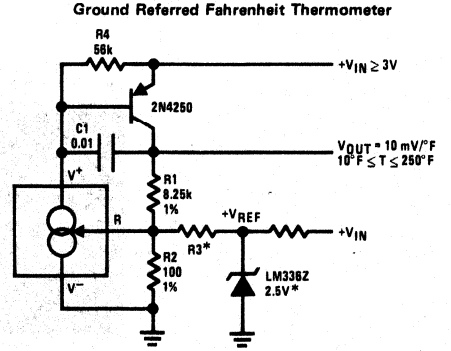


*Select ratio of R1 to R_{SET} to obtain zero drift. $I^+ \approx 2\ I_{SET}$

Terminating Remote Sensor for Voltage Output



Ground Referred Fahrenheit Thermometer



*Select R3 = V_{REF}/583 μA. V_{REF} may be any stable positive voltage ≥ 2V
Trim R3 to calibrate

Absolute Maximum Ratings

V^+ to V^- Forward Voltage	
LM134/LM234	40V
LM334/LM134-3/LM134-6/LM234-3/LM234-6	30V
V^+ to V^- Reverse Voltage	20V
R Pin to V^- Voltage	5V
Set Current	10 mA
Power Dissipation	200 mW
Operating Temperature Range	
LM134/LM134-3/LM134-6	−55°C to +125°C
LM234/LM234-3/LM234-6	−25°C to +100°C
LM334	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM134/LM234			LM334			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Set Current Error, V^+ = 2.5V, (Note 2)	10 μA ≤ I_{SET} ≤ 1 mA			3			6	%
	1 mA < I_{SET} ≤ 5 mA			5			8	%
	2 μA ≤ I_{SET} < 10 μA			5			8	%
Ratio of Set Current to V^- Current	10 μA ≤ I_{SET} ≤ 1 mA	14	18	23	14	18	26	
	1 mA ≤ I_{SET} ≤ 5 mA		14			14		
	2 μA ≤ I_{SET} ≤ 10 μA	14	18	23	14	18	26	
Minimum Operating Voltage	2 μA ≤ I_{SET} ≤ 100 μA		0.8			0.8		V
	100 μA < I_{SET} ≤ 1 mA		0.9			0.9		V
	1 mA < I_{SET} ≤ 5 mA		1.0			1.0		V
Average Change in Set Current with Input Voltage	1.5 ≤ V^+ ≤ 5V 2 μA ≤ I_{SET} ≤ 1 mA		0.02	0.05		0.02	0.1	%/V
	5V ≤ V^+ ≤ 40V		0.01	0.03		0.01	0.05	%/V
	1.5V ≤ V ≤ 5V 1 mA < I_{SET} ≤ 5 mA		0.03			0.03		%/V
	5V ≤ V ≤ 40V		0.02			0.02		%/V
Temperature Dependence of Set Current (Note 3)	25 μA ≤ I_{SET} ≤ 1 mA	0.96T	T	1.04T	0.96T	T	1.04T	
Effective Shunt Capacitance			15			15		pF

Note 1: Unless otherwise specified, tests are performed at T_j = 25°C with pulse testing so that junction temperature does not change during test.

Note 2: Set current is the current flowing into the V^+ pin. It is determined by the following formula: I_{SET} = 67.7 mV/R_{SET} (@ 25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C @ T_j = 25°C.

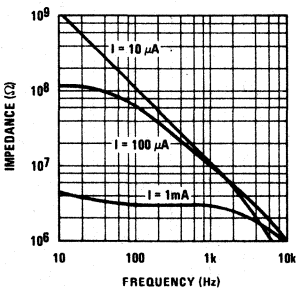
Note 3: I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_o (T/T_o)$ where I_o is I_{SET} measured at T_o (°K).

Electrical Characteristics (Continued) (Note 1)

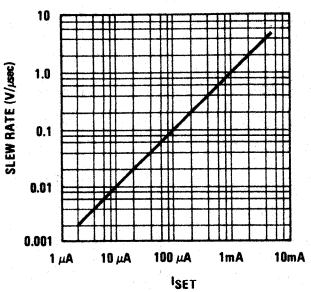
PARAMETER	CONDITIONS	LM134-3, LM234-3			LM134-6, LM234-6			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$100\ \mu A \leq I_{SET} \leq 1\ mA$ $T_j = 25°C$			±1			±2	%
Equivalent Temperature Error				±3			±6	°C
Ratio of Set Current to V^- Current	$100\ \mu A \leq I_{SET} \leq 1\ mA$	14	18	26	14	18	26	
Minimum Operating Voltage	$100\ \mu A\ I_{SET} \leq 1\ mA$		0.9			0.9		V
Average Change in Set Current with Input Voltage	$1.5 \leq V^+ \leq 5V$		0.02	0.05		0.02	0.1	%/V
	$100\ \mu A \leq I_{SET} \leq 1\ mA$ $5V \leq V^+ \leq 30V$		0.01	0.03		0.01	0.05	%/V
Temperature Dependence of Set Current (Note 3) and Equivalent Slope Error	$100\ \mu A \leq I_{SET} \leq 1\ mA$	0.98T	T	1.02T	0.97T	T	1.03T	
				±2			±3	%
Effective Shunt Capacitance			15			15		pF

Typical Performance Characteristics

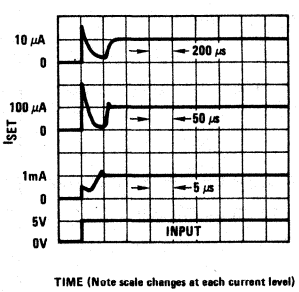
Output Impedance



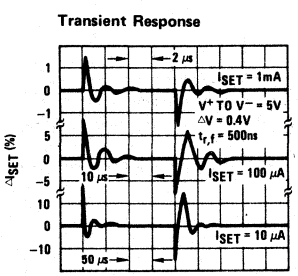
Maximum Slew Rate for Linear Operation



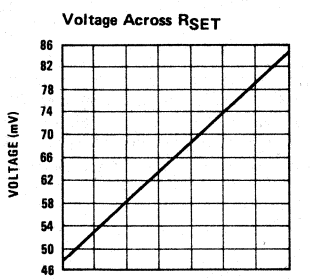
Start-Up



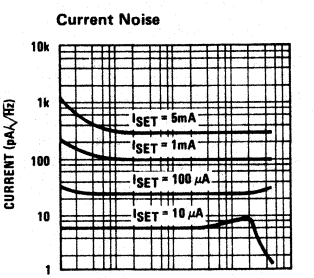
Transient Response



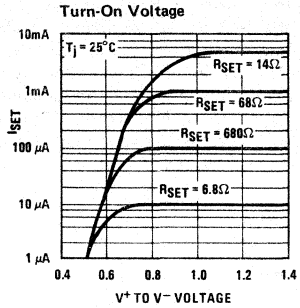
Voltage Across R_{SET}

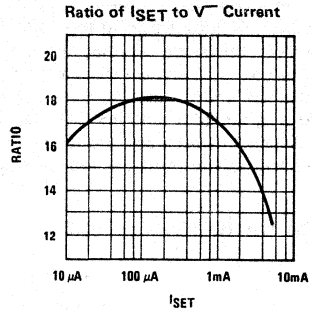


Current Noise



Typical Performance Characteristics (Continued)





Application Hints

The LM134 has been designed for ease of application, but a general discussion of design features is presented here to familiarize the designer with device characteristics which may not be immediately obvious. These include the effects of slewing, power dissipation, capacitance, noise, and contact resistance.

SLEW RATE

At slew rates above a given threshold (see curve), the LM134 may exhibit non-linear current shifts. The slewing rate at which this occurs is directly proportional to I_{SET}. At I_{SET} = 10 μA, maximum dV/dt is 0.01V/μs; at I_{SET} = 1 mA, the limit is 1V/μs. Slew rates above the limit do not harm the LM134, or cause large currents to flow.

THERMAL EFFECTS

Internal heating can have a significant effect on current regulation for I_{SET} greater than 100 μA. For example, each 1V increase across the LM134 at I_{SET} = 1 mA will increase junction temperature by ≈ 0.4°C in still air. Output current (I_{SET}) has a temperature coefficient of ≈ 0.33%/°C, so the change in current due to temperature rise will be (0.4)(0.33) = 0.132%. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when DC regulation is critical and I_{SET} exceeds 100 μA. Heat sinking of the TO-46 package or the TO-92 leads can reduce this effect by more than 3:1.

SHUNT CAPACITANCE

In certain applications, the 15 pF shunt capacitance of the LM134 may have to be reduced, either because of loading problems or because it limits the AC output impedance of the current source. This can be easily accomplished by buffering the LM134 with an FET as shown in the applications. This can reduce capacitance to less than 3 pF and improve regulation by at least an order of magnitude. DC characteristics (with the exception of minimum input voltage), are not affected.

NOISE

Current noise generated by the LM134 is approximately 4 times the shot noise of a transistor. If the LM134 is used as an active load for a transistor amplifier, input referred noise will be increased by about 12 dB. In many cases, this is acceptable and a single stage amplifier can be built with a voltage gain exceeding 2000.

LEAD RESISTANCE

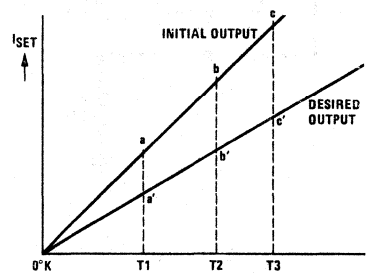
The sense voltage which determines operating current of the LM134 is less than 100 mV. At this level, thermocouple or lead resistance effects should be minimized by locating the current setting resistor physically close to the device. Sockets should be avoided if possible. It takes only 0.7Ω contact resistance to reduce output current by 1% at the 1 mA level.

SENSING TEMPERATURE

The LM134 makes an ideal remote temperature sensor because its current mode operation does not lose accuracy over long wire runs. Output current is directly proportional to absolute temperature in degrees Kelvin, according to the following formula:

$$I_{SET} = \frac{(227\ \mu V/^{\circ}K)(T)}{R_{SET}}$$

Calibration of the LM134 is greatly simplified because of the fact that most of the initial inaccuracy is due to a gain term (slope error) and not an offset. This means that a calibration consisting of a gain adjustment only will trim both slope and zero at the same time. In addition, gain adjustment is a one point trim because the output of the LM134 extrapolates to zero at 0°K, independent of R_{SET} or any initial inaccuracy.



This property of the LM134 is illustrated in the accompanying graph. Line abc is the sensor current before

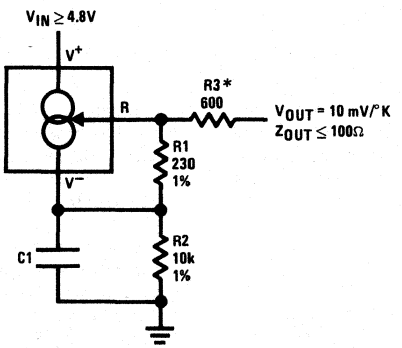
Application Hints (Continued)

trimming. Line a'b'c' is the desired output. A gain trim done at T2 will move the output from b to b' and will simultaneously correct the slope so that the output at T1 and T3 will be correct. This gain trim can be done on R_{SET} or on the load resistor used to terminate the LM134. Slope error after trim will normally be less than ±1%. To maintain this accuracy, however, a low temperature coefficient resistor must be used for R_{SET}.

A 33 ppm/°C drift of R_{SET} will give a 1% slope error because the resistor will normally see about the same temperature variations as the LM134. Separating R_{SET} from the LM134 requires 3 wires and has lead resistance problems, so is not normally recommended. Metal film resistors with less than 20 ppm/°C drift are readily available. Wire wound resistors may also be used where best stability is required.

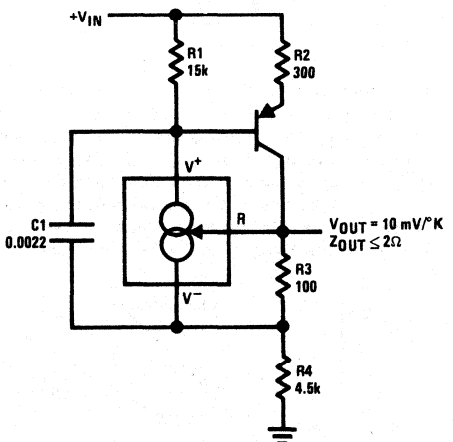
Typical Applications (Continued)

Low Output Impedance Thermometer

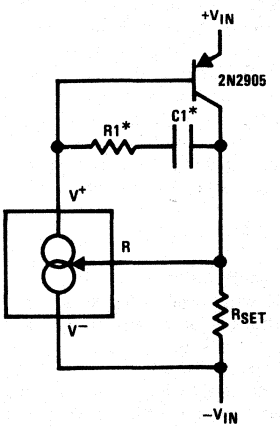


*Output impedance of the LM134 at the "R" pin is approximately $\frac{-R_O\ \Omega}{16}$, where R_O is the equivalent external resistance connected to the V^- pin. This negative resistance can be reduced by a factor of 5 or more by inserting an equivalent resistor in series with the output.

Low Output Impedance Thermometer



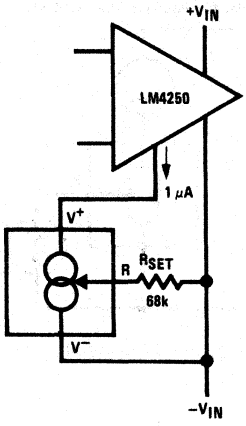
Higher Output Current



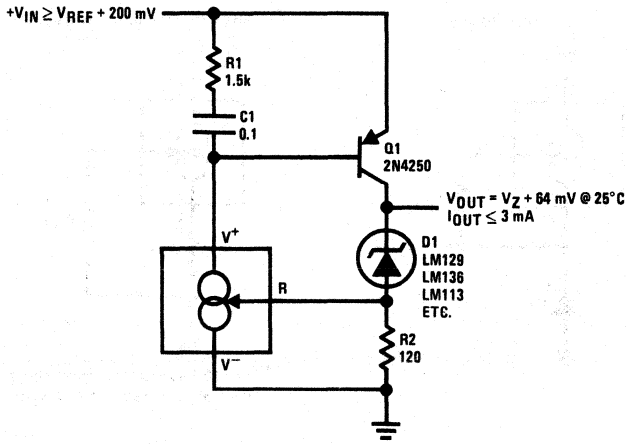
*Select R1 and C1 for optimum stability

Typical Applications (Continued)

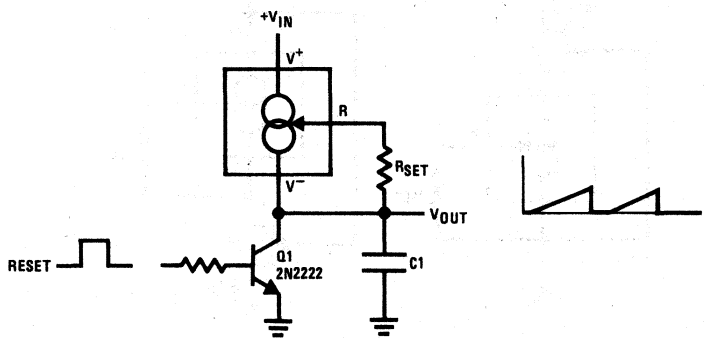
Micropower Bias



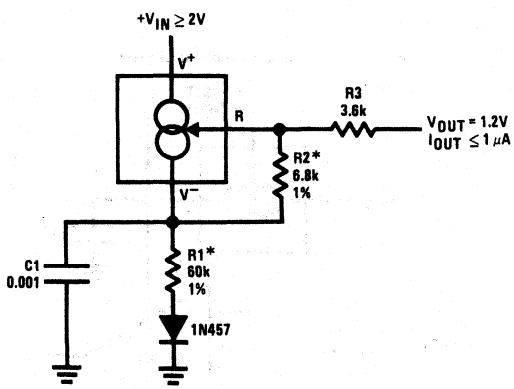
Low Input Voltage Reference Driver



Ramp Generator

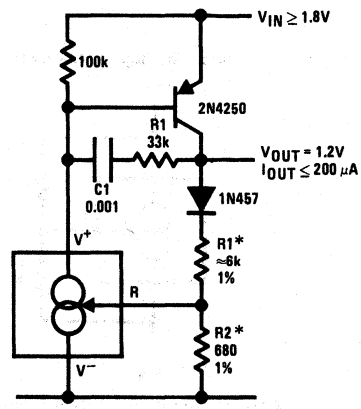


1.2V Reference Operates on 10 μA and 2V



*Select ratio of R1 to R2 to obtain zero temperature drift

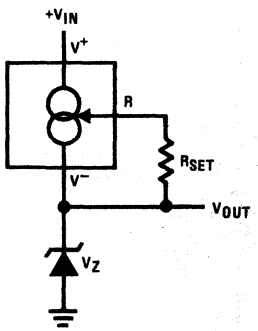
1.2V Regulator with 1.8V Minimum Input



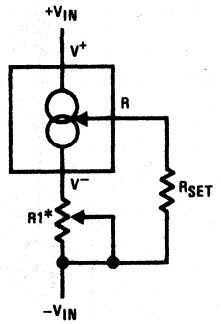
*Select ratio of R1 to R2 for zero temperature drift

Typical Applications (Continued)

Zener Biasing

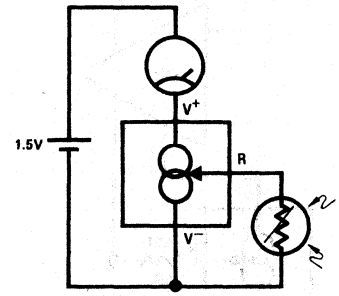


Alternate Trimming Technique

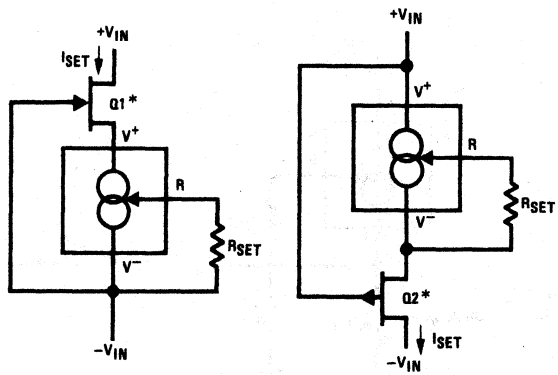


*For ±10% adjustment, select R_{SET} 10% high, and make R1 ≈ 3 R_{SET}

Buffer for Photoconductive Cell

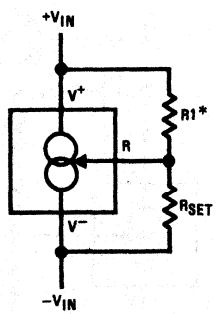


FET Cascoding for Low Capacitance and/or Ultra High Output Impedance



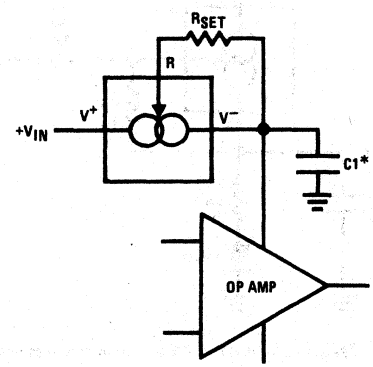
*Select Q1 or Q2 to ensure at least 1V across the LM134. $V_p\ (1 - I_{SET}/I_{DSS}) \geq 1.2V$.

Generating Negative Output Impedance



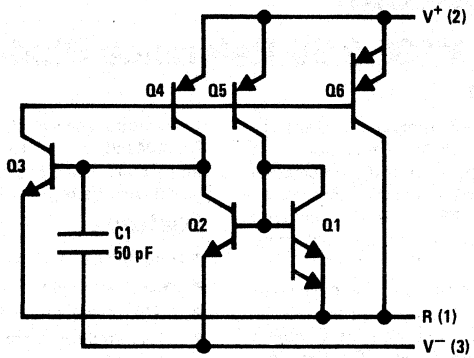
*$Z_{OUT} \approx -16 \cdot R1\ (R1/V_{IN}$ must not exceed $I_{SET})$

In-Line Current Limiter

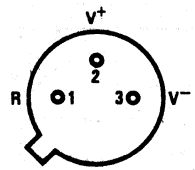


*Use minimum value required to ensure stability of protected device. This minimizes inrush current to a direct short.

Schematic and Connection Diagrams



TO-46
Metal Can Package

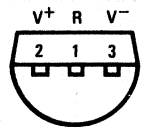


BOTTOM VIEW

Pin 3 is electrically connected to case

Order Number LM134H, LM134H-3, LM134H-6, LM234H, LM234H-3, LM234H-6 or LM334H
See NS Package H03H

TO-92
Plastic Package



BOTTOM VIEW

Order Number LM334Z, LM234Z-3 or LM234Z-6
See NS Package Z03A

National Semiconductor

LM136/LM236/LM336 2.5V Reference Diode

General Description

The LM136/LM236 and LM336 integrated circuits are precision 2.5V shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient 2.5V zener with 0.2Ω dynamic impedance. A third terminal on the LM136 allows the reference voltage and temperature coefficient to be trimmed easily.

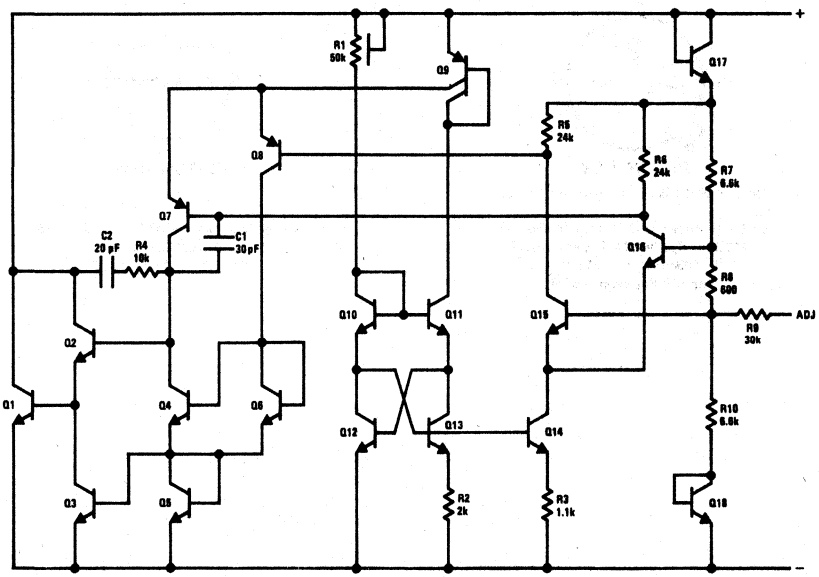
The LM136 series is useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from 5V logic supplies. Further, since the LM136 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

The LM136 is rated for operation over −55°C to +125°C while the LM236 is rated over a −25°C to +85°C temperature range. Both are packaged in a TO-46 package. The LM336 is rated for operation over a 0°C to +70°C temperature range and is available in either a three lead TO-46 package or a TO-92 plastic package.

Features

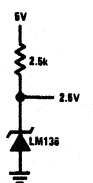
- Low temperature coefficient
- Wide operating current of 300 μA to 10 mA
- 0.2Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package
- 5.0V device also available—LM336–5.0

Schematic Diagram

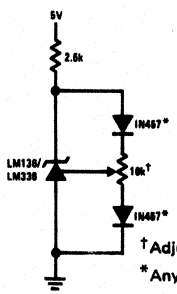


Typical Applications

2.5V Reference



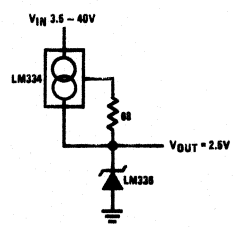
2.5V Reference with Minimum Temperature Coefficient



†Adjust to 2.490V

*Any silicon signal diode

Wide Input Range Reference



Absolute Maximum Ratings

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	−60°C to +150°C
Operating Temperature	
LM136	−55°C to +150°C
LM236	−25°C to +85°C
LM336	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

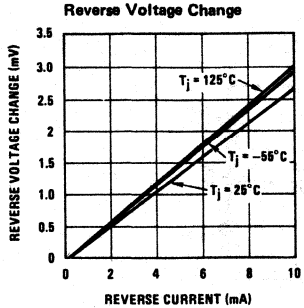
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM136A/LM236A LM136/LM236			LM336B LM336			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1$ mA							
	LM136/LM236/LM336	2.440	2.490	2.540	2.390	2.490	2.590	V
	LM136A/LM236A, LM336B	2.465	2.490	2.515	2.440	2.490	2.540	V
Reverse Breakdown Change With Current	$T_A = 25°C$, $400\ \mu A \leq I_R \leq 10$ mA		2.6	6		2.6	10	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1$ mA		0.2	0.6		0.2	1	Ω
Temperature Stability	V_R Adjusted to 2.490V, $I_R = 1$ mA, *(Figure 2)*							
	$0°C \leq T_A \leq 70°C$ (LM336)					1.8	6	mV
	$-25°C \leq T_A \leq +85°C$ (LM236)		3.5	9				mV
	$-55°C \leq T_A \leq +125°C$ (LM136)		12	18				mV
Reverse Breakdown Change With Current	$400\ \mu A \leq I_R \leq 10$ mA		3	10		3	12	mV
Reverse Dynamic Impedance	$I_R = 1$ mA		0.4	1		0.4	1.4	Ω
Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1$ mA		20			20		ppm

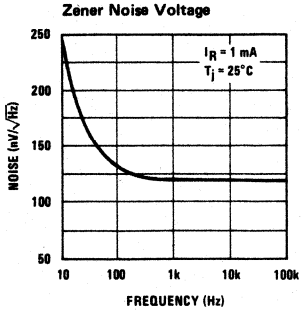
Note 1: Unless otherwise specified, the LM136 is specified from $-55°C \leq T_A \leq +125°C$, the LM236 from $-25°C \leq T_A \leq +85°C$ and the LM336 from $0°C \leq T_A \leq +70°C$. The maximum junction temperature of the LM136 is 150°C, LM236 is 125°C and the LM336 is 100°C. For elevated junction temperature, devices in the TO-46 package should be derated based on a thermal resistance of 440°C/W junction to ambient or 80°C/W junction to case. For the TO-92 package, the derating is based on 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

Typical Performance Characteristics

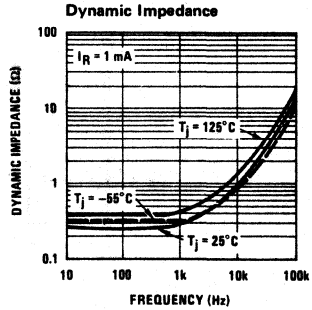
Reverse Voltage Change



Zener Noise Voltage

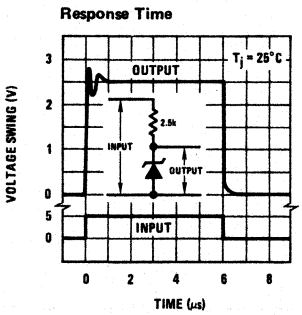


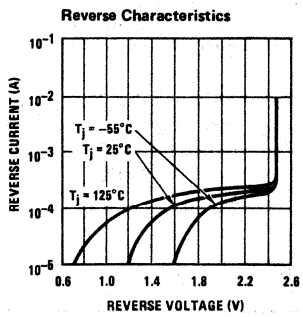
Dynamic Impedance

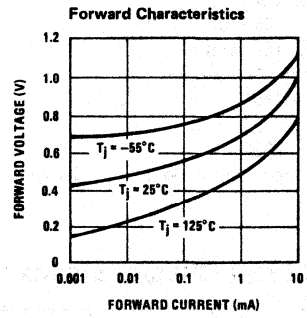


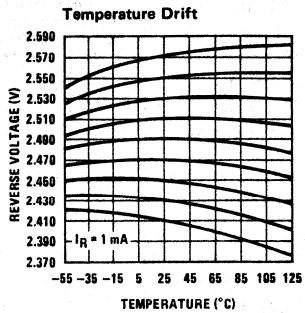
14

Typical Performance Characteristics (Continued)









Application Hints

The LM136 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

If minimum temperature coefficient is desired, two diodes can be added in series with the adjustment potentiometer as shown in *Figure 2*. When the device is adjusted to 2.490V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136. It is usually sufficient to mount the diodes near the LM136 on the printed circuit board. The absolute resistance of R1 is not critical and any value from 2k to 20k will work.

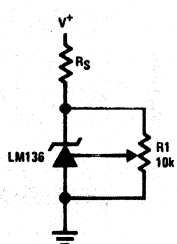


FIGURE 1. LM136 With Pot for Adjustment of Breakdown Voltage

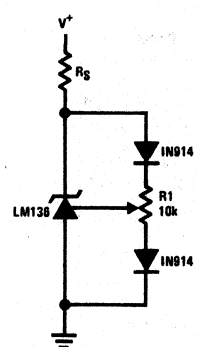
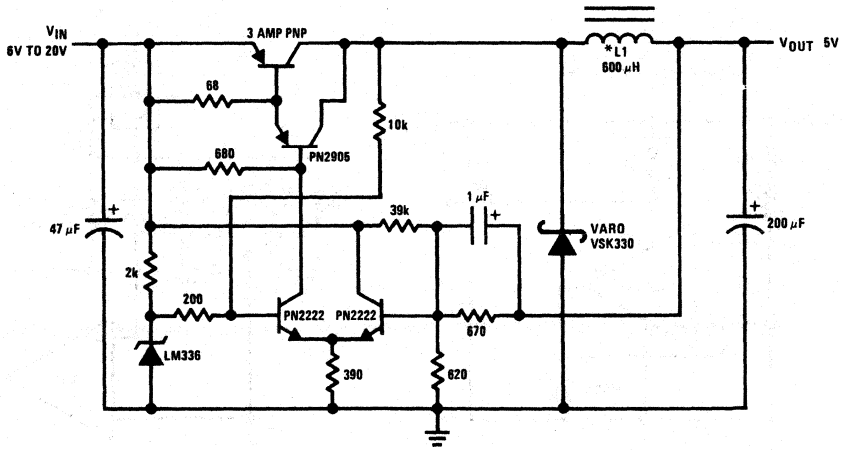


FIGURE 2. Temperature Coefficient Adjustment

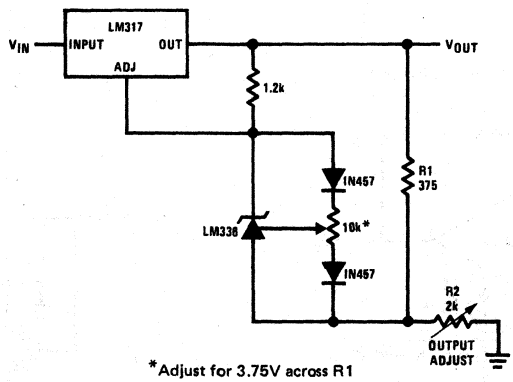
Typical Applications (Continued)

Low Cost 2 Amp Switching Regulator†



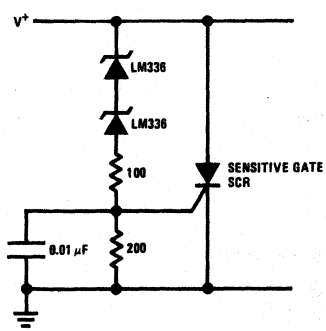
*L1 60 turns #16 wire on Arnold Core A-254168-2
†Efficiency ≈ 80%

Precision Power Regulator with Low Temperature Coefficient

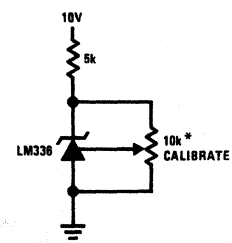


*Adjust for 3.75V across R1

5V Crowbar



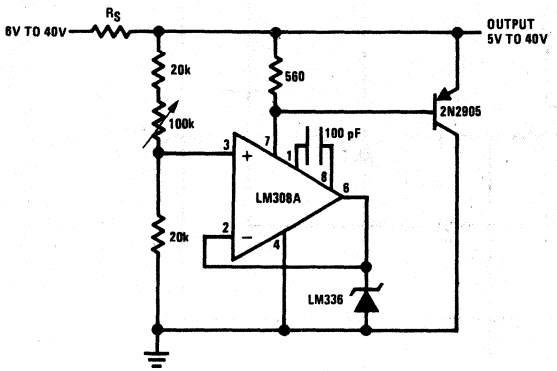
Trimmed 2.5V Reference with Temperature Coefficient Independent of Breakdown Voltage



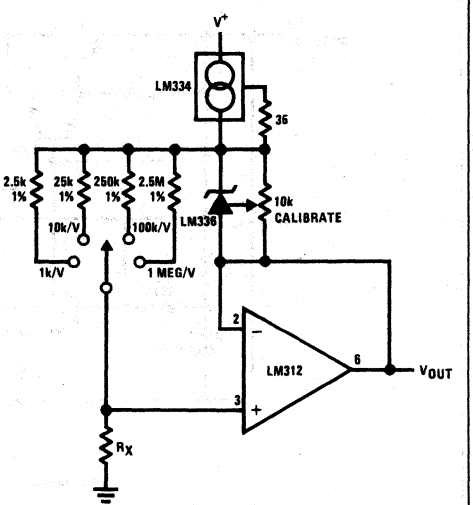
*Does not affect temperature coefficient

Typical Applications (Continued)

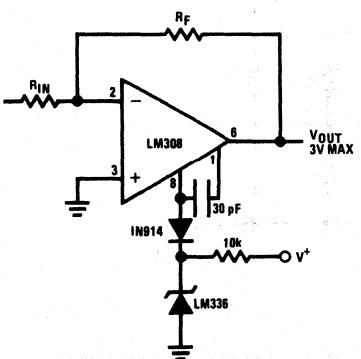
Adjustable Shunt Regulator



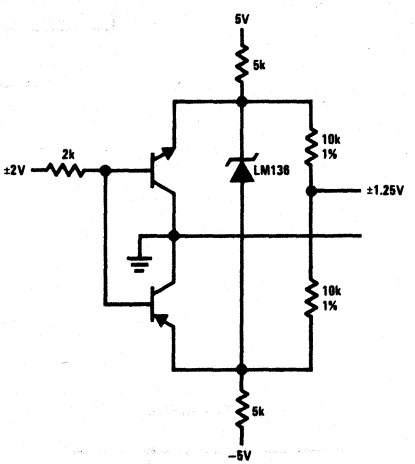
Linear Ohmmeter



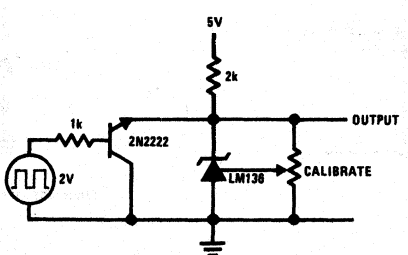
Op Amp with Output Clamped



Bipolar Output Reference

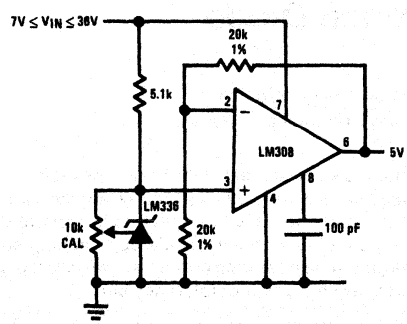


2.5V Square Wave Calibrator

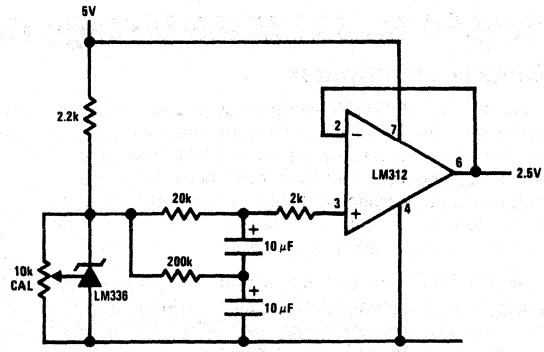


Typical Applications (Continued)

5V Buffered Reference

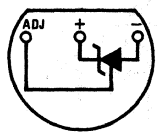


Low Noise Buffered Reference



Connection Diagrams

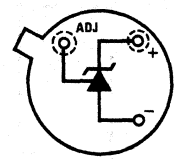
TO-92
Plastic Package



BOTTOM VIEW

Order Number
LM336Z or LM336BZ
See NS Package Z03A

TO-46
Metal Can Package



BOTTOM VIEW

Order Number
LM136H, LM236H, LM336H, LM136AH,
LM236AH or LM336BH
See NS Package H03H

National Semiconductor

LM185/LM285/LM385 Voltage Reference Diode

General Description

The LM185/LM285/LM385 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

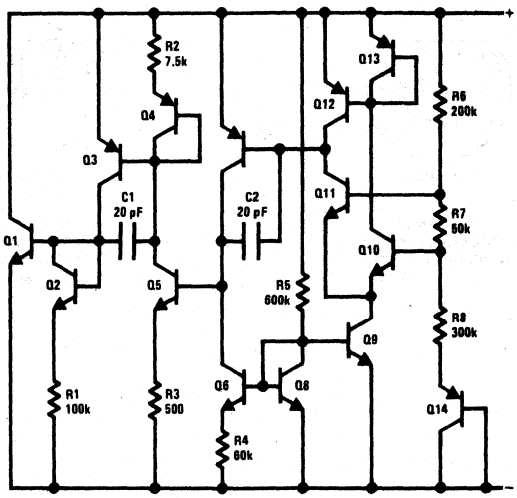
Careful design of the LM185 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation. Some outstanding features are:

- Operating current of 10 μA to 20 mA
- 1% and 2% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient
- Low voltage reference—1.235V

The extremely low power drain of the LM185 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

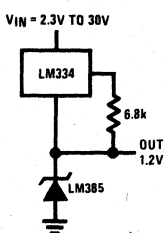
The LM185 is rated for operation over a −55°C to 125°C temperature range while the LM285 is rated −25°C to 85°C and the LM385 0°C to 70°C. The LM185/LM285/LM385 are available in a hermetic TO-46 package and the LM385 is also available in a low-cost TO-92 molded package.

Schematic Diagram

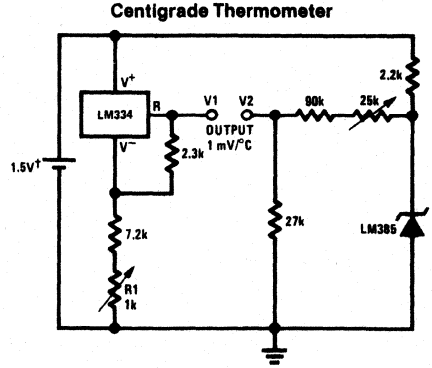


Applications

Wide Input Range Reference



Centigrade Thermometer



Calibration

1. Adjust R1 so that V1 = temp at 1 mV/°K
2. Adjust V2 to 273.2 mV

†I_Q for 1.3V to 1.6V battery voltage = 50 μA to 150 μA

Absolute Maximum Ratings

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range	
LM185	−55°C to +125°C
LM285	−25°C to +85°C
LM385	0°C to 70°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

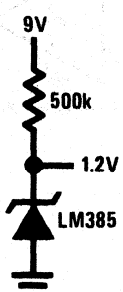
Parameter	Conditions	LM185/LM285			LM385B/LM385			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$ $I_{MIN} \leq I_R \leq 20$ mA							
	LM185/LM285	1.223	1.235	1.247				V
	LM385				1.205	1.235	1.260	V
	LM385B				1.223	1.235	1.247	
Minimum Operating Current			8	10		8	15	μA
Reverse Breakdown Voltage Change with Current	$I_{MIN} \leq I_R \leq 1$ mA			1			1	mV
				1.5			**1.5**	mV
	1 mA $\leq I_R \leq$ 20 mA			10			20	mV
				20			**25**	mV
Reverse Dynamic Impedance	$I_R = 100$ μA		0.2	0.6		0.4	1	Ω
				1.5			**1.5**	Ω
Average Temperature Coefficient	10 μA $\leq I_R \leq$ 20 mA (Note 2)		20			20		ppm/°C
Wide Band Noise (RMS)	$I_R = 100$ μA, 10 Hz $\leq f \leq$ 10 kHz		60			60		μV
Long Term Stability	$I_R = 100$ μA, $T_A = 25°C \pm 0.1°C$		20			20		ppm/kHR

Note 1: Boldface type applies over the operating temperature range. Thermal resistance of the TO-46 package is 440°C/W junction to ambient or 80°C junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient.

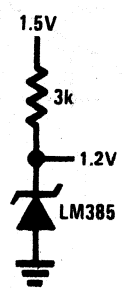
Note 2: Guaranteed maximum average temperature coefficient available as special order.

Applications (Continued)

Micropower Reference from 9V Battery

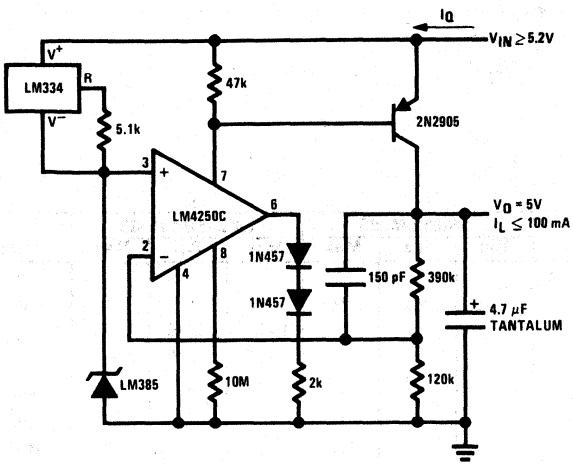


Reference from 1.5V Battery



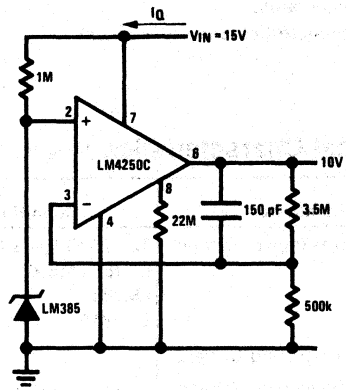
LM385 Applications

Micropower* 5V Regulator



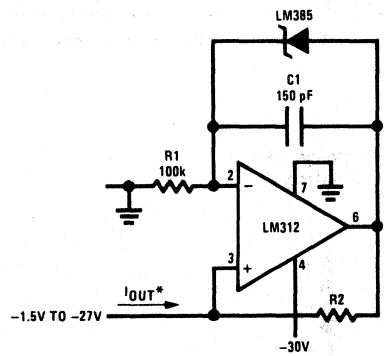
* $I_Q \cong 30$ μA

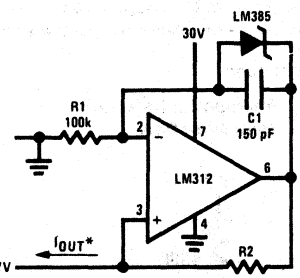
Micropower* 10V Reference



* $I_Q \cong 20$ μA standby current

Precision 1 μA to 1 mA Current Sources



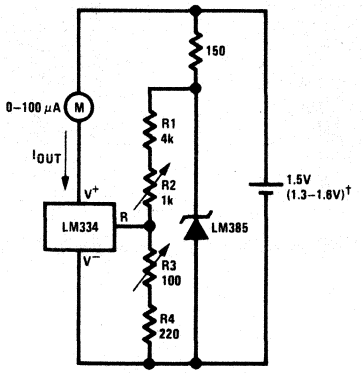


* $I_{OUT} = \frac{1.23V}{R2}$

LM385 Applications (Continued)

METER THERMOMETERS

0°C-100°C Thermometer



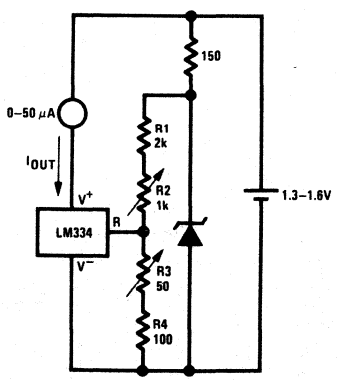
Calibration

1. Short LM385, adjust R3 for I_{OUT} = temp at 1 μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

†I_Q at 1.3V≅500 μA

I_Q at 1.6V ≅2.4 mA

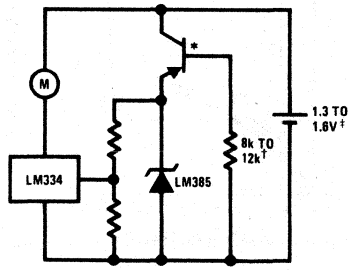
0°F-50°F Thermometer



Calibration

1. Short LM385, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

Lower Power Thermometer

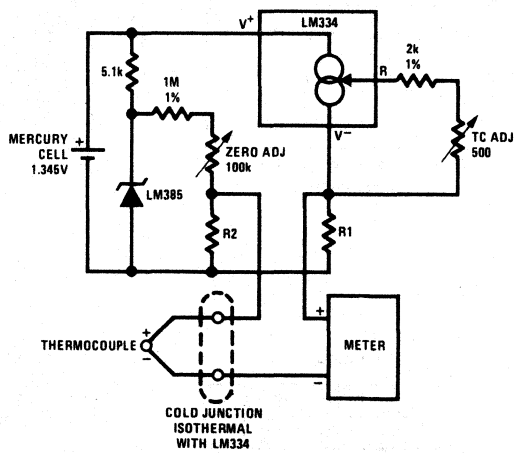


*2N3638 or 2N2907 select for inverse H_{FE}≅5

†Select for operation at 1.3V

‡I_Q≅600 μA to 900 μA

Micropower Thermocouple Cold Junction Compensator



Adjustment Procedure

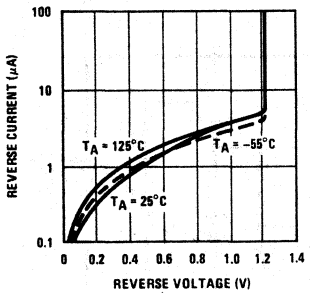
1. Adjust TC ADJ pot until voltage across R1 equals kelvin temperature multiplied by the thermocouple seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple seebeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Coefficient (μV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

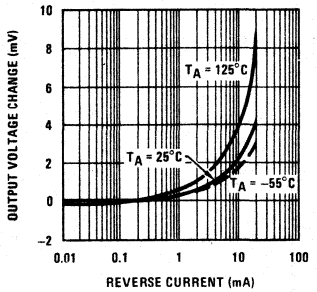
Typical supply current 50 μA

Typical Performance Characteristics

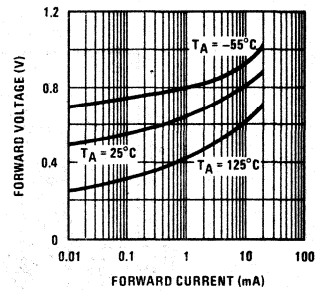
Reverse Characteristics



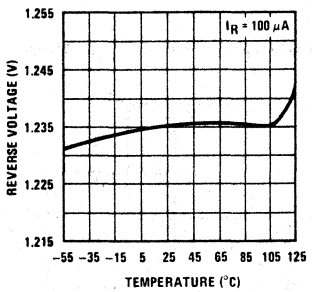
Reverse Characteristics



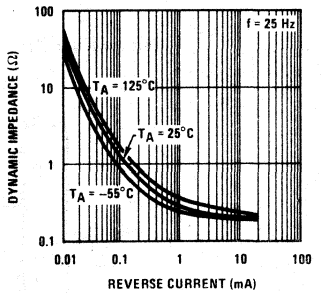
Forward Characteristics



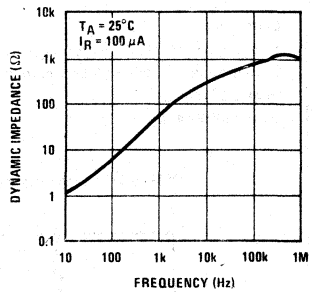
Temperature Drift



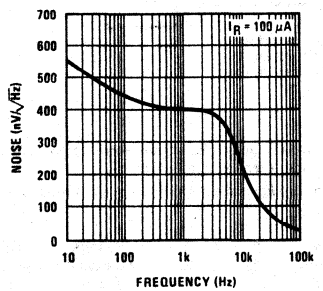
Reverse Dynamic Impedance



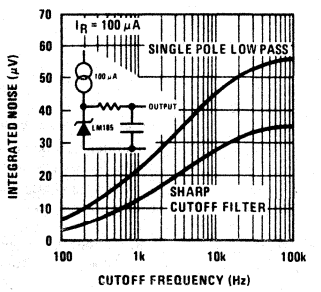
Reverse Dynamic Impedance



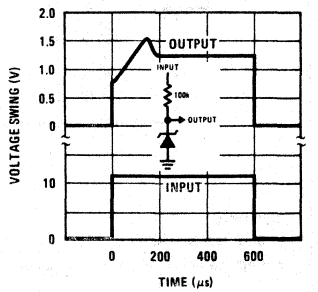
Noise Voltage



Filtered Output Noise

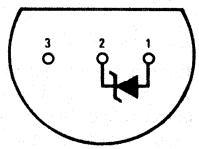


Response Time



Connection Diagrams

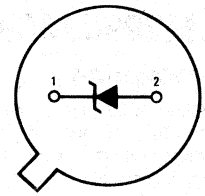
TO-92
Plastic Package



BOTTOM VIEW

Order Number LM385Z or LM385BZ
See NS Package Z03D

TO-46
Metal Can Package



BOTTOM VIEW

Order Number LM185H, LM285H,
LM385H or LM385BH
See NS Package H02A

National Semiconductor

LM199/LM299/LM399 Precision Reference

General Description

The LM199/LM299/LM399 are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

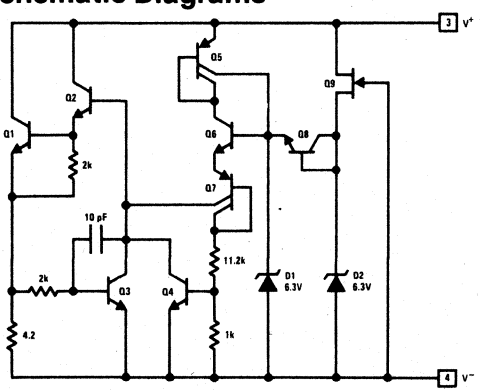
The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299 is rated for operation from −25°C to +85°C and the LM399 is rated from 0°C to +70°C.

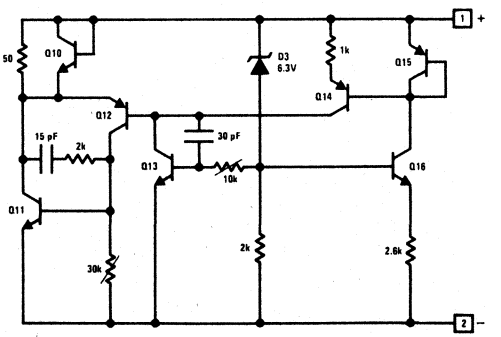
Features

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance – 0.5Ω
- Initial tolerance on breakdown voltage – 2%
- Sharp breakdown at 400μA
- Wide operating current – 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization – 300 mW at 25°C
- Long term stability – 20 ppm

Schematic Diagrams



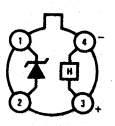
Temperature Stabilizer



Reference

Connection Diagram

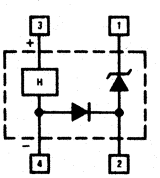
Metal Can Package



TOP VIEW

Order Number LM199H, LM299H or LM399H
See NS Package H04D

Functional Block Diagram



Absolute Maximum Ratings

Temperature Stabilizer Voltage	40V
Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	40V −0.1V
Operating Temperature Range	
LM199	−55°C to +125°C
LM299	−25°C to +85°C
LM399	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM199/LM299			LM399			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	0.5 mA ≤ I_R ≤ 10 mA	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	0.5 mA ≤ I ≤ 10 mA		6	9		6	12	mV
Reverse Dynamic Impedance	I_R = 1 mA		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	−55°C ≤ T_A ≤ 85°C, LM199		0.00003	0.0001				%/°C
	85°C ≤ T_A ≤ 125°C, LM199		0.0005	0.0015				%/°C
	−25°C ≤ T_A ≤ 85°C, LM299		0.00003	0.0001				%/°C
	0°C ≤ T_A ≤ 70°C, LM399					0.00003	0.0002	%/°C
RMS Noise	10 Hz ≤ f ≤ 10 kHz		7	20		7	50	μV
Long Term Stability	Stabilized, 22°C ≤ T_A ≤ 28°C, 1000 Hours, I_R = 1 mA ±0.1%		20			20		ppm
Temperature Stabilizer Supply Current	T_A = 25°C, Still Air, V_S = 30V		8.5	14		8.5	15	mA
	T_A = −55°C		22	28				
Temperature Stabilizer Supply Voltage	(Note 3)	9		40	9		40	V
Warm-Up Time to 0.05%	V_S = 30V, T_A = 25°C		3			3		Seconds
Initial Turn-on Current	9 ≤ V_S ≤ 40, T_A = 25°C, (Note 3)		140	200		140	200	mA

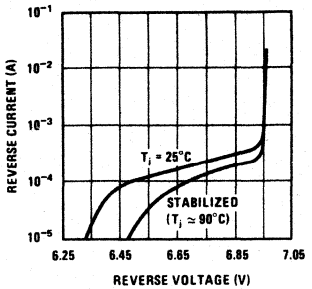
Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and −55°C ≤ T_A ≤ +125°C for the LM199; −25°C ≤ T_A ≤ +85°C for the LM299 and 0°C ≤ T_A ≤ +70°C for the LM399.

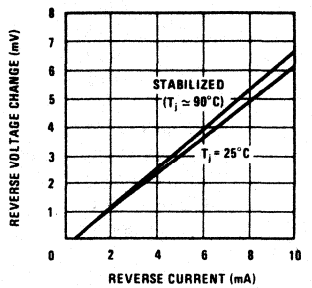
Note 3: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

Typical Performance Characteristics

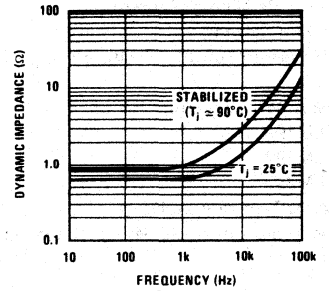
Reverse Characteristics



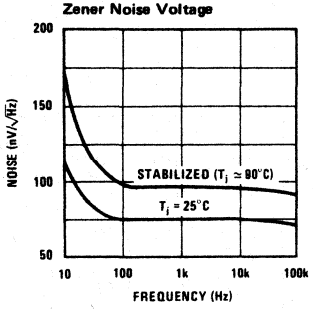
Reverse Voltage Change



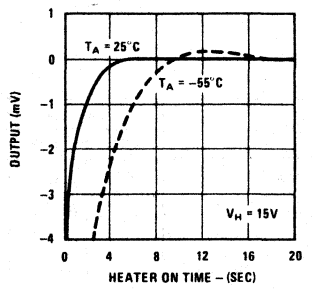
Dynamic Impedance



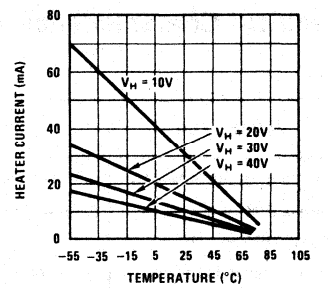
Zener Noise Voltage



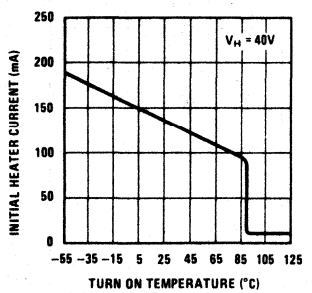
Stabilization Time



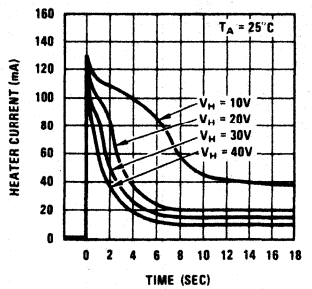
Heater Current



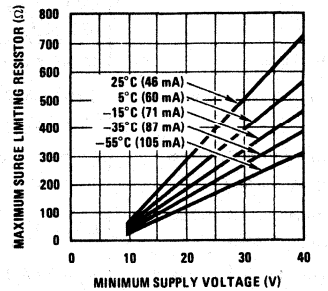
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)

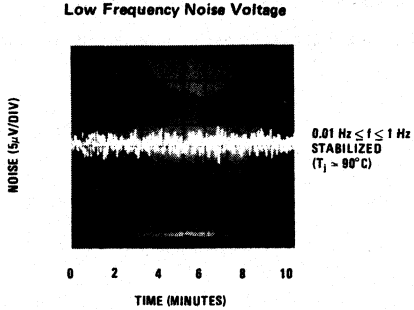


Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures

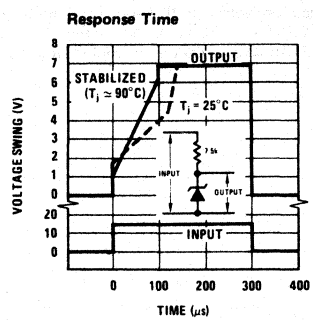


*Heater must be bypassed with a 2 μF or larger tantalum capacitor if maximum value resistors are used. Otherwise, 30% to 50% smaller values must be used. If heater oscillates, resistor value may be too small.

Low Frequency Noise Voltage

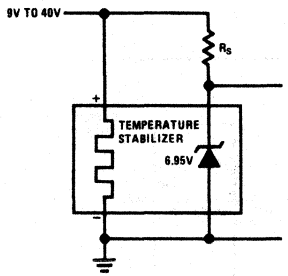


Response Time

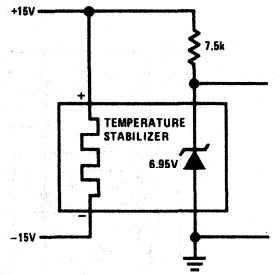


Typical Applications

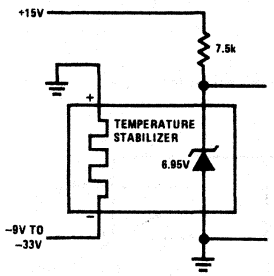
Single Supply Operation



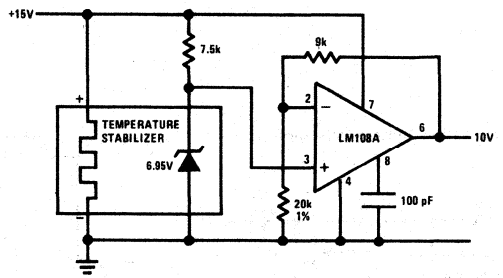
Split Supply Operation



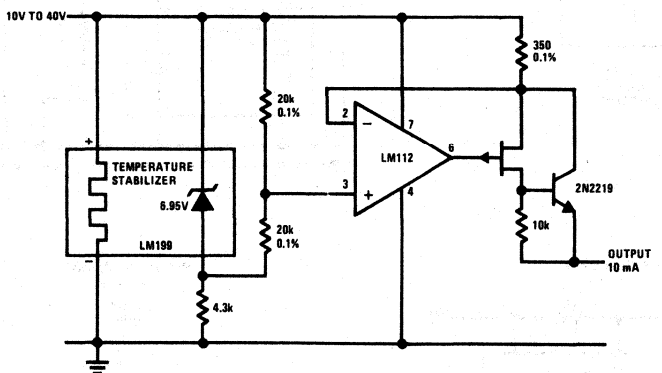
Negative Heater Supply with Positive Reference



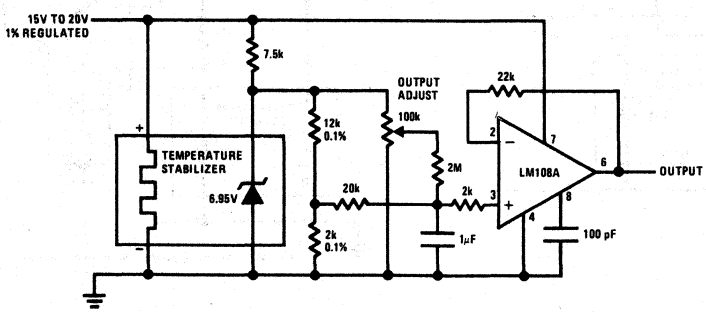
Buffered Reference With Single Supply



Positive Current Source

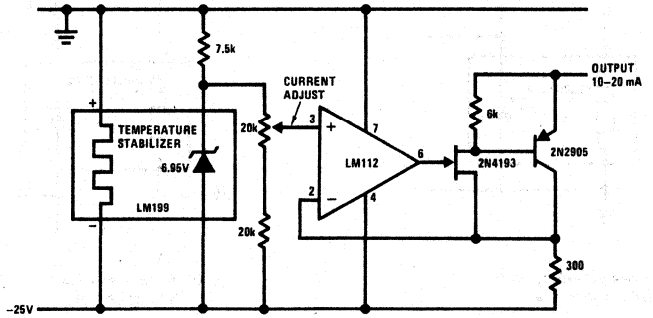


Standard Cell Replacement

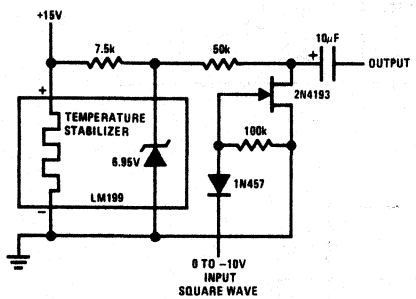


Typical Applications (Continued)

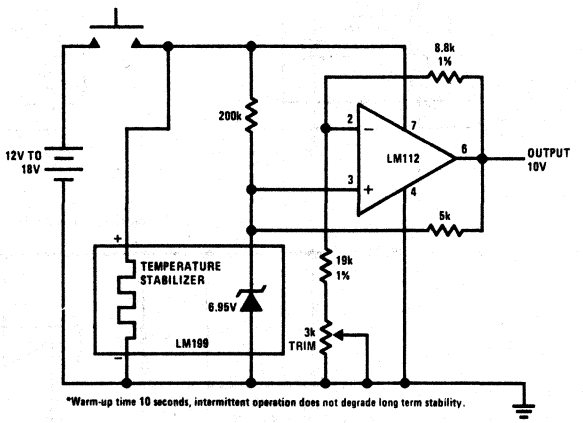
Negative Current Source



Square Wave Voltage Reference

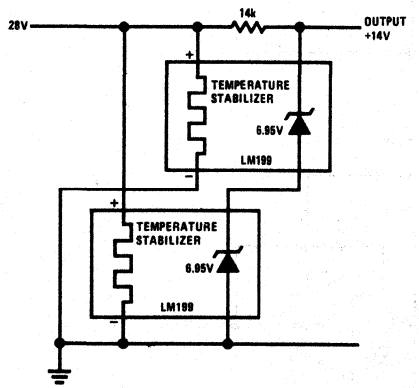


Portable Calibrator*

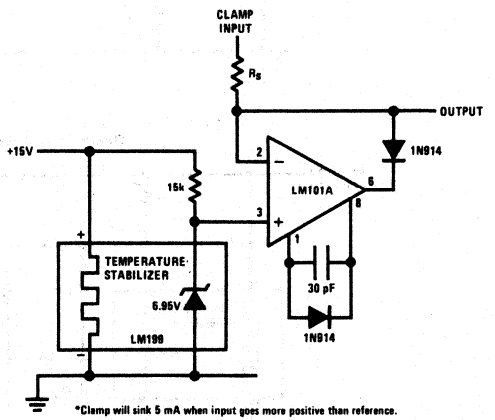


*Warm-up time 10 seconds, intermittent operation does not degrade long term stability.

14V Reference



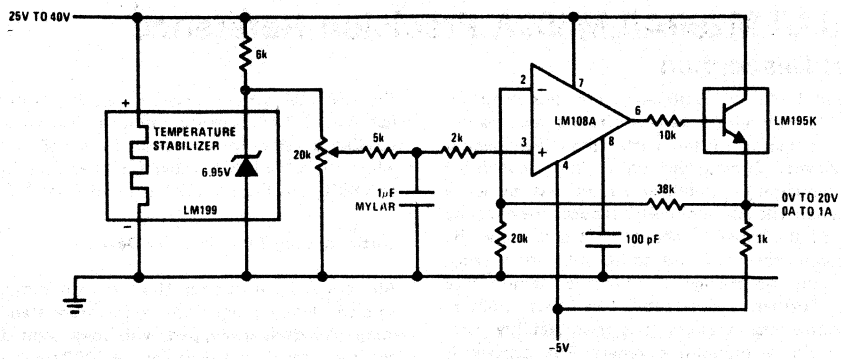
Precision Clamp*



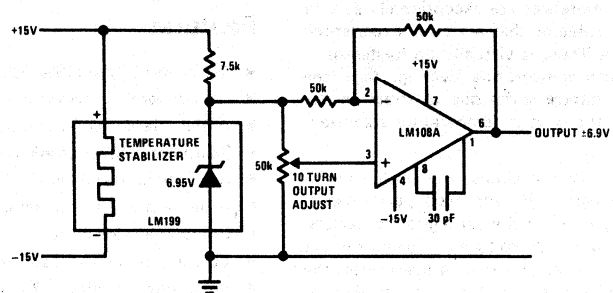
*Clamp will sink 5 mA when input goes more positive than reference.

Typical Applications (Continued)

0V to 20V Power Reference



Bipolar Output Reference



National Semiconductor

LM199A/LM299A/LM399A Precision Reference

General Description

The LM199A/LM299A/LM399A are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199A series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199A is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

The LM199A can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199A can replace references in existing equipment with a minimum of wiring changes.

The LM199A series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299A is rated for operation from −25°C to +85°C and the LM399A is rated from 0°C to +70°C.

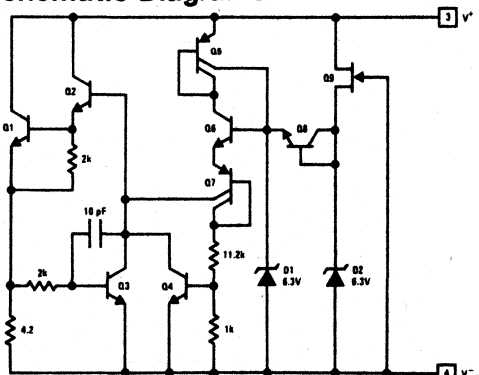
Certified Long Term Stability Devices

All devices are tested for 1000 hours minimum at 25°C ambient temperature with temperature stabilizer operating. All devices shipped with long term data which certifies a maximum drift for the 1000 hours of 20 ppm or 50 ppm.

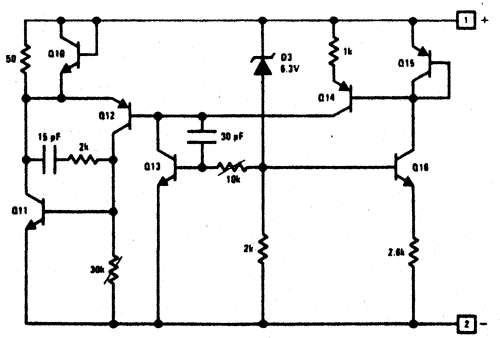
Features

- Guaranteed 0.00005%/°C temperature coefficient
- Low dynamic impedance – 0.5Ω
- Initial tolerance on breakdown voltage – 2%
- Sharp breakdown at 400μA
- Wide operating current – 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization – 300 mW at 25°C
- Long term stability – 20 ppm
- Certified long term stability available

Schematic Diagrams



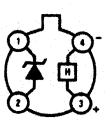
Temperature Stabilizer



Reference

Connection Diagram

Metal Can Package



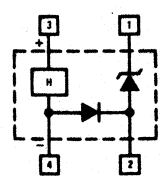
TOP VIEW

Order Number LM199AH, LM299AH or LM399AH
See NS Package H04D

Certified Long Term Stability Device

CERTIFIED LONG TERM STABILITY ppm MAX	ORDERING NUMBERS
20	LM199AH-20
20	LM299AH-20
50	LM399AH-50

Functional Block Diagram



Absolute Maximum Ratings

Temperature Stabilizer Voltage	40V
Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	+40V −0.1V
Operating Temperature Range	
LM199A	−55°C to +125°C
LM299A	−25°C to +85°C
LM399A	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS		LM199A, LM299A			LM399A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	0.5 mA ≤ I_R ≤ 10 mA		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	0.5 mA ≤ I_R ≤ 10 mA			6	9		6	12	mV
Reverse Dynamic Impedance	I_R = 1 mA			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	−55°C ≤ T_A ≤ 85°C 85°C ≤ T_A ≤ 125°C	LM199A		0.00002 0.0005	0.00005 0.0010				%/°C %/°C
	−25°C ≤ T_A ≤ 85°C	LM299A		0.00002	0.00005				%/°C
	0°C ≤ T_A ≤ 70°C	LM399A					0.00003	0.0001	%/°C
RMS Noise	10 Hz ≤ f ≤ 10 kHz			7	20		7	50	μV
Long Term Stability	Stabilized, 22°C ≤ T_A ≤ 28°C, 1000 Hours, I_R = 1 mA ±0.1%			20			20		ppm
Temperature Stabilizer Supply Current	T_A = 25°C, Still Air, V_S = 30V T_A = −55°C			8.5 22	14 28		8.5	15	mA
Temperature Stabilizer Supply Voltage (Note 3)			9		40	9		40	V
Warm-Up Time to 0.05%	V_S = 30V, T_A = 25°C			3			3		Seconds
Initial Turn-on Current	9 ≤ V_S ≤ 40, T_A = 25°C, (Note 3)			140	200		140	200	mA

Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and −55°C ≤ T_A ≤ +125°C for the LM199A; −25°C ≤ T_A ≤ +85°C for the LM299A and 0°C ≤ T_A ≤ +70°C for the LM399A.

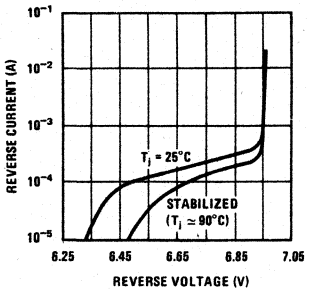
Note 3: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

Typical Applications

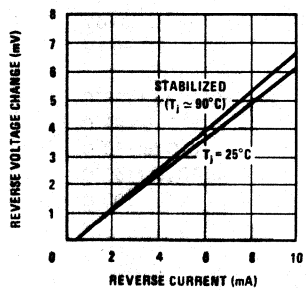
For typical applications, see LM199 data sheet on preceding pages.

Typical Performance Characteristics

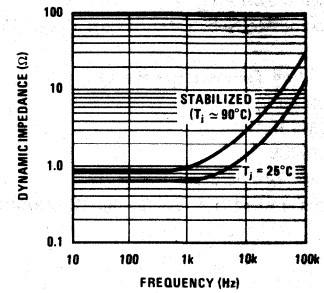
Reverse Characteristics



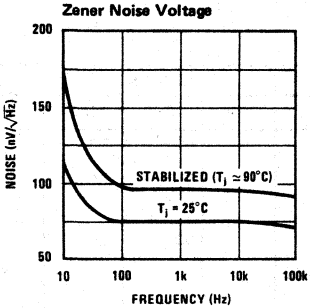
Reverse Voltage Change



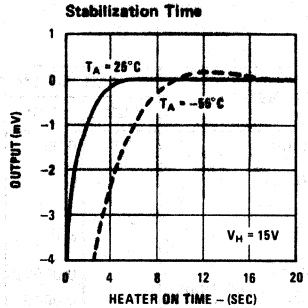
Dynamic Impedance



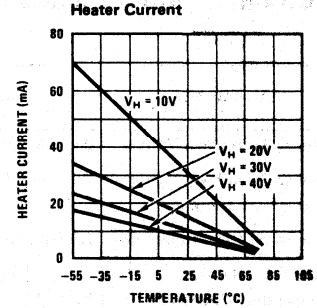
Zener Noise Voltage



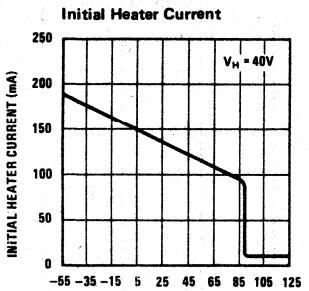
Stabilization Time



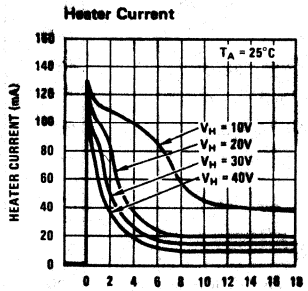
Heater Current



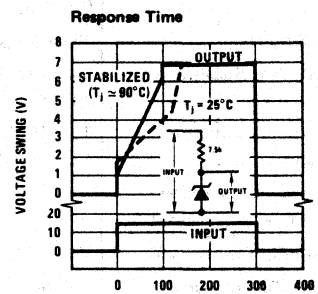
Initial Heater Current



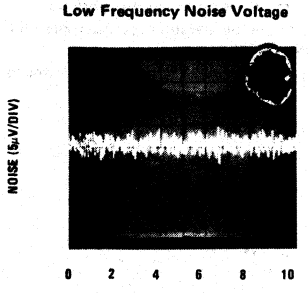
Heater Current



Response Time



Low Frequency Noise Voltage



0.01 Hz ≤ f ≤ 1 Hz
STABILIZED
($T_j \simeq$ 90°C)

National Semiconductor

LM3999 Precision Reference

General Description

The LM3999 is a precision, temperature-stabilized monolithic zener offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners.

The LM3999 reference is exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM3999 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

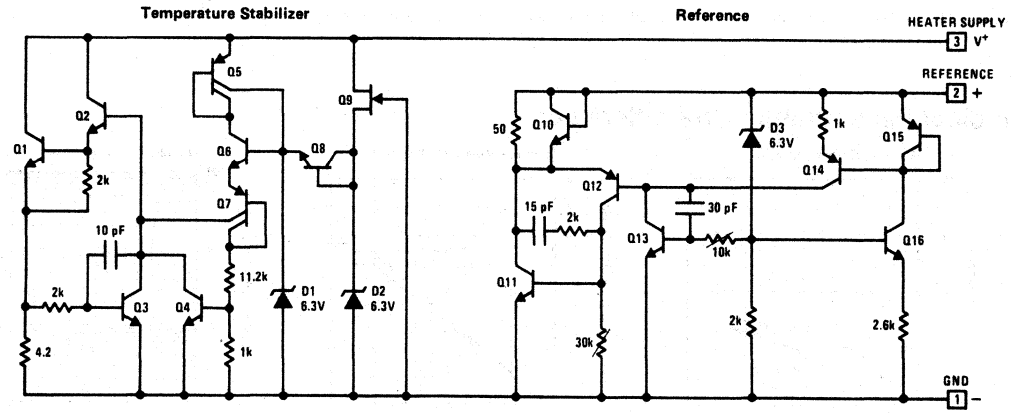
The LM3999 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, precision voltage or current sources or precision power supplies. Further, in many cases, the LM3999 can replace references in existing equipment with a minimum of wiring changes.

The LM3999 is packaged in a standard TO-92 package and is rated from 0°C to +70°C.

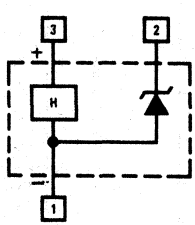
Features

- Guaranteed 0.0005%/°C temperature coefficient
- Low dynamic impedance – 0.5Ω
- Initial tolerance on breakdown voltage – 5%
- Sharp breakdown at 400μA
- Wide operating current – 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Low power for stabilization – 400 mW at 25°C
- Long term stability – 20 ppm

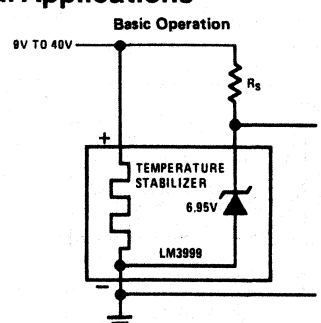
Schematic Diagram



Functional Block Diagram



Typical Applications



Absolute Maximum Ratings

Temperature Stabilizer Voltage	36V
Reverse Breakdown Current	20 mA
Forward Current	0.1 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

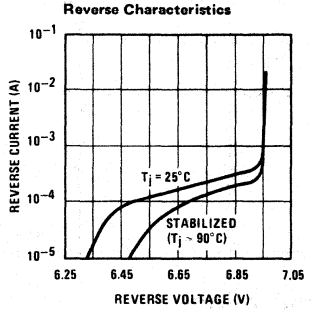
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	$0.6\ mA \leq I_R \leq 10\ mA$	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.6\ mA \leq I \leq 10\ mA$		6	20	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.6	2.2	Ω
Reverse Breakdown Temperature Coefficient	$0°C \leq T_A \leq 70°C$		0.0002	0.0005	%/°C
RMS Noise	$10\ Hz \leq f \leq 10\ kHz$		7		μV
Long Term Stability	Stabilized, $22°C \leq T_A \leq 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20		ppm
Temperature Stabilizer	$T_A = 25°C$, Still Air, $V_S = 30V$		12	18	mA
Temperature Stabilizer Supply Voltage				36	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		5		Seconds
Initial Turn-on Current	$9 \leq V_S \leq 40$, $T_A = 25°C$		140	200	mA

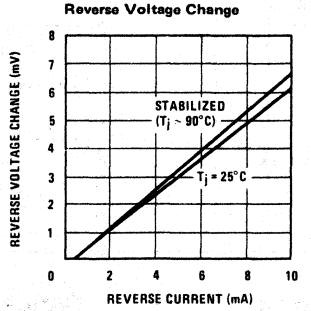
Note 1: These specifications apply for 30V applied to the temperature stabilizer and $0°C \leq T_A \leq +70°C$.

Typical Performance Characteristics

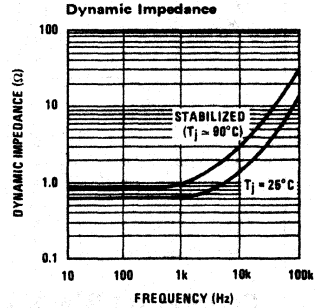
Reverse Characteristics



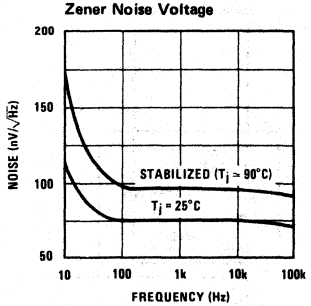
Reverse Voltage Change



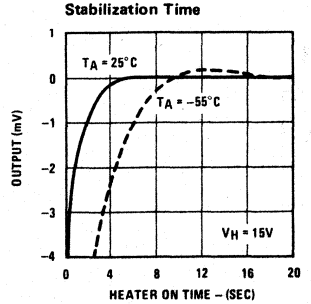
Dynamic Impedance



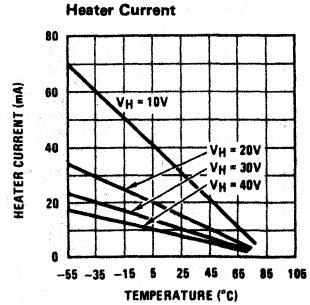
Zener Noise Voltage



Stabilization Time

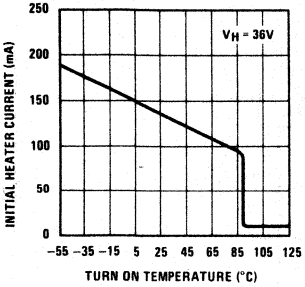


Heater Current

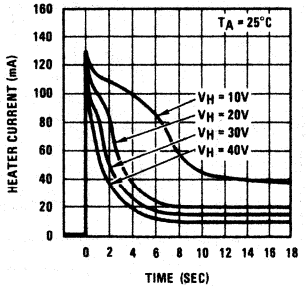


Typical Performance Characteristics (Continued)

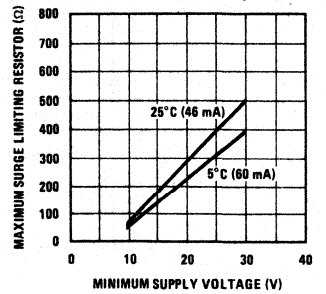
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)

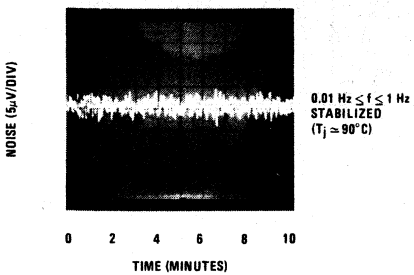


Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures

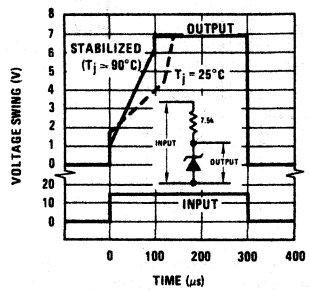


*Heater must be bypassed with a 2 μF tantalum capacitor if maximum value resistors are used. Otherwise 30% to 50% smaller values must be used.If heater voltage oscillates under any condition, temperature is not at control point.

Low Frequency Noise Voltage

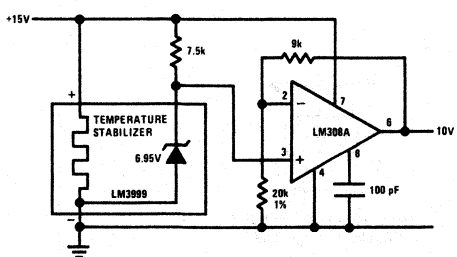


Response Time

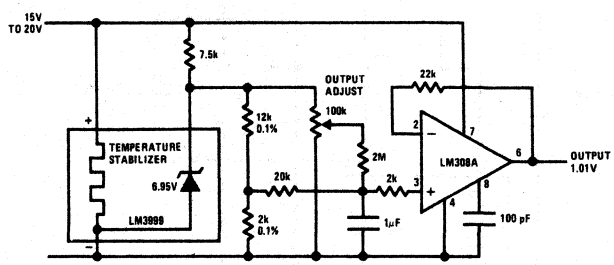


Typical Applications (Continued)

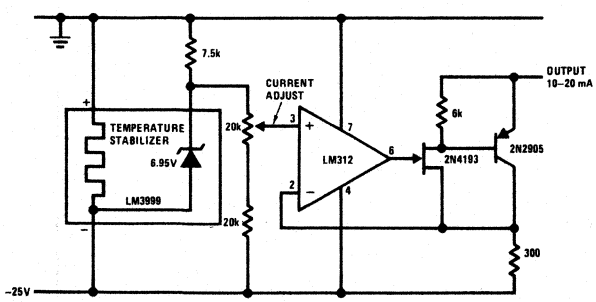
Buffered Reference With Single Supply



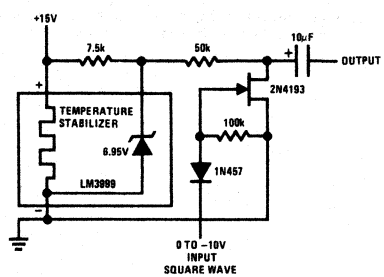
Voltage Reference



Negative Current Source

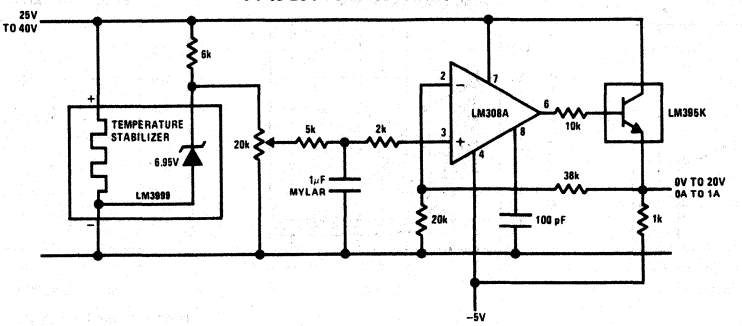


Square Wave Voltage Reference

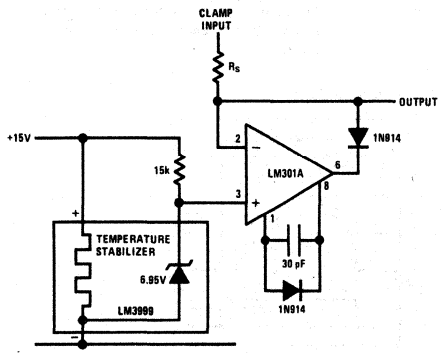


Typical Applications (Continued)

0V to 20V Power Reference

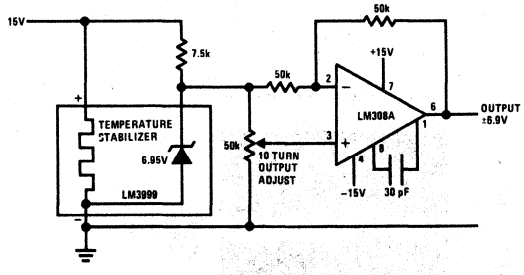


Precision Clamp*

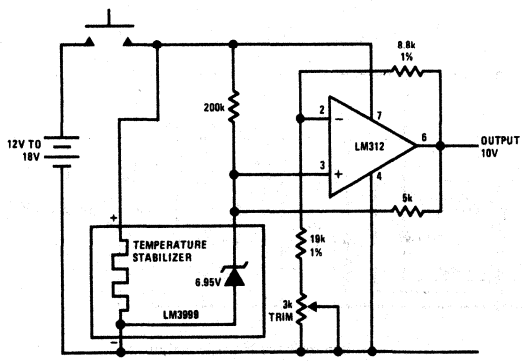


*Clamp will sink 5 mA when input goes more positive than reference.

Bipolar Output Reference



Portable Calibrator*



*Warm-up time 10 seconds; intermittent operation does not degrade long term stability.

Connection Diagram

Plastic Package

BOTTOM VIEW

Order Number LM3999Z
See NS Package Z03A

Section 15

Applications

15

Section Contents

Specifying A/D and D/A Converters

National Semiconductor
Application Note 156
Jim Sherwin
February 1976

The specification or selection of analog-to-digital (A/D) or digital-to-analog (D/A) converters can be a chancey thing unless the specifications are understood by the person making the selection. Of course, you know you want an accurate converter of specific resolution; but how do you insure that you get what you want? For example, 12 switches, 12 arbitrarily valued resistors, and a reference will produce a 12-bit DAC exhibiting 12 quantum steps of output voltage. In all probability, the user wants something better than the expected performance of such a DAC. Specifying a 12-bit DAC or an ADC must be made with a full understanding of accuracy, linearity, differential linearity, monotonicity, scale, gain, offset, and hysteresis errors.

This note explains the meanings of and the relationships between the various specifications encountered in A/D and D/A converter descriptions. It is intended that the meanings be presented in the simplest and clearest practical terms. Included are transfer curves showing the several types of errors discussed. Timing and control signals and several binary codes are described as they relate to A/D and D/A converters.

MEANING OF PERFORMANCE SPECS

Resolution describes the smallest standard incremental change in output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between one code change and the next adjacent code change. A converter with n switches can resolve 1 part in 2^n. The least significant increment is then 2^{-n}, or one least significant bit (LSB). In contrast, the most significant bit (MSB) carries a weight of 2^{-1}. Resolution applies to DACs and ADCs, and may be expressed in percent of full scale or in binary bits. For example, an ADC with 12-bit resolution could resolve 1 part in 2^{12} (1 part in 4096) or 0.0245% of full scale. A converter with 10V full scale could resolve a 2.45mV input change. Likewise, a 12-bit DAC would exhibit an output voltage change of 0.0245% of full scale when the binary input code is incremented one binary bit (1 LSB). Resolution is a design parameter rather than a performance specification; it says nothing about accuracy or linearity.

Accuracy is sometimes considered to be a non-specific term when applied to D/A or A/D converters. A linearity spec is generally considered as more descriptive. An accuracy specification describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors. A 12-bit DAC could not have a conversion accuracy better than ±½ LSB or ±1 part in 2^{12+1} (±0.0122% of full scale due to finite resolution). This would be the case in figure 1 if there were no errors. Actually, ±0.0122% FS represents a deviation from 100% accuracy; therefore accuracy should be specified as 99.9878%. However, convention would dictate 0.0122% as being an accuracy spec rather than an inaccuracy (tolerance or error) spec.

Accuracy as applied to an ADC would describe the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. If a 12-bit ADC is stated to be ±1 LSB accurate, this is equivalent to ±0.0245% or twice the minimum possible quantizing error of 0.0122%. An accuracy spec describes the maximum sum of all errors including quantizing error, but is rarely provided on data sheets as the several errors are listed separately.

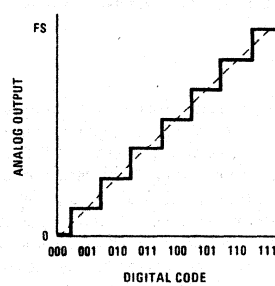


FIGURE 1. Linear DAC Transfer Curve Showing Minimum Resolution Error and Best Possible Accuracy

Quantizing Error is the maximum deviation from a straight line transfer function of a perfect ADC. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution ADC would exhibit zero quantizing error. A perfect ADC, suitably offset ½ LSB at zero scale as shown in figure 2, exhibits only ±½ LSB maximum output error. If not offset, the error will be ± 1 LSB as shown in figure 3. For example, a perfect 12-bit ADC will show a ±½ LSB error of ±0.0122% while the quantizing error of an 8-bit ADC is ±½ part in 2^8 or ±0.195% of full scale. Quantizing error is not strictly applicable to a DAC; the equivalent effect is more properly a resolution error.

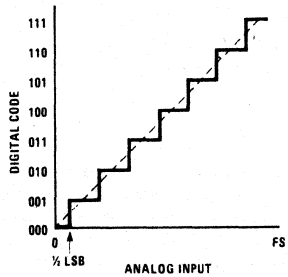


FIGURE 2. ADC Transfer Curve, ½ LSB Offset at Zero

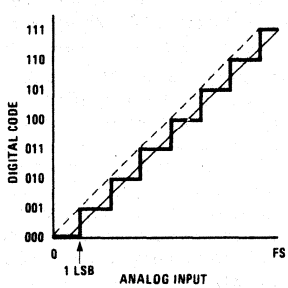


FIGURE 3. ADC Transfer Curve, No Offset

Scale Error (full scale error) is the departure from design output voltage of a DAC for a given input code, usually full-scale code. (See figure 4.) In an ADC it is the departure of actual input voltage from design input voltage for a full-scale output code. Scale errors can be caused by errors in reference voltage, ladder resistor values, or amplifier gain, *et. al.* (See **Temperature Coefficient.**) Scale errors may be corrected by adjusting output amplifier gain or reference voltage. If the transfer curve resembles that of figure 7, a scale adjustment at ¾ scale could improve the overall ± accuracy compared to an adjustment at full scale.

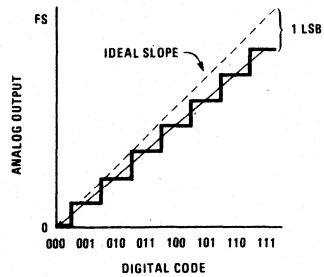


FIGURE 4. Linear, 1 LSB Scale Error

Gain Error is essentially the same as scale error for an ADC. In the case of a DAC with current and voltage mode outputs, the current output could be to scale while the voltage output could exhibit a gain error. The amplifier feedback resistors would be trimmed to correct the gain error.

Offset Error (zero error) is the output voltage of a DAC with zero code input, or it is the required mean value of input voltage of an ADC to set zero code out. (See figure 5.) Offset error is usually caused by amplifier or comparator input offset voltage or current; it can usually be trimmed to zero with an offset zero adjust potentiometer external to the DAC or ADC. Offset error may be expressed in % FS or in fractional LSB.

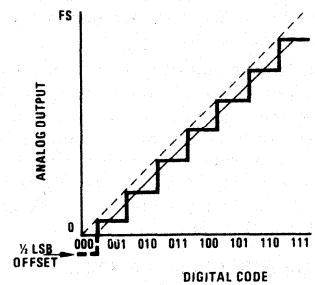


FIGURE 5. Linear, ½ LSB Offset Error

Hysteresis Error in an ADC causes the voltage at which a code transition occurs to be dependent upon the direction from which the transition is approached. This is usually caused by hysteresis in the comparator inside an ADC. Excessive hysteresis may be reduced by design; however, some slight hysteresis is inevitable and may be objectionable in converters if hysteresis approaches ½ LSB.

Linearity, or, more accurately, non-linearity specifications describe the departure from a linear transfer curve for either an ADC or a DAC. Linearity error does not include quantizing, zero, or scale errors. Thus, a specifi-

cation of ±½ LSB linearity implies error in addition to the inherent ±½ LSB quantizing or resolution error. In reference to figure 2, showing no errors other than quantizing error, a linearity error allows for one or more of the steps being greater or less than the ideal shown.

Figure 6 shows a 3-bit DAC transfer curve with no more than ±½ LSB non-linearity, yet one step shown is of zero amplitude. This is within the specification, as the maximum deviation from the ideal straight line is ±1 LSB (½ LSB resolution error plus ½ LSB non-linearity). With any linearity error, there is a differential non-linearity (see below). A ±½ LSB linearity spec guarantees monotonicity (see below) and ⩽ ±1 LSB differential non-linearity (see below). In the example of figure 6, the code transition from 100 to 101 is the worst possible non-linearity, being the transition from 1 LSB high at code 100 to 1 LSB low at 110. Any fractional non-linearity beyond ±½ LSB will allow for a non-monotonic transfer curve. Figure 7 shows a typical non-linear curve; non-linearity is 1¼ LSB yet the curve is smooth and monotonic.

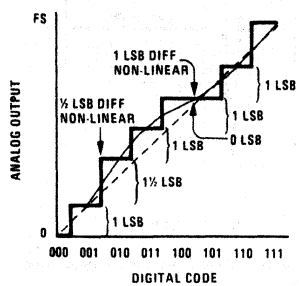


FIGURE 6. ±½ LSB Non-Linearity (Implies 1 LSB Possible Error), 1 LSB Differential Non-Linearity (Implies Monotonicity)

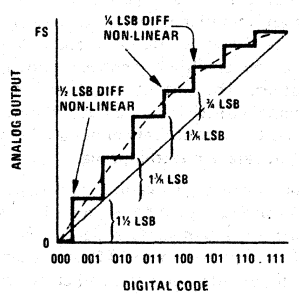


FIGURE 7. 1¼ LSB Non-Linear, ½ LSB Differential Non-Linearity

Linearity specs refer to either ADCs or to DACs, and do not include quantizing, gain, offset, or scale errors. Linearity errors are of prime importance along with differential linearity in either ADC or DAC specs, as all other errors (except quantizing, and temperature and long-term drifts) may be adjusted to zero. Linearity errors may be expressed in % FS or fractional LSB.

Differential Non-Linearity indicates the difference between actual analog voltage change and the ideal (1 LSB) voltage change at any code change of a DAC. For example, a DAC with a 1.5 LSB step at a code change would be said to exhibit ½ LSB differential non-linearity (see figures 6 and 7). Differential non-linearity may be expressed in fractional bits or in % FS.

Differential linearity specs are just as important as linearity specs because the apparent quality of a converter curve can be significantly affected by differential non-linearity even though the linearity spec is good. Figure 6 shows a curve with a ±½ LSB linearity and ±1 LSB differential non-linearity while figure 7 shows a curve with +1¼ LSB linearity and ±½ LSB differential non-linearity. In many user applications, the curve of figure 7 would be preferred over that of figure 6 because the curve is smoother. The differential non-linearity spec describes the smoothness of a curve; therefore it is of great importance to the user. A gross example of differential non-linearity is shown in figure 8 where the linearity spec is ±1 LSB and the differential linearity spec is ±2 LSB. The effect is to allow a transfer curve with grossly degraded resolution; the normal 8-step curve is reduced to 3 steps in figure 8. Similarly, a 16-step curve (4-bit converter) with only 2 LSB differential non-linearity could be reduced to 6 steps (a 2.6-bit converter?). The real message is, "Beware of the specs." Do not ignore or omit differential linearity characteristics on a converter unless the linearity spec is tight enough to guarantee the desired differential linearity. As this characteristic is impractical to measure on a production basis, it is rarely, if ever, specified, and linearity is the primary specified parameter. Differential non-linearity can always be as much as twice the non-linearity, but no more.

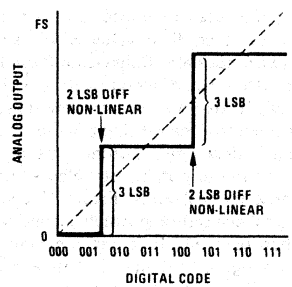


FIGURE 8. ±1 LSB Linear, ±2 LSB Differential Non-Linear

Monotonicity. A monotonic curve has no change in sign of the slope; thus all incremental elements of a monotonically increasing curve will have positive or zero, but never negative slope. The converse is true for decreasing curves. The transfer curve of a monotonic DAC will contain steps of only positive or zero height, and no negative steps. Thus a smooth line connecting all output voltage points will contain no peaks or dips. The transfer function of a monotonic ADC will provide no decreasing output code for increasing input voltage.

Figure 9 shows a non-monotonic DAC transfer curve. For the curve to be non-monotonic, the linearity error must exceed ±½ LSB no matter by how little. The greater the linearity error, the more significant the negative step might be. A non-monotonic curve may not be a special disadvantage in some systems; however, it is a disaster in closed-loop servo systems of any type (including a DAC-controlled ADC). A ±½ LSB maximum linearity spec on an n-bit converter guarantees monotonicity to n bits. A converter exhibiting more than ±½ LSB non-linearity may be monotonic, but is not necessarily monotonic. For example, a 12-bit DAC with ±½ bit linearity to 10 bits (not ±½ LSB) will be monotonic at 10 bits but may or may not be monotonic at 12 bits unless tested and guaranteed to be 12-bit monotonic.

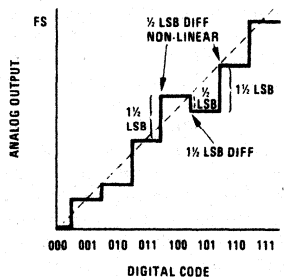
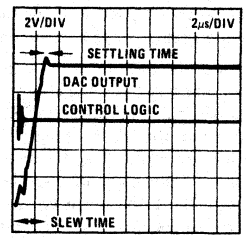
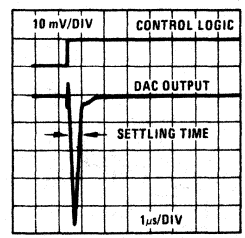


FIGURE 9. Non-Monotonic (Must be > ±½ LSB Non-Linear)



(a) Full-Scale Step



(b) 1 LSB Step

FIGURE 10. DAC Slew and Settling Time

Settling Time is the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±½ LSB. (See also **Conversion Rate** below.) Settling time is often listed along with a slew rate specification; if so, it may not include slew time. If no slew rate spec is included, the settling time spec must be expected to include slew time. Settling time is usually summed with slew time to obtain total elapsed time for the output to settle to final value. Figure 10 delineates that part of the total elapsed time which is considered to be slew and that part which is settling time. It is apparent from this figure that the total time is greater for a major than for a minor code change due to amplifier slew limitations, but settling time may also be different depending upon amplifier overload recovery characteristics.

Slew Rate is an inherent limitation of the output amplifier in a DAC which limits the rate of change of output voltage after code transitions. Slew rate is usually anywhere from 0.2 to several hundred volts/μs. Delay in reaching final value of DAC output voltage is the sum of slew time and settling time as shown in figure 10.

Overshoot and Glitches occur whenever a code transition occurs in a DAC. There are two causes. The current output of a DAC contains switching glitches due to possible asynchronous switching of the bit currents (expected to be worst at half-scale transition when all bits are switched). These glitches are normally of extremely short duration but could be of ½ scale amplitude. The current switching glitches are generally somewhat attenuated at the voltage output of the DAC because the output amplifier is unable to slew at a very high rate; they are, however, partially coupled around the amplifier via the amplifier feedback network and seen at the output. The output amplifier introduces overshoot and some non-critically damped ringing which may be minimized but not entirely eliminated except at the expense of slew rate and settling time.

Temperature Coefficient of the various components of a DAC or ADC can produce or increase any of the several errors as the operating temperature varies. Zero scale offset error can change due to the TC of the amplifier and comparator input offset voltages and currents. Scale error can occur due to shifts in the reference, changes in ladder resistance or non-compensating RC product shifts in dual-slope ADCs, changes in beta or reference current in current switches, changes in amplifier bias current, or drift in amplifier gain-set resistors. Linearity and monotonicity of the DAC can be affected by differential temperature drifts of the ladder resistors and switches. Overshoot, settling time, and slew rate can be affected by temperature due to internal change in amplifier gain and bandwidth. In short, every specification except resolution and quantizing error can be affected by temperature changes.

Long-Term Drift, due mainly to resistor and semiconductor aging can affect all those characteristics which temperature change can affect. Characteristics most commonly affected are linearity, monotonicity, scale, and offset. Scale change due to reference aging is usually the most important change.

Supply Rejection relates to the ability of a DAC or ADC to maintain scale, offset, TC, slew rate, and linearity when the supply voltage is varied. The reference must, of course, remain constant unless considering a multiplying DAC. Most affected are current sources (affecting linearity and scale) and amplifiers or comparators (affecting offset and slew rate). Supply rejection is usually specified only as a % FS change at or near full scale at 25°C.

Conversion Rate is the speed at which an ADC or DAC can make repetitive data conversions. It is affected by propagation delay in counting circuits, ladder switches and comparators; ladder RC and amplifier settling times; amplifier and comparator slew rates; and integrating time of dual-slope converters. Conversion rate is specified as a number of conversions per second, or conversion time is specified as a number of microseconds to complete one conversion (including the effects of settling time). Sometimes, conversion rate is specified for less than full resolution, thus showing a misleading (high) rate.

Clock Rate is the minimum or maximum pulse rate at which ADC counters may be driven. There is a fixed relationship between the minimum conversion rate and the clock rate depending upon the converter accuracy and type. All factors which affect conversion rate of an ADC limit the clock rate.

Input Impedance of an ADC describes the load placed on the analog source.

Output Drive Capability describes the digital load driving capability of an ADC or the analog load driving capacity of a DAC; it is usually given as a current level or a voltage output into a given load.

CODES

Several types of DAC input or ADC output codes are in common use. Each has its advantages depending upon the system interfacing the converter. Most codes are binary in form; each is described and compared below.

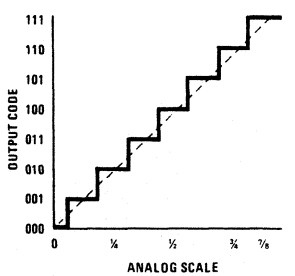
Natural Binary (or simply Binary) is the usual 2^n code with 2, 4, 8, 16, . . . , 2^n progression. An input or output high or "1" is considered a signal, whereas a "0" is considered an absence of signal. This is a positive true binary signal. Zero scale is then all "zeros" while full scale is all "ones."

Complementary Binary (or Inverted Binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all "ones" while full scale is all "zeros."

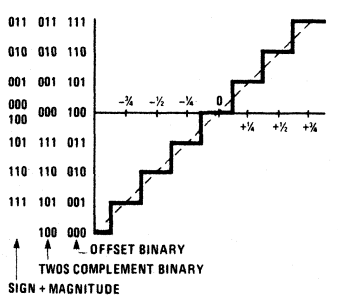
Binary Coded Decimal (BCD) is the representation of decimal numbers in binary form. It is useful in ADC systems intended to drive decimal displays. Its advantage over decimal is that only 4 lines are needed to represent 10 digits. The disadvantage of coding DACs or ADCs in BCD is that a full 4 bits could represent 16 digits while only 10 are represented in BCD. The full-scale resolution of a BCD coded system is less than that of a binary coded system. For example, a 12-bit BCD system has a resolution of only 1 part in 1000 compared to 1 part in 4096 for a binary system. This represents a loss in resolution of over 4:1.

Offset Binary is a natural binary code except that it is offset (usually ½ scale) in order to represent negative and positive values. Maximum negative scale is represented to be all "zeros" while maximum positive scale is represented as all "ones." Zero scale (actually center scale) is then represented as a leading "one" and all remaining "zeros." The comparison with binary is shown in figure 11.

Twos Complement Binary is an alternate and more widely used code to represent negative values. With this code, zero and positive values are represented as in natural binary while all negative values are represented in a twos complement form. That is, the twos complement of a number represents a negative value so that interface to a computer or microprocessor is simplified. The twos complement is formed by complementing each bit and then adding a 1; any overflow is neglected. The decimal number –8 is represented in twos complement as follows: start with binary code of decimal 8 (off scale for ± representation in 4 bits so not a valid code in the ± scale of 4 bits) which is 1000; complement it to 0111; add 0001 to get 1000. The comparison with offset binary is shown in figure 11. Note that the offset binary representation of the ± scale differs from the twos complement representation only in that the MSB is complemented. The conversion from offset binary to twos complement only requires that the MSB be inverted.



(a) Zero to + Full-Scale



(b) ± Full-Scale

FIGURE 11. ADC Codes

Sign Plus Magnitude coding contains polarity information in the MSB (MSB = 1 indicates a negative sign); all other bits represent magnitude only. This code is compared to offset binary and twos complement in figure 11. Note that one code is used up in providing a double code for zero. Sign plus magnitude code is used in certain instrument and audio systems; its advantage is that only one bit need be changed for small scale changes in the vicinity of zero, and plus and minus scales are symmetrical. A DVM might be an example of its use.

CONTROL

Each ADC must accept and/or provide digital control signals telling it and/or the external system what to do and when to do it. Control signals should be compatible with one or more types of logic in common use. Control signal timing must be such that the converter or connected system will accept the signals. Common control signals are listed below.

Start Conversion (SC) is a digital signal to an ADC which initiates a single conversion cycle. Typically, an SC signal must be present at the fall (or rise) of the clock waveform to initiate the cycle. A DAC needs no SC signal; however, such could be provided to gate digital inputs to a DAC.

End of Conversion (EOC) is a digital signal from an ADC which informs the external system that the digital output data is valid. Typically, an EOC output can be connected to an SC input to cause the ADC to operate in continuous conversion mode. In non-continuous conversion systems, the SC signal is a command from the system to the ADC. A DAC does not supply an EOC signal.

Clock signals are required or must be generated within an ADC to control counting or successive approximation registers. The clock controls the conversion speed within the limitations of the ADC. DACs do not require clock signals.

CONCLUSION

Once the user has a working knowledge of DAC or ADC characteristics and specifications, he should be able to select a converter to suit a specific system need. The likelihood of overspecification, and therefore an unnecessarily high cost, is likewise reduced. The user will also be aware that specific parameters, test conditions, test circuits, and even definitions may vary from manufacturer to manufacturer. For practical production reasons, parameters may not be tested in the same manner for all converter types, even those supplied by the same manufacturer. Using information in this note, the user should, however, be able to sort out and understand those specifications (from any manufacturer) pertinent to his needs.

IC Voltage Reference has 1 ppm per Degree Drift

National Semiconductor
Application Note 161
Robert C. Dobkin
June 1976

A new linear IC now provides the ultimate in highly stable voltage references. Now, a new monolithic IC the LM199, out-performs zeners and can provide a 6.9V reference with a temperature drift of less than 1 ppm/° and excellent long term stability. This new IC, uses a unique subsurface zener to achieve low noise and a highly stable breakdown. Included is an on-chip temperature stabilizer which holds the chip temperature at 90°C, eliminating the effects of ambient temperature changes on reference voltage.

The planar monolithic IC offers superior performance compared to conventional reference diodes. For example, active circuitry buffers the reverse current to the zener giving a dynamic impedance of 0.5Ω and allows the LM199 to operate over a 0.5 mA to 10 mA current range with no change in performance. The low dynamic impedance, coupled with low operating current significantly simplifies the current drive circuitry needed for operation. Since the temperature coefficient is independent of operating current, usually a resistor is all that is needed.

Previously, the task of providing a stable, low temperature coefficient reference voltage was left to a discrete zener diode. However, these diodes often presented significant problems. For example, ordinary zeners can show many millivolts change if there is a temperature gradient across the package due to the zener and temperature compensation diode not being at the same temperature. A 1°C difference may cause a 2 mV shift in reference voltage. Because the on-chip temperature stabilizer maintains constant die temperature, the IC reference is free of voltage shifts due to temperature gradients. Further, the temperature stabilizer, as well as eliminating drift, allows exceptionally fast warm-up over conventional diodes. Also, the LM199 is insensitive to stress on the leads—another source of error with ordinary glass diodes. Finally, the LM199 shows virtually no hysteresis in reference voltage when subject to temperature cycling over a wide temperature range. Temperature cycling the LM199 between 25°C, 150°C and back to 25°C causes less than 50μV change in reference voltage. Standard reference diodes exhibit shifts of 1 mV to 5 mV under the same conditions.

SUB SURFACE ZENER IMPROVES STABILITY

Previously, breakdown references made in monolithic IC's usually used the emitter-base junction of an NPN transistor as a zener diode. Unfortunately, this junction breaks down at the surface of the silicon and is therefore susceptible to surface effects. The breakdown is noisy, and cannot give long-term stabilities much better than about 0.3%. Further, a surface zener is especially sensitive to contamination in the oxide or charge on the surface of the oxide which can cause short-term instability or turn-on drift.

The new zener moves the breakdown below the surface of the silicon into the bulk yielding a zener that is stable with time and exhibits very low noise. Because the new zener is made with well-controlled diffusions in a planar structure, it is extremely reproducible with an initial 2% tolerance on breakdown voltage.

A cut-away view of the new zener is shown in *Figure 1.* First a small deep P+ diffusion is made into the surface of the silicon. This is then covered by the standard base diffusion. The N+ emitter diffusion is then made completely covering the P+ diffusion. The diode then breaks down where the dopant concentration is greatest, that is, between the P+ and N+. Since the P+ is completely covered by N+ the breakdown is below the surface and at about 6.3V. One connection to the diode is to the N+ and the other is to the P base diffusion. The current flows laterally through the base to the P+ or cathode of the zener. Surface breakdown does not occur since the base P to N+ breakdown voltage is greater than the breakdown of the buried device. The buried zener has been in volume production since 1973 as the reference in the LX5600 temperature transducer.

CIRCUIT DESCRIPTION

The block diagram of the LM199 is shown in *Figure 2.* Two electrically independent circuits are included on the same chip—a temperature stabilizer and a floating active zener. The only electrical connection between the two

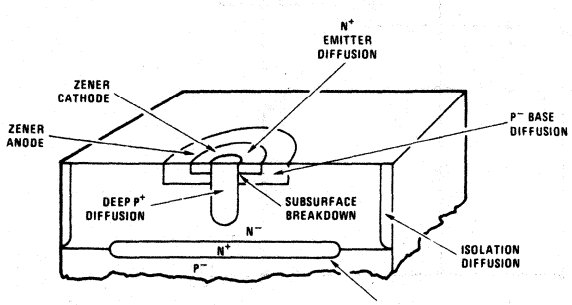


FIGURE 1. Subsurface Zener Construction

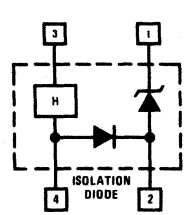


FIGURE 2. Functional Block Diagram

circuits is the isolation diode inherent in any junction-isolated integrated circuit. The zener may be used with or without the temperature stabilizer powered. The only operating restriction is that the isolation diode must never become forward biased and the zener must not be biased above the 40V breakdown of the isolation diode.

The actual circuit is shown in *Figure 3*. The temperature stabilizer is composed of Q1 through Q9. FET Q9 provides current to zener D2 and Q8. Current through Q8 turns a loop consisting of D1, Q5, Q6, Q7, R1 and R2. About 5V is applied to the top of R1 from the base of Q7. This causes 400μA to flow through the divider R1, R2. Transistor Q7 has a controlled gain of 0.3 giving Q7 a total emitter current of about 500μA. This flows through the emitter of Q6 and drives another controlled gain PNP transistor Q5. The gain of Q5 is about 0.4 so D1 is driven with about 200μA. Once current flows through Q5, Q8 is reverse biased and the loop is self-sustaining. This circuitry ensures start-up.

The resistor divider applies 400 mV to the base of Q4 while Q7 supplies 120μA to its collector. At temperatures below the stabilization point, 400 mV is insufficient to cause Q4 to conduct. Thus, all the collector current from Q7 is provided as base drive to a Darlington composed of Q1 and Q2. The Darlington is connected across the supply and initially draws 140 mA (set by current limit transistor Q3). As the chip heats, the turn on voltage for Q4 decreases and Q4 starts to conduct. At about 90°C the current through Q4 appreciably increases and less drive is applied to Q1 and Q2. Power dissipation decreases to whatever is necessary to hold the chip at the stabilization temperature. In this manner, the chip temperature is regulated to better than 2°C for a 100°C temperature range.

The zener section is relatively straight-forward. A buried zener D3 breaks down biasing the base of transistor Q13. Transistor Q13 drives two buffers Q12 and Q11. External current changes through the circuit are fully absorbed by the buffer transistors rather than D3. Current through D3 is held constant at 250μA by a 2k resistor across the emitter base of Q13 while the emitter-base voltage of Q13 nominally temperature compensates the reference voltage.

The other components, Q14, Q15 and Q16 set the operating current of Q13. Frequency compensation is accomplished with two junction capacitors.

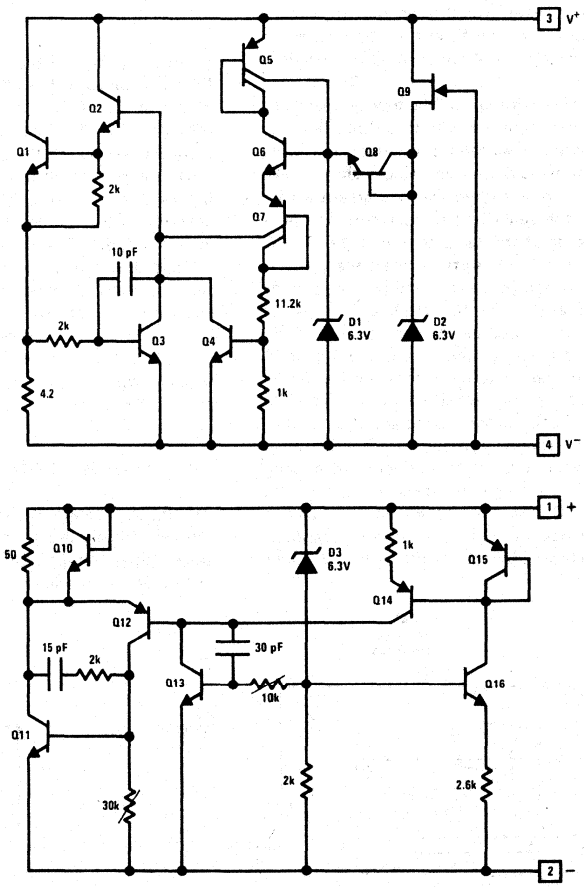


FIGURE 3. Schematic Diagram of LM199 Precision Reference

PERFORMANCE

A polysulfone thermal shield, shown in *Figure 4,* is supplied with the LM199 to minimize power dissipation and improve temperature regulation. Using a thermal shield as well as the small, high thermal resistance TO-46 package allows operation at low power levels without the problems of special IC packages with built-in thermal isolation. Since the LM199 is made on a standard IC assembly line with standard assembly techniques, cost is significantly lower than if special techniques were used. For temperature stabilization only 300 mW are required at 25°C and 660 mW at −55°C.

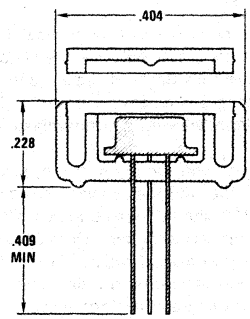


FIGURE 4. Polysulfone Thermal Shield

Temperature stabilizing the device at 90°C virtually eliminates temperature drift at ambient temperatures less than 90°C. The reference is nominally temperature compensated and the thermal regulator further decreases the temperature drift. Drift is typically only 0.3 ppm/°C. Stabilizing the temperature at 90°C rather than 125°C significantly reduces power dissipation but still provides very low drift over a major portion of the operating temperature range. Above 90°C ambient, the temperature coefficient is only 15 ppm/°C.

A low drift reference would be virtually useless without equivalent performance in long term stability and low noise. The subsurface breakdown technology yields both of these. Wideband and low frequency noise are both exceptionally low. Wideband noise is shown in *Figure 5* and low frequency noise is shown over a 10 minute period in the photograph of *Figure 6.* Peak to peak noise over a 0.01 Hz to 1 Hz bandwidth is only about 0.7μV.

Long term stability is perhaps one of the most difficult measurements to make. However, conditions for long-term stability measurements on the LM199 are considerably more realistic than for commercially available certified zeners. Standard zeners are measured in ±0.05°C temperature controlled both at an operating current of 7.5 mA ±0.05μA. Further, the standard devices must have stress-free contacts on the leads and the test must not be interrupted during the measurement interval. In contrast, the LM199 is measured in still air of 25°C to 28°C at a reverse current of 1 mA ±0.5%. This is more typical of actual operating conditions in instruments.

When a group of 10 devices were monitored for long-term stability, the variations all correlated, which indicates changes in the measurement system (limitation of 20 ppm) rather than the LM199.

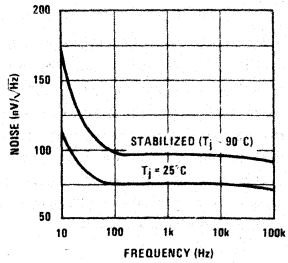


FIGURE 5. Wideband Noise of the LM199 Reference

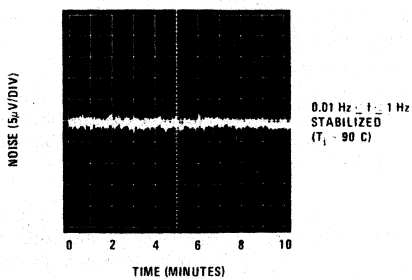


FIGURE 6. Low Frequency Noise Voltage

Because the planar structure does not exhibit hysteresis with temperature cycling, long-term stability is not impaired if the device is switched on and off.

The temperature stabilizer heats the small thermal mass of the LM199 to 90°C very quickly. Warm-up time at 25°C and −55°C is shown in *Figure 7.* This fast warm-up is significantly less than the several minutes needed by ordinary diodes to reach equilibrium. Typical specifications are shown in Table I.

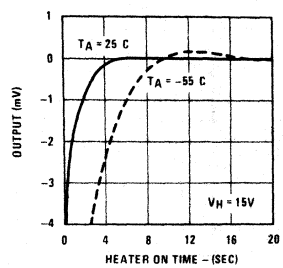


FIGURE 7. Fast Warmup Time of the LM199

Table I. Typical Specifications for the LM199

Reverse Breakdown Voltage	6.95V
Operating Current	0.5 mA to 10 mA
Temperature Coefficient	0.3 ppm/°C
Dynamic Impedance	0.5Ω
RMS Noise (10 Hz to 10 kHz)	7μV
Long-Term Stability	≤ 20 ppm
Temperature Stabilizer Operating Voltage	9V to 40V
Temperature Stabilizer Power Dissipation (25°C)	300 mW
Warm-up Time	3 Seconds

APPLICATIONS

The LM199 is easier to use than standard zeners, but the temperature stability is so good—even better than precision resistors—that care must be taken to prevent external circuitry from limiting performance. Basic operation only requires energizing the temperature stabilizer from a 9V to 40V power source and biasing the reference with between 0.5 mA to 10 mA of current. The low dynamic impedance minimizes the current regulation required compared to ordinary zeners.

The only restriction on biasing the zener is the bias applied to the isolation diode. Firstly, the isolation diode must not be forward biased. This restricts the voltage at either terminal of the zener to a voltage equal to or greater than the V^-.

A dc return is needed between the zener and heater to insure the voltage limitation on the isolation diodes are not exceeded. *Figure 8* shows the basic biasing of the LM199.

The active circuitry in the reference section of the LM199 reduces the dynamic impedance of the zener to about 0.5Ω. This is especially useful in biasing the reference. For example, a standard reference diode such as a 1N829 operates at 7.5 mA and has a dynamic impedance of 15Ω. A 1% change in current (75μA) changes the reference voltage by 1.1 mV. Operating the LM199 at 1 mA with the same 1% change in operating current (10μA) results in a reference change of only 5μV. *Figure 9* shows reverse voltage change with current.

Biasing current for the reference can be anywhere from 0.5 mA to 10 mA with little change in performance. This wide current range allows direct replacement of most zener types with no other circuit changes besides the temperature stabilizer connection. Since the dynamic impedance is constant with current changes regulation

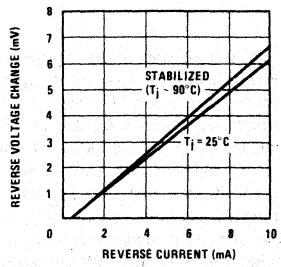


FIGURE 9. The LM199 Shows Excellent Regulation Against Current Changes

is better than discrete zeners. For optimum regulation, lower operating currents are preferred since the ratio of source resistance to zener impedance is higher, and the attenuation of input changes is greater. Further, at low currents, the voltage drop in the wiring is minimized.

Mounting is an important consideration for optimum performance. Although the thermal shield minimizes the heat low, the LM199 should not be exposed to a direct air flow such as from a cooling fan. This can cause as much as a 100% increase in power dissipation degrading the thermal regulation and increasing the drift. Normal conviction currents do not degrade performance.

Printed circuit board layout is also important. Firstly, four wire sensing should be used to eliminate ohmic drops in pc traces. Although the voltage drops are small the temperature coefficient of the voltage developed along a copper trace can add significantly to the drift. For example, a trace with 1Ω resistance and 2 mA current flow will develop 2 mV drop. The TC of copper is 0.004%/°C so the 2 mV drop will change at 8μV/°C, this is an additional 1 ppm drift error. Of course, the effects of voltage drops in the printed circuit traces are eliminated with 4-wire operation. The heater current also should not be allowed to flow through the voltage reference traces. Over a −55°C to +125°C temperature

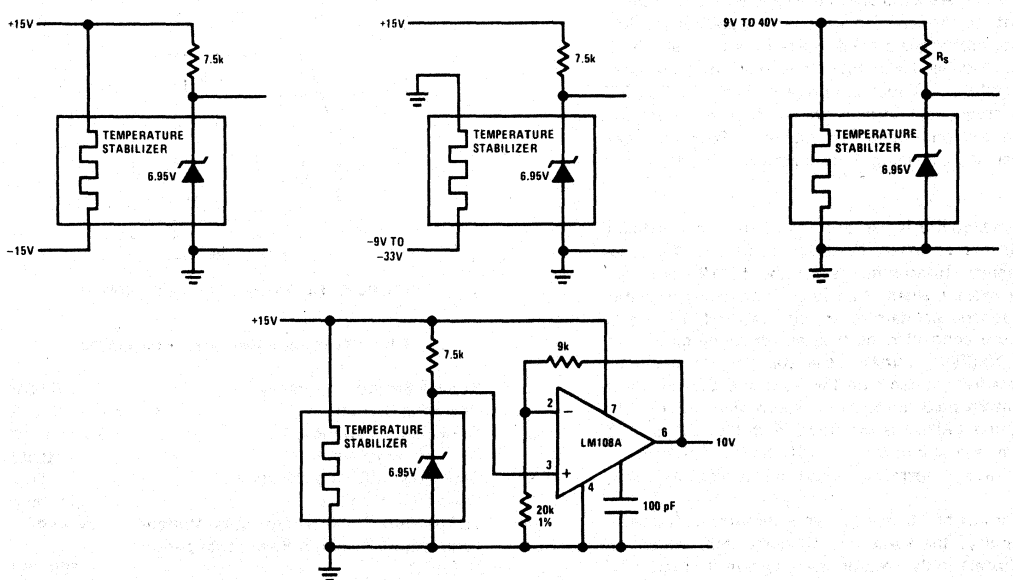


FIGURE 8. Basic Biasing of the LM199

range the heater current will change from about 1 mA to over 40 mA. These magnitudes of current flowing reference leads or reference ground can cause huge errors compared to the drift of the LM199.

Thermocouple effects can also cause errors. The kovar leads from the LM199 package form a thermocouple with copper printed circuit board traces. Since the package of the 199 is heated, there is a heat flow along the leads of the LM199 package. If the leads terminate into unequal sizes of copper on the p.c. board greater heat will be absorbed by the larger copper trace and a temperature difference will develop. A temperature *difference* of 1°C between the two leads of the reference will generate about 30μV. Therefore, the copper traces to the zener should be equal in size. This will generally keep the errors due to thermocouple effects under about 15μV.

The LM199 should be mounted flush on the p.c. board with a minimum of space between the thermal shield and the boards. This minimizes air flow across the kovar leads on the board surface which also can cause thermocouple voltages. Air currents across the leads usually appear as ultra-low frequency noise of about 10μV to 20μV amplitude.

It is usually necessary to scale and buffer the output of any reference to some calibrated voltage. *Figure 10* shows a simple buffered reference with a 10V output. The reference is applied to the non-inverting input of the LM108A. An RC rolloff can be inserted in series with the input to the LM108A to roll-off the high frequency noise. The zener heater and op amp are all powered from a single 15V supply. About 1% regulation on the input supply is adequate contributing less than 10μV of error to the output. Feedback resistors around the LM308 scale the output to 10V.

Although the absolute values of the resistors are not extremely important, tracking of temperature coefficients is vital. The 1 ppm/°C drift of the LM199 is easily exceeded by the temperature coefficient of most resistors. Tracking to better than 1 ppm is also not easy to obtain. Wirewound types made of Evenohm or Mangamin are good and also have low thermoelectric effects. Film types such as Vishay resistors are also good. Most potentiometers do not track fixed resistors so it is a good idea to minimize the adjustment range and therefore minimize their effects on the output TC. Overall temperature coefficient of the circuit shown in *Figure 10* is worst case 3 ppm/°C. About 1 ppm is due to the reference, 1 ppm due to the resistors and 1 ppm due to the op amp.

Figure 11 shows a standard cell replacement with a 1.01V output. A LM321 and LM308 are used to minimize op amp drift to less than 1μV/°C. Note the adjustment connection which minimizes the TC effects of the pot. Set-up for this circuit requires nulling the offset of the op amp first and then adjusting for proper output voltage.

The drift of the LM321 is very predictable and can be used to eliminate overall drift of the system. The drift changes at 3.6μV/°C per millivolt of offset so 1 mV to 2 mV of offset can be introduced to minimize the overall TC.

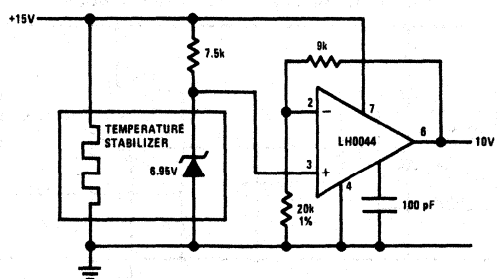


FIGURE 10. Buffered 10V Reference

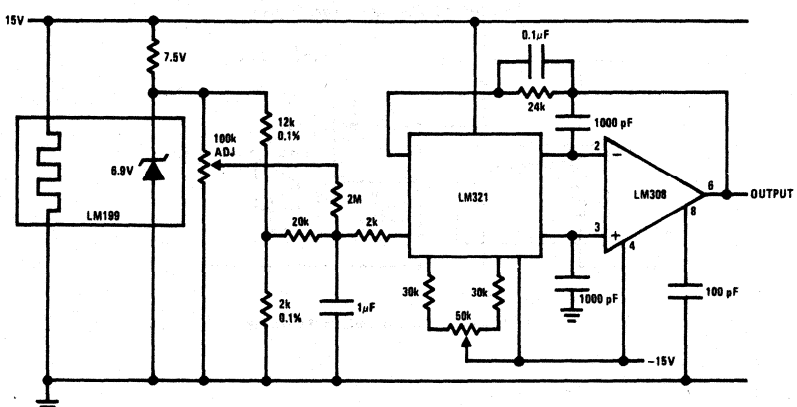


FIGURE 11. Standard Cell Replacement

For circuits with a wide input voltage range, the reference can be powered from the output of the buffer as is shown in *Figure 12.* The op amp supplies regulated voltage to the resistor biasing the reference minimizing changes due to input variation. There is some change due to variation of the temperature stabilizer voltage so extremely wide range operation is not recommended for highest precision. An additional resistor (shown 80 kΩ) is added to the unregulated input to insure the circuit starts up properly at the application of power.

A precision power supply is shown in *Figure 13.* The output of the op amp is buffered by an IC power transistor the LM395. The LM395 operates as an NPN power device but requires only 5μA base current. Full overload protection inherent in the LM395 includes current limit, safe-area protection, and thermal limit.

A reference which can supply either a positive or a negative continuously variable output is shown in *Figure 14.* The reference is biased from the ±15V input supplies as was shown earlier. A ten-turn pot will adjust the output from $+V_Z$ to $-V_Z$ continuously. For negative output the op amp operates as an inverter while for positive outputs it operates as a non-inverting connection.

Op amp choice is important for this circuit. A low drift device such as the LM108A or a LM108-LM121 combination will provide excellent performance. The pot should be a precision wire wound 10 turn type. It should be noted that the output of this circuit is not linear.

CONCLUSIONS

A new monolithic reference which exceeds the performance of conventional zeners has been developed. In fact, the LM199 performance is limited more by external components than by reference drift itself. Further, many of the problems associated with conventional zeners such as hysteresis, stress sensitivity and temperature gradient sensitivity have also been eliminated. Finally, long-term stability and noise are equal of the drift performance of the new device.

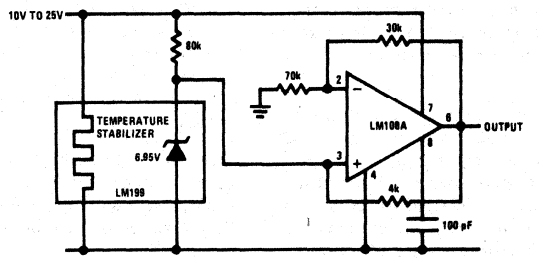


FIGURE 12. Wide Range Input Voltage Reference

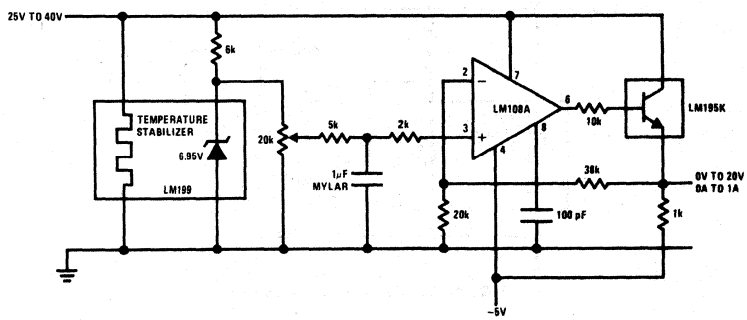


FIGURE 13. Precision Power Supply

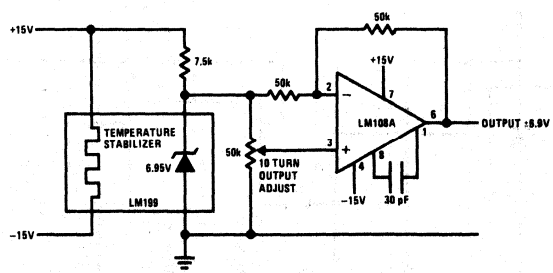


FIGURE 14. Bipolar Output Reference

IC Zener Eases Reference Design

National Semiconductor
Application Note 173
Robert C. Dobkin
November 1976

DESCRIPTION

A new IC Zener with low dynamic impedance and wide operating current range significantly simplifies reference or regulator circuit design. The low dynamic impedance provides better regulation against operating current changes, easing the requirements on the biasing supply. Further, the temperature coefficient is independent of operating current, so that the LM129 can be used at any convenient current level. Other characteristics such as temperature coefficient, noise and long term stability are equal to or better than good quality discrete Zeners.

The LM129 uses a new subsurface breakdown IC Zener combined with a buffer circuit to lower dynamic impedance. The new subsurface Zener has low noise and excellent long term stability since the breakdown is in the bulk of the silicon. Circuitry around the Zener supplies internal biasing currents and buffers external current changes from the Zener. The overall breakdown is about 6.9 V with devices selected for temperature coefficients.

The Zener is relatively straightforward. A buried Zener D1 breaks down biasing the base of transistor Q1. Transistor Q1 drives two buffers Q2 and Q3. External current changes through the circuit are fully absorbed by the buffer transistors rather than by D1. Current through D1 is held constant at 250 μA by a 2k resistor across the emitter base of Q1 while the emitter-base voltage of Q1 nominally temperature compensates the reference voltage.

The other components, Q4, Q5 and Q6, set the operating current of Q1. Frequency compensation is accomplished with two junction capacitors.

All that is needed for biasing in most applications is a resistor as shown in figure 2. Biasing current can be anywhere from 0.6 mA to 15 mA with little change in performance. Optimally, however, the biasing current should be as low as possible for the best regulation. The dynamic impedance of the LM129 is about 1 Ω and is independent of current. Therefore, the regulation of the LM129 against voltage changes is 1/Rs.

Lower currents or higher Rs give better regulation. For example, with a 15 V supply and 1 mA operating current, the reference change for a 10% change in the 15 V supply is 180 μV. If the LM129 is run at 5 mA, the change is 900 μV or 5 times worse. By comparison, a standard IN821 Zener will change about 17 mV. All discrete Zeners have about the same regulation since their dynamic impedance is inversely proportional to operating current.

If the Zener does not have to be grounded, a bridge compensating circuit can be used to get virtually perfect regulation, as shown in figure 3. A small compensating voltage is generated across R1, which matches the dynamic impedance of the LM129. Since the dynamic impedance of the LM129 is linear with current, this circuit will work even with large changes in the unregulated input voltage.

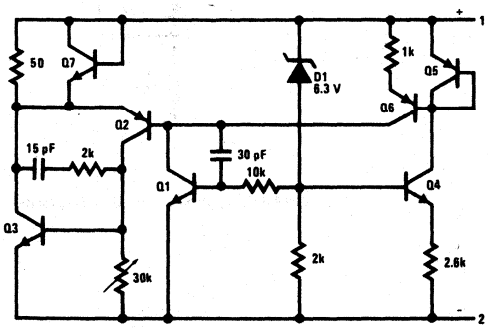


FIGURE 1. IC Reference Zener

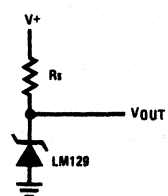


FIGURE 2. Basic Biasing

Other output voltages are easily obtained with the simple op-amp circuit shown in figure 4. A simple non-inverting amplifier is used to boost and buffer the Zener to 10 V. The reference is run directly from the input power rather than the output of the op-amp. When the Zener is powered from the op-amp, special starting circuitry is sometimes necessary to insure the output comes up in the right polarity. For outputs lower than the breakdown of the LM129 a divider can be connected across the Zener to drive the op-amp.

An AC square wave or bipolarity output reference can easily be made with an op-amp and FET switch as shown in figure 5. When Q1 is "ON," the LM108 functions as a normal inverting op-amp with a gain of −1 and an output of −6.9 V. With Q1 "OFF" the op-amp acts as a giving 6.9 V at the output. Some non-symmetry will occur from loading change on the LM129 in the different states and mismatch of R1 and R2. Trimming either R1 or R2 can make the output exactly symmetrical around ground.

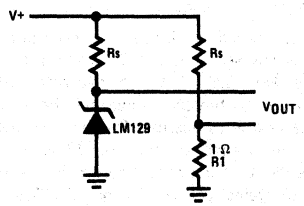


FIGURE 3. Bridge Compensation for Line Changes

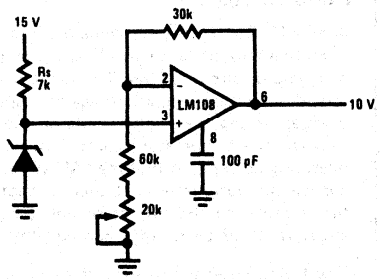


FIGURE 4. 10 Volt Buffered Output Reference

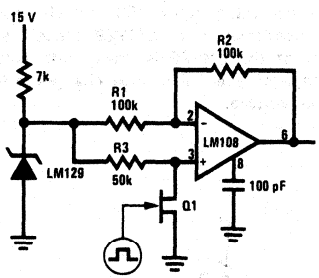


FIGURE 5. Bipolar Output Reference

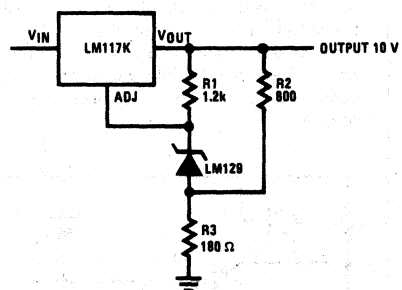


FIGURE 6. High Stability 10 V Regulator

By combining the LM129 with an LM117 three-terminal regulator a high stability power regulator can be made. This is shown in figure 6. Resistor R1 biases the LM129 at about 1 mA from the 1.25 V reference in the LM117. The voltage of the LM129 is added to the 1.25 V of the LM117 to make a total reference voltage of 8.1 V. The output voltage is then set at 10 V by R2 and R3. Since the internal reference of the LM117 contributes only about 20% of the total reference voltage, regulation and drift are essentially those of the external Zener. The regulator has 0.2% load and line regulation and if a low drift Zener such as the LM129A is used overall temperature coefficient is less than 0.002%/°C.

The new Zener can be used as the reference for conventional IC voltage regulators for enhanced performance. Noise is lower, time stability is better, and temperature coefficient can be better depending on the device selected. Further, the output voltage is independent of power changes in the regulator.

Figure 7 shows an LM723 using an external LM129 reference. The internal 7 V reference is not used and a single resistor biases the LM129 as the reference. The 5k resistor chosen provides sufficient operating current for the Zener over the 10 V to 40 V input voltage range of the LM723. Since the dynamic impedance of the LM129 is so low, the reference regulation against line changes is only 0.02%/V. This is small compared to the regulation of 0.1%/V for the LM723; however, the resistor can be replaced by a 1 mA to 5 mA FET used as a constant current source for improved regulation. When the FET is used reference regulation is easily 0.001%/V. Output voltage is set in the standard manner except that for low output voltages sufficient current must be run through the Zener to power the voltage divider supplying the reference to the LM723.

An overload protected power shunt regulator is shown in figure 8. The output voltage is about 7.8 V – the 7 V breakdown of the LM129 plus the 0.8 V emitter-base voltage of the LM395. The LM395 is an IC, 1.5 A power transistor with complete overload protection on the chip. Included on the chip are current limiting and thermal limiting, making the device virtually blowout-proof. Further, the base current is only 5 μA, making it easy to drive as a shunt regulator. As the input voltage rises, more drive is applied to the base of the LM395, turning it on harder and dropping more voltage across the series resistance. Should the input voltage rise too high, the LM395 will current limit or thermal limit, protecting itself.

The new IC Zener can replace existing Zeners in just about any application with improved performance and simpler external circuitry. As with any Zener reference, devices are selected for temperature coefficient and operating temperature range. Since the devices are made by a standard integrated circuit process, cost is low and good reproducibility is obtained in volume production.

Finally, since the device is actually an IC, it is packaged in a rugged TO-46 metal can package or a 3-lead plastic transistor package.

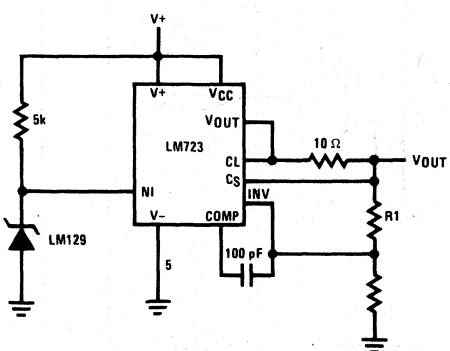


FIGURE 7. External Reference For IC

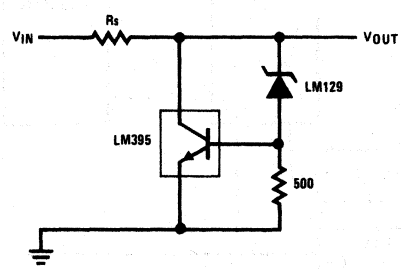


FIGURE 8. Power Shunt Regulator

A/D Converter Testing

National Semiconductor
Application Note 179
Dennis Dauenhauer
Doug Falco
April 1977

Attempting to test an analog-to-digital converter can be a challenging and rewarding experience. The recent increased interest in converter products has spawned renewed interest in test equipment dedicated to testing converters. Unfortunately, the broad range of converter products available makes testing by a single piece of equipment difficult at best.

A crude method of testing would be to monitor an analog signal at the converter input using a precision DVM and compare that with the converter output. This is simple enough to do, but in most cases this would prove impractical. For a 10-bit converter, this would require plotting 1,024 such readings. Automatic equipment can be used, but in all cases will require some sophisticated interface hardware and software routines. A person favoring auto test equipment can expect to pay around $10,000 for the hardware and at least that much for the software. What will be described is a method which costs a couple hundred dollars in components and which gives a device characteristic in a relatively short time period.

Because very little standardization has occurred for converter products, the user must adhere to the old adage "caveat emptor" or "buyer beware". The only universal statement that can be made for definitions of terms characterizing converter products is that they are universally inconsistent. For this reason, this application note will provide a simple method of providing a very graphic means of testing several of National's A/D converter products. It is also recommended that the reader refer to Application Note AN-156 for additional information concerning converter products definitions. Specific parameters which will be focused on in this paper are zero error, scale error, non-linearity error, differential non-linearity, monotonicity, total unadjusted error and quantizing error.

The block diagram of *Figure 1* shows the basic blocks of the complete test circuit of *Figure 2*. A storage scope is required to provide a continuous display. A Tektronix 7633 or equivalent is recommended. A typical characteristic for the ADC0800 shown in *Figure 3*.

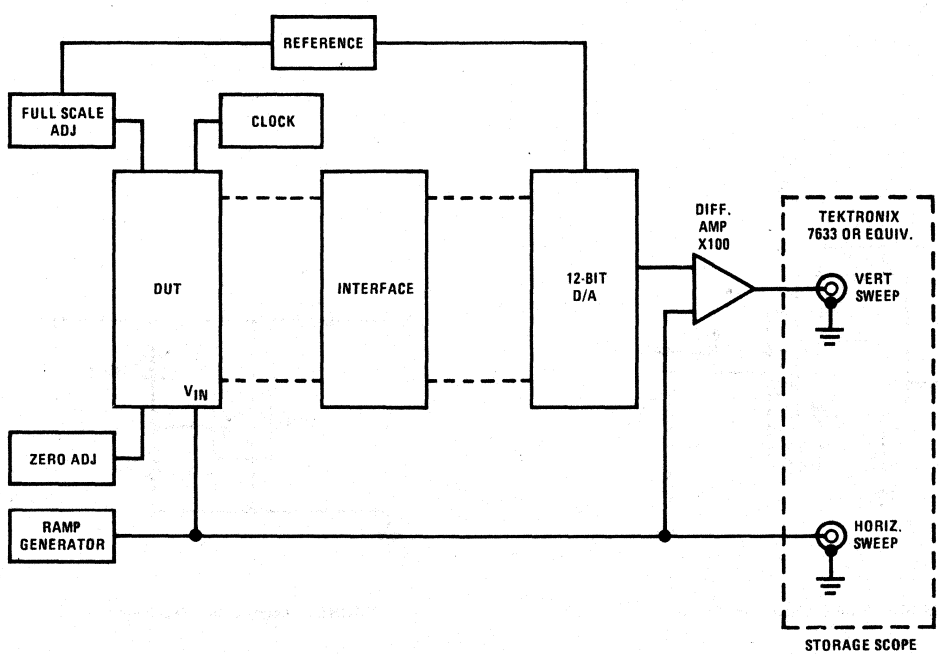


FIGURE 1. Block Diagram for A/D Tester

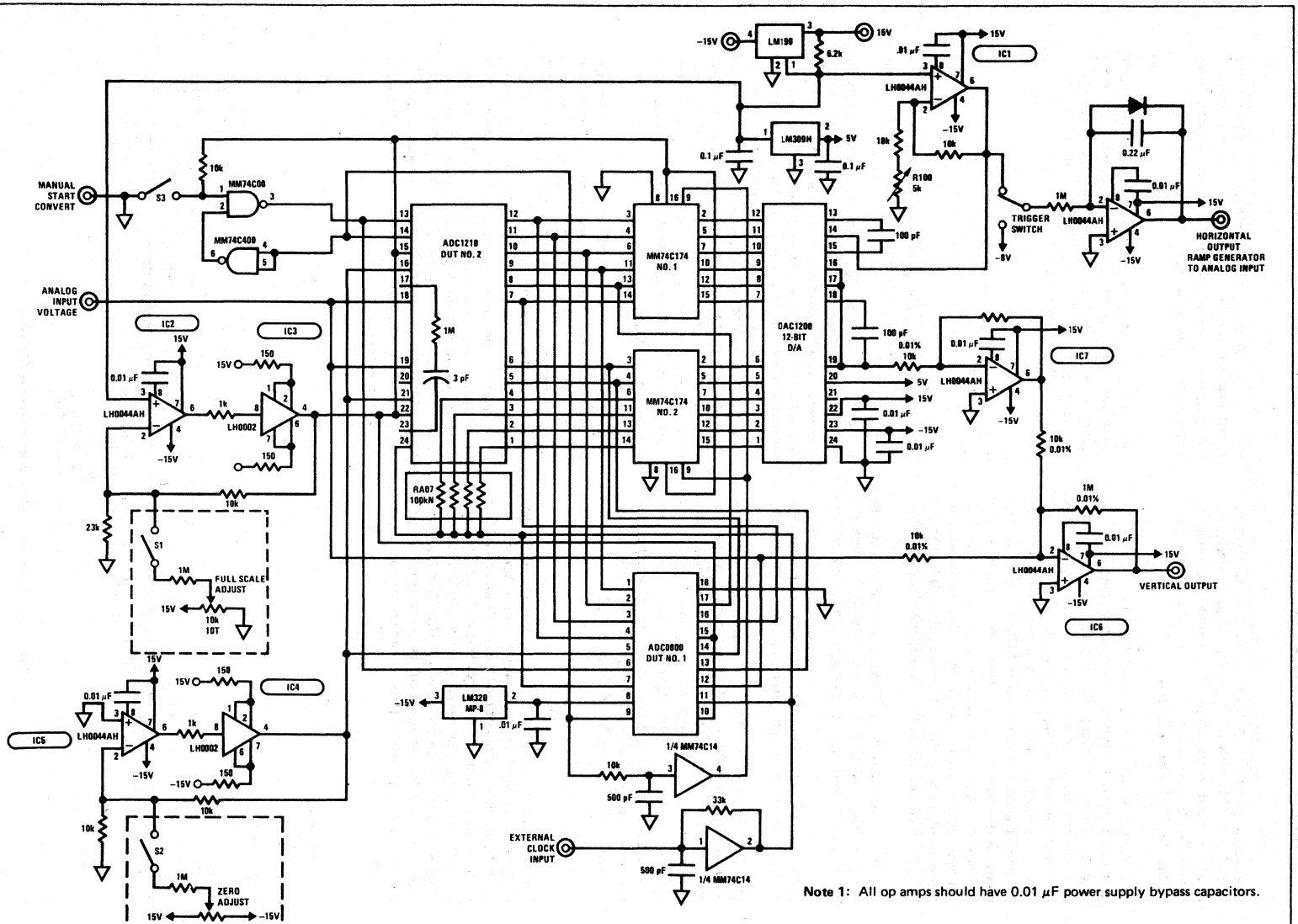

MANUAL START CONVERT
ANALOG INPUT VOLTAGE
S3
MM74C08
MM74C408
ADC1210 DUT NO. 2
MM74C174 NO. 1
MM74C174 NO. 2
DAC1208 12-BIT D/A
RA07 10pkN
ADC0808 DUT NO. 1
LM199
LM309H
LM320 MP-8
LH0044AH
LH0002
IC1
IC2
IC3
IC4
IC5
IC6
IC7
R100 5k
TRIGGER SWITCH
HORIZONTAL OUTPUT RAMP GENERATOR TO ANALOG INPUT
VERTICAL OUTPUT
S1
FULL SCALE ADJUST
S2
ZERO ADJUST
1/4 MM74C14
EXTERNAL CLOCK INPUT
Note 1: All op amps should have 0.01 μF power supply bypass capacitors.

FIGURE 2

The ramp generator provides a linear output voltage from 0V to 10V. This voltage is used as a) the horizontal amplifier input to the scope b) as a reference voltage to the difference amplifier and c) as the analog input voltage to the device under test.

The storage scope is used as an X-Y display with the horizontal input functioning as an input amplifier. The vertical input (Y-direction) displays the difference between the converter's analog input voltage and the equivalent output voltage of the same converter. The equivalent output voltage is generated by the 12-bit digital-to-analog converter (DAC1200). The horizontal input (X-direction) displays the difference voltage over the entire analog input voltage range. For a reference voltage set to 10.24V, the range is 0V to 10.24V. In the case of an 8-bit A/D, there would be 256 different voltages displayed across the entire range of the reference.

The test circuit shown in *Figure 2* can be used to test the ADC0800, ADC1211 or the ADC1210. These are 8-bit, 10-bit and 12-bit analog-to-digital converters.

Zero and full scale adjustment circuits are provided to allow a more accurate computation of non-linearity error.

The DAC1200D is a 12-bit D/A converter. It is quite adequate for the 8-bit and 10-bit parts but may be replaced by a higher resolution part if testing 12-bit A/D converters. The LH0044AH is a precision low noise amplifier and the LH0002CH is a buffer amplifier. The output of the reference must be adjusted to the full scale input voltage to assure proper output from the DAC1200. This is done by adjusting R-100.

TESTING

Figure 3 shows a typical output characteristic for the ADC0800, an 8-bit A/D converter. The reference line is set by switching the vertical channel (Y-axis amplifier) to dc and triggering the ramp generator. The adjustment is made using the horizontal positioning. The vertical range should be set to 5V/division. The 50 mV/division shown is the effective range of the channel taking into the account that the difference amplifier has a gain of 100.

When the initial set-up is completed, it is relatively easy to get readings for zero error, scale error, non-linearity error, differential non-linearity error, quantizing error, and to detect missing codes.

Zero error is simply the deviation from the reference line to the middle of the quantizing error when the input voltage is zero. All errors can be expressed as percent of full scale of in LSB's (least significant bits). For a 0V to 10.24V analog input 8-bit converter;

$$1\ \text{LSB} = \frac{10\text{V}}{2^8} = 40\ \text{mV} = 0.40\%\ \text{FS}$$

Scale error is the same as the zero error except that it occurs when the analog input voltage is at full scale.

In most applications, it is not the non-linearity in itself which is important, but rather the slope of the non-linearity. For instance, in an application using an A/D to sense gas in a tank and then to compute the remaining miles or time based on the current rate of usage, you do not want a large non-linearity slope. This gives the typical analog gas gauge effect of getting what appears to be good mileage over a certain range and poorer mileage over another range. Specifying non-linearity error and differential non-linearity error provides an error band around which to limit this change in slope or rate of change.

Non-linearity error can be defined in either of 2 ways. Shown in *Figure 3* is the "best straight line" definition for non-linearity. This is the more traditional definition for non-linearity and is the one use for the ADC0800 because of the inherent unidirectional nature of the error. A more conservative definition of "ideal straight line linearity" or more appropriately "total error" is twice that of the best straight line error. This linearity error is the maximum deviation from a straight line drawn between zero and full scale. The ADC1210 and ADC1211, 12-bit and 10-bit A/D converters, use this definition of non-linearity because the deviation can be in either direction.

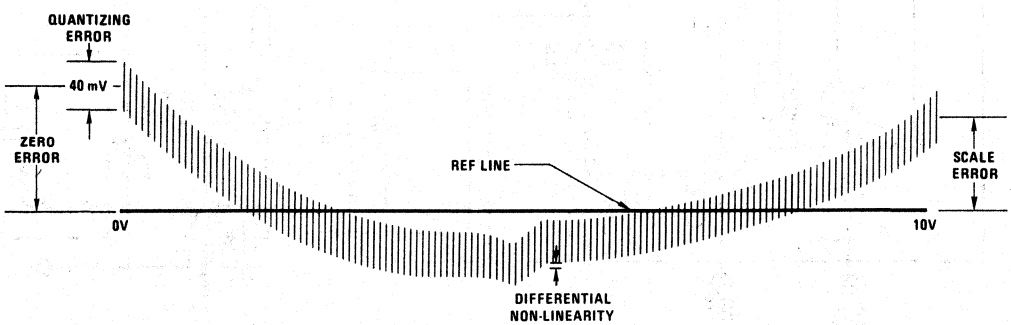


FIGURE 3. Typical Output Characteristic for the ADC0800

Differential non-linearity is most noticeable in converters using the successive approximation technique for conversion. It occurs when switching in a new resistance value for approximating the analog input voltage. It is the amount of change in the input voltage required to get a change in the digital output. On the scope it shows up as a change in non-linearity at one point. Differential non-linearity with this test method can be used to check for "no missing codes". "No missing codes" means that over the reference range, the converter will provide 2^n digital output codes, where N is the resolution of the converter.

Total unadjusted error is the maximum deviation from an ideal transfer function for an A/D converter. This error does not include quantizing error. The non-linearity error of an unadjusted ADC0800 is in a direction so as to decrease the total error. Therefore, the total unadjusted error for the ADC0800 will be either the zero error or the scale error, whichever is greater. This characteristic is only peculiar to this form of successive approximation type of converter.

Quantizing is inherent in the nature of the device. An 8-bit converter can make only 256 changes in the output regardless of the input voltage range. Therefore, for any converter there is always 1 LSB of quantizing error. This would appear as ±1/2 LSB of error around a straight line approximation of the output characteristic.

Monotonicity is the ability of the converter to give a digital output which is always in the same direction as the analog input voltage. The ADC0800 is inherently monotonic.

This paper has focused on the parameters peculiar to A/D converter products. It should give the user of any manufacturer's A/D converter a method for easily testing and comparing the characteristics of a particular A/D converter. It provides a low cost means of testing parameters which have historically been difficult to test.

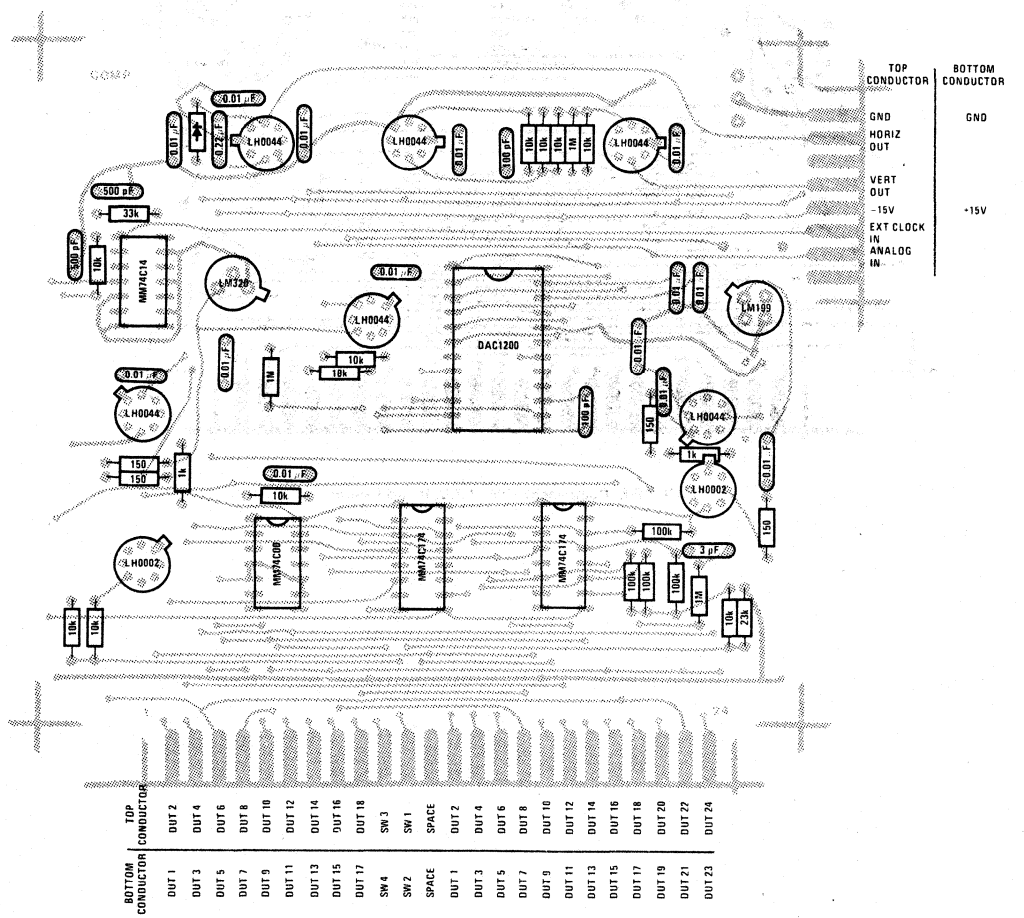


FIGURE 4. "Component Placement" on Component Side of P.C. Board

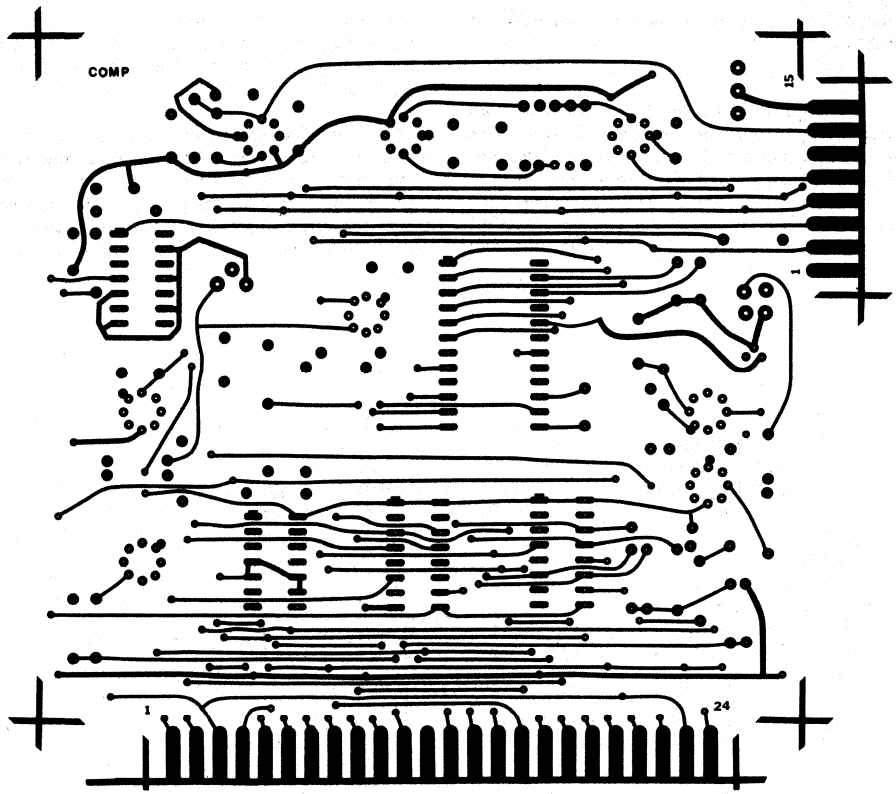


FIGURE 5. Component Side of P.C. Board Layout

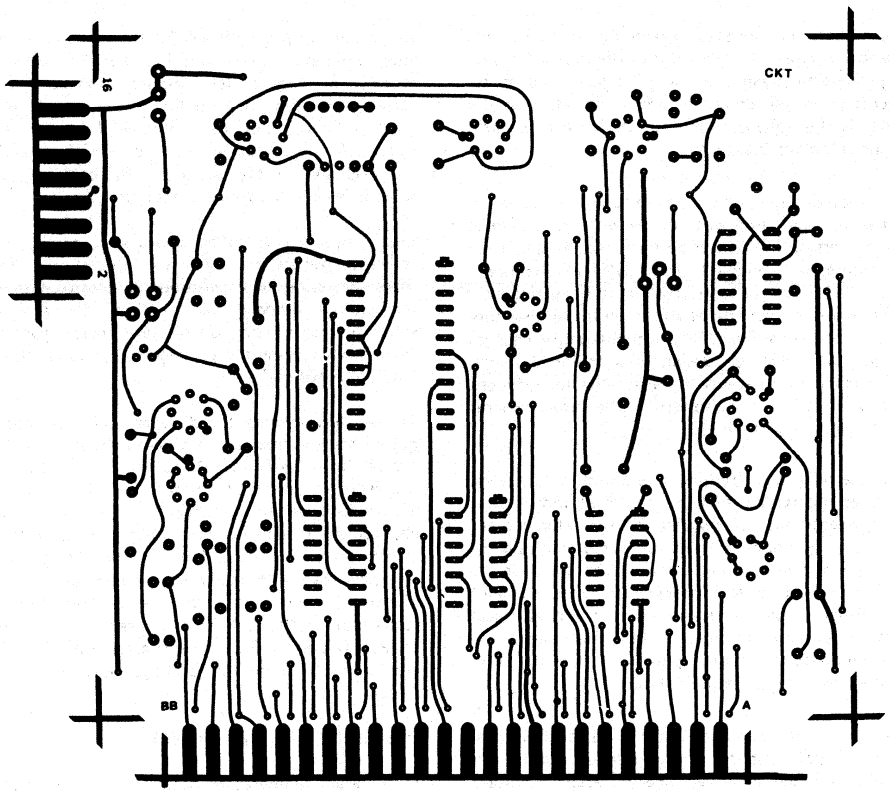


FIGURE 6. Backside of P.C. Board Layout

References for A/D Converters

National Semiconductor
Application Note 184
Robert C. Dobkin
July 1977

Interfacing between digital and analog signals is becoming increasingly important with the proliferation of digital signal processing. System accuracy is often limited by the accuracy of the converter and a limitation of the converter is the voltage reference. Design can be difficult if the reference is external.

The accuracy of any converter is limited by the temperature dirft or long term drift of the voltage reference, even if conversion linearity is perfect. Assuming that the voltage reference is allowed to add 1/2 least significant bit error (LSB) to the converter, it is surprising how good the reference must be when even small temperature excursions are considered. When temperature changes are large, the reference design is a major problem. Table I shows the reference requirements for different converters while Table II shows how the same problems exist with digital panel meters.

The voltage reference circuitry is required to do several functions to maintain a stable output. First, input power supply changes must be rejected by the reference circuitry. Secondly, the zener used in the reference must be biased properly, while other parts of circuitry scale the typical zener voltage and provides a low impedance output. Finally, the reference circuitry must reject ambient temperature changes so that the temperature drift of the reference circuitry plus the drift of the zener does not exceed the desired drift limit.

While zener temperature coefficient is obviously critical to reference performance, other sources of drift can easily add as much error as zener — even in voltage references with modest performance of 20 ppm/°C temperature drift. Zener drift and op amp drift add directly to the drift error, while resistor error is only a function of how well the scaling resistors track. Resistors which have a high TC can be used if they track. For a 10V output with a 6.9V zener, the drift contribution of resistor mistracking is about 0.4 since the gain is 1.4. The range of temperature coefficient errors for different components used to make a 10V reference from a 6.9V zener are shown in Table III. Another potential source of error, input supply variations, are negligible if the input is 1% regulated, and the resistor feeding the zener is stable to 1%.

Less frequently specified sources of error in voltage reference zeners are hysteresis and stress sensitivity. Stress on either a zener-diode junction or the series-temperature-compensating junction will cause voltage shifts. The axial leads on discrete devices can transmit stress from outside the package to the junction, causing 1 mV to 5 mV shifts.

Temperature cycling the discrete zener can also induce non-reversible changes in zener voltage. If a zener is heated from 25°C to 100°C and then back to 25°C, the zener voltage may not return to its original value. This is because the temperature cycle has permanently changed the stress in the die, changing the voltage. This effect can be as high as 5 mV in some diodes and may be cumulative with many temperature cycles. The new planar IC zeners, such as the LM199 (temperature stabilized) or the LM129 are insensitive to stress and show only about 50 μV of hysteresis for a 150°C temperature cycle since the package does not stress the silicon chip.

DESIGNING THE REFERENCE

If moderate temperature performance such as 20 ppm/°C is all that is needed, 2 different approaches can be used in the reference design. In the first, the temperature drift error is split equally between the zener and the amplifier or scaling resistors. This requires a moderately low drift zener and op amp with 10 ppm resistors.

TABLE I. Maximum Allowable Reference Drift for 1/2 Least Significant Bits Error of Binary Coded Converter

TEMP CHANGE	BITS					
	6	8	10	12	14	
25°C	310	80	20	5	1.25	ppm/°C
50°C	160	40	10	2.5	0.6	ppm/°C
100°C	80	20	5	1.2	0.3	ppm/°C
125°C	63	16	3	1	0.2	ppm/°C

TABLE II. Maximum Allowable Reference Drift for 1/2 Digit Error of Digital Meters

TEMP CHANGE	DIGITS								
	2	2 1/2	3	3 1/2	4	4 1/2	5	5 1/2	
25°C	200	100	20	10	2	1	0.2	0.1	ppm/°C
5°C			100	50	10	5	1	0.5	ppm/°C

*0.01%/°C = 100 ppm/°C, 0.001%/°C = 10 ppm/°C, 0.0001%/°C = 1 ppm/°C

TABLE III. Drift Error Contribution From Reference Components for a 10V Reference

DEVICE	ERROR	10V OUTPUT DRIFT
Zener	**Zener Drift**	
LM199A	0.5 ppm/°C	0.5 ppm/°C
LM199, LM399A	1 ppm/°C	1 ppm/°C
LM399	2 ppm/°C	2 ppm/°C
1N829, LM3999	5 ppm/°C	5 ppm/°C
LM129, 1N823A, 1N827A, LM329A	10–50 ppm/°C	10–50 ppm/°C
LM329, 1N821, 1N825	20–100 ppm/°C	20–100 ppm/°C
Op Amp	**Offset Voltage Drift**	
LM725, LH0044, LM121	1 μV/°C	0.15 ppm/°C
LM108A, LM208A, LM308A	5 μV/°C	0.7 ppm/°C
LM741, LM101A	15 μV/°C	2 ppm/°C
LM741C, LM301A, LM308	30 μV/°C	4 ppm/°C
Resistors	**Resistance Ratio Drift**	
1% (RN55D)	50–100 ppm	20–40 ppm/°C
0.1% (Wirewound)	5–10	2–4 ppm
Tracking 1 ppm Film or Wirewound	–	0.4 ppm/°C

The second approach uses a very low drift zener and allows the buffer amplifier or scaling resistor to cause most of the drift error. This type of design is now made economical by the availability of low cost temperature stabilized IC zeners with virtually no TC. Further, the temperature coefficient of this reference is easily upgraded, if necessary. The 2 reference circuits are shown in *Figure 1a and Figure 1b.*

In *Figure 1a*, an LM308 op amp is used to increase the typical zener output to 10V while adding a worst-case drift of 4 ppm/°C to the 10 ppm/°C of the zener. Resistors R3 and R4 should track to better than 10 ppm bringing the total error so far to 18 ppm. Since the output must be adjusted to eliminate the initial zener tolerance, a pot, R5 and R2 have been added. The loading on the pot by R2 is small, and there is no tracking requirement between the pot and R2. It is necessary for R2 to track R3 and R4 within 50 ppm.

In *Figure 1b*, a low drift reference and op amp are used to give a total drift, exclusive of resistors of 3 ppm/°C. Now the resistor tracking requirement is relaxed to about 50 ppm, allowing ordinary 1% resistors to be used. The circuit in *Figure 1b* is modified easily for applications requiring 3 ppm/°C to 5 ppm/°C overall drift by tightening the tracking of the resistors. For more accurate applications, the Kelvin sensing for both output and ground should be used. For even lower drifts, substituting a 1 μV/°C op amp, 1 ppm tracking resistors and an LM199A zener, overall drifts of 1 ppm/°C can be achieved. In both of the circuits, it is important to remember that the tracking of resistors can, at worst-case, be twice temperature drift of either resistance.

In both circuits, the zener is biased by a single resistor from the supply, rather than from the reference output. This eliminates possible start-up problems and, because of the 1Ω dynamic impedance of the IC zeners, only

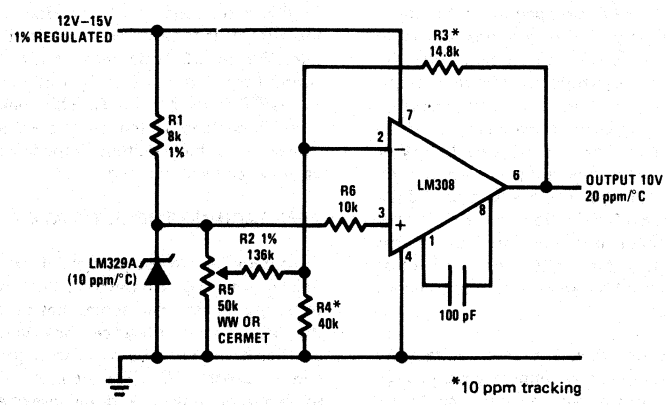


FIGURE 1a. 10V, 20 ppm Reference Using a Low Cost Zener and Low Drift Resistors

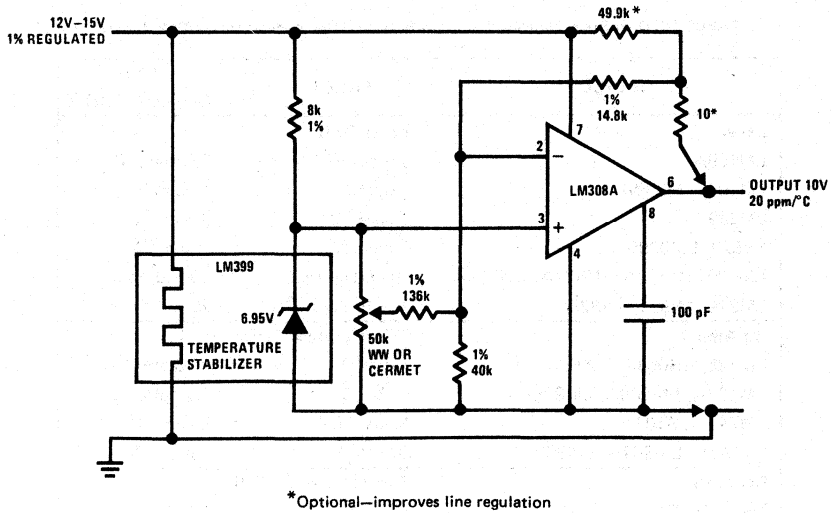


FIGURE 1b. 10V Reference has Low Drift Reference and Standard 1% Resistors. Kelvin Sensing is Shown with Compensation for Line Changes.

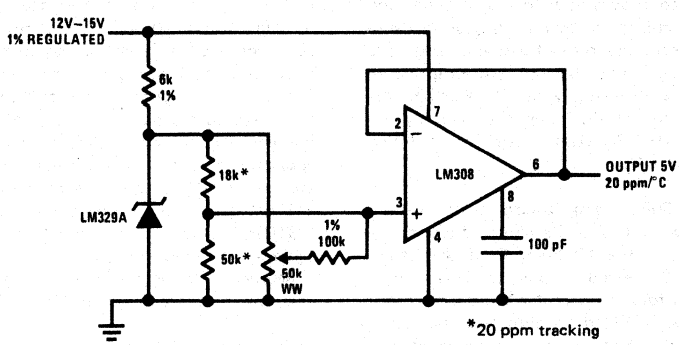


FIGURE 2. Low Voltage Reference

adds about 20 μV of error. Compensation for input changes is shown in *Figure 1b*. Conventional zeners do not allow this biasing. A conventional 5 ppm reference such as the 1N829 has a dynamic impedance of about 15Ω. If it is biased from a resistor from a 1% regulated 15V supply, the operating current can change by 1.7% or 127 μA. This will shift the zener voltage by 1.9 mV or 60 ppm. With the IC zeners operating at 1 mA, a 1% shift in the supply will change the reference by 20 μV or 3 ppm. Further, power dissipation in the IC is only 7 mW, giving low warm-up drift compared to 7.5 mA zeners. The biasing resistor for the IC zener need not be any better than an ordinary 1% resistor since performance is independent of current.

When output voltages less than the zener voltage are desired, the IC zeners significantly simplify circuit design since no auxiliary regulator is needed for biasing. *Figure 2* shows a 5V reference circuit for use with a 15V input. In this case, zener drift contributes proportionally to the output drift while op amp offset drift adds a greater rate. With the 10V reference, 15 μV/°C from the op amp contributed 2 ppm/°C drift, but for the 5V reference, 15 μV/°C adds 3 ppm/°C. This makes op amp choice more important as the output voltage is lowered. Of course, if a high output impedance is tolerable, the op amp can be eliminated.

APPROACHING THE ULTIMATE DRIFT

To obtain the lowest possible drifts, temperature coefficient trimming is necessary. With discrete zeners, the operating current can sometimes be trimmed to change the TC of the reference; however, the temperature coefficient is not always linear or predictable. With the new IC zeners, TC is independent of operating current so trimming must be done elsewhere in the circuit. The lowest drift components should be used since

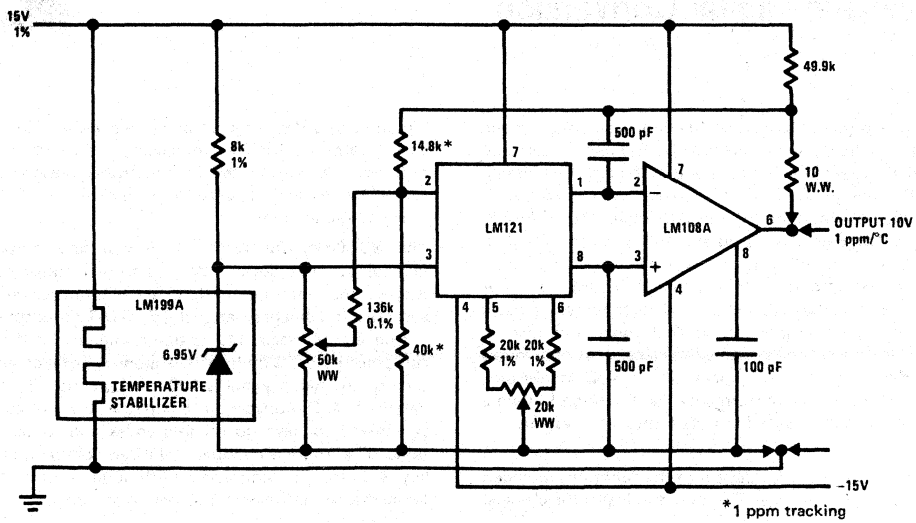


FIGURE 3. Ultra Low Drift Reference

trimming can only remove a linear component of drift. High TC devices can have a highly non-linear drift, making trimming difficult.

Figure 3 shows a circuit suitable for trimming. An LM199A reference with 0.5 ppm/°C drift is used with a 121/108 op amp. Resistors should be 1 ppm tracking to give overall untrimmed drifts of about 0.9 ppm. The 121/108 is a low drift amplifier combination where drift is predictably proportional to offset voltage. An offset can be set for the 108/121 combination to cancel the measured drift with 1 pass calibration.

Trimming procedure is as follows: the zener is disconnected and the input of the op amp grounded. Then the offset of the op amp is nulled out to zero. Reconnecting the zener, the output is adjusted to precisely 10V. A temperature run is made and the drift noted. The op amp will drift 3.6 μV/°C for every 1 mV of offset, so for every 5 μV/°C drift at the output, the offset of the op amp is adjusted 1 mV (1.4 mV measured at the output) in the opposite direction. The output is readjusted to 10V and the drift checked.

Although this trimming scheme was chosen since only a single adjustment is usually required, compensation is not always perfect. Hysteresis effects can appear in resistors or op amps as well as zeners. Best results can be obtained by cycling the circuit to temperature a few times before taking data to relieve assembly stresses on the components. Also, oven testing can sometimes cause thermal gradients across circuits, giving 50 μV to 100 μV of error. However, with careful layout and trimming, overall reference drifts of 0.1 ppm/°C to 0.2 ppm/°C can be achieved.

There are 2 other possible problem areas to be considered before final layout. Good single point grounding is important. Traces on a PC board can easily have 0.1Ω and only 10 mA will cause a 1 mV shift. Also, since these references are close to high-speed digital circuitry, shielding may be necessary to prevent pick-up at the inputs of the op amp. Transient response to pick-up or rapid loading changes can sometimes be improved by a large capacitor (1 μF–10 μF) directly on the op amp output; but this will depend on the stability of the op amp.

Single Chip Data Acquisition System Simplifies Analog-to-Digital Conversion

National Semiconductor
Application Note 193
Jake Buurma
July 1977

Until recently, building an analog data acquisition system required a hardy cross-breed of both analog design and digital design. Now National Semiconductor has simplified the design problem of a data acquisition system with the introduction of the ADC0816 (MM74C948). This CMOS device incorporates many of the standard features of a data acquisition system onto a single chip. Included on-chip is an 8-bit analog-to-digital converter with bus oriented outputs, a 16-channel expandable multiplexer, provisions for external signal conditioning, and logic control for systems interface. This chip marks the advent of a new generation in A/D converters, bringing versatility, performance, and economy using a technology ideally suited to data acquisition systems.

Figure 1 shows a block diagram of the functions provided within a single package. The chip duplicates the classical structure of a data acquisition system while relieving the user from multichip interface and compatibility problems. A wide range of functional options allows extremely versatile operation of the device in a wide range of applications.

The ADC0816 uses National's low voltage, metal gate technology. The device operates from a single +5 volt supply and features a 16-channel multiplexer with address input latches, latched TRI-STATE® outputs and a true eight-bit-accurate analog-to-digital converter. It consumes only 20 milliwatts of power. Total conversion time of an analog signal is 100 microseconds. By using a patented A/D conversion technique the converter is guaranteed to have no missing codes and to be monotonic. The internal chopper stabilized comparator is the key element in minimizing both long term drift and temperature coefficients of other error terms.

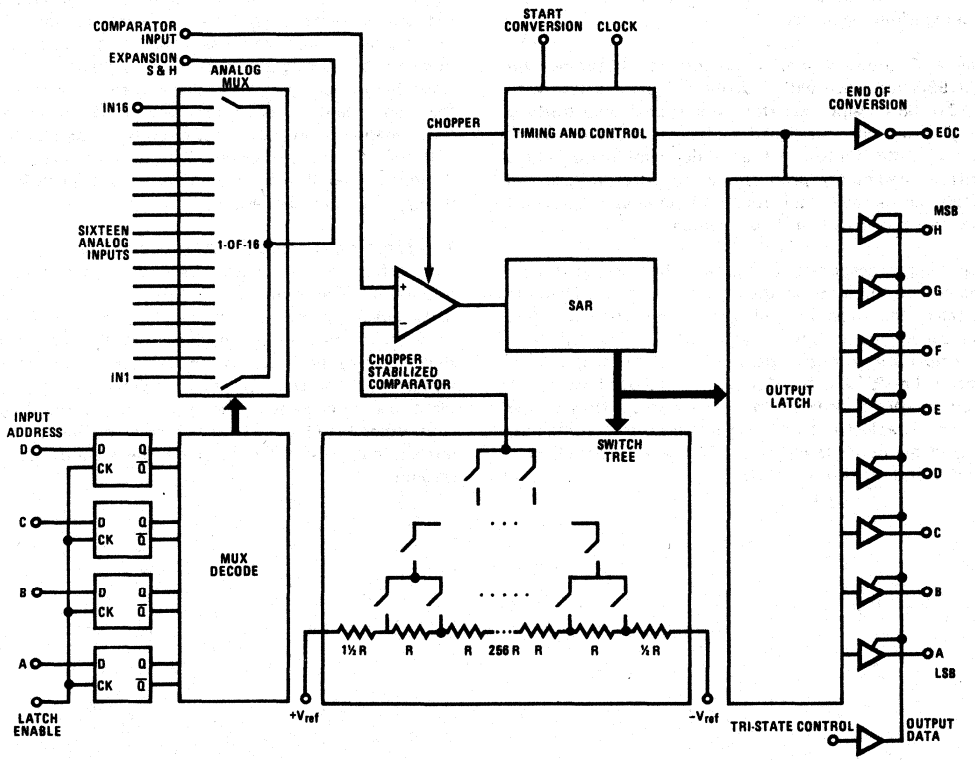


Figure 1. ADC0816/MM74C948 Block Diagram

Figure 2 shows a typical application employing the ADC0816 for use in a microprocessor-based environmental control system. In this system the microprocessor can select a channel, monitor a particular sensor reading, convert that signal to a digital word, and make a system decision based upon that input. Many other areas of process control, machine control, or multi-input analog system can utilize this basic configuration.

THE CONVERTER

The heart of this single-chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into three major sections: the 256R ladder network, the successive approximation register, and the comparator.

The 256R ladder network approach was chosen over the conventional R/2R ladder because of its inherent monotonicity. Monotonicity is particularly important in closed-loop feedback control systems. A non-monotonic relationship can cause oscillations that could be catastrophic. Additionally, the 256R network does not cause load variations on the reference voltage.

Figure 3 shows a comparison of the output characteristic for the two approaches with a variation in the ladder resistance. In the 256R approach with unequal or shorted resistors the slope of the output transfer function cannot be different from the slope of the analog input. For the R/2R ladder network, mismatches in the resistor values can cause the slope of the output digital code to be different from the analog input signal.

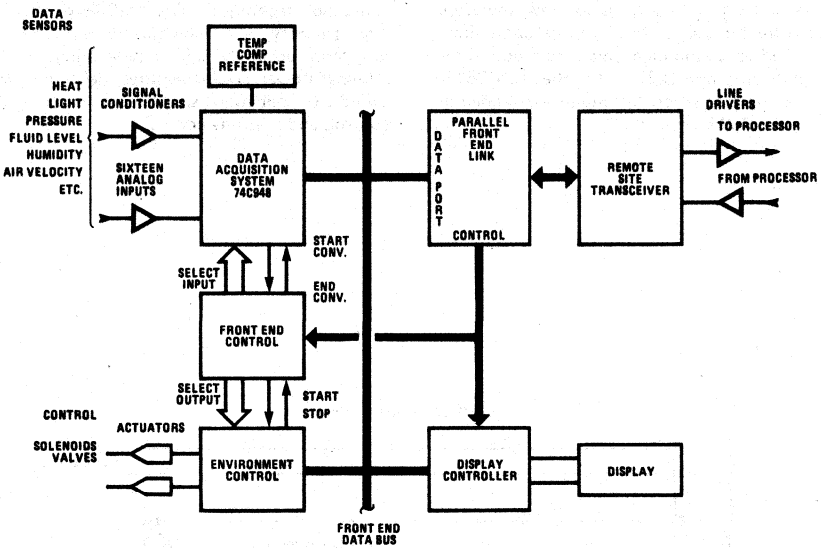


Figure 2. Remote Environmental Control System

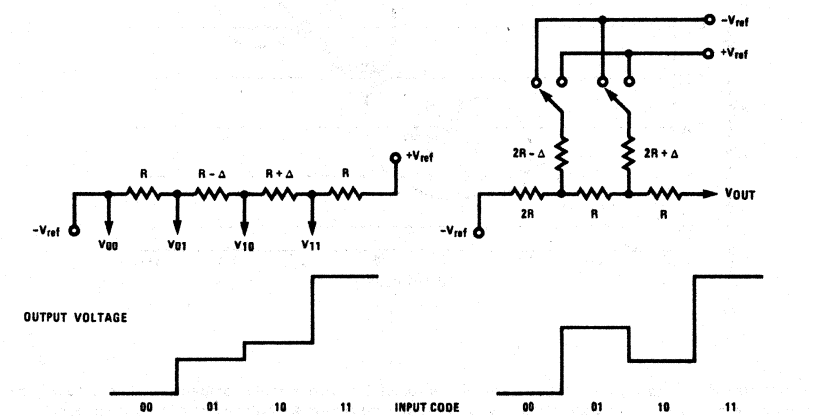


Figure 3. 2^nR and R2R Ladder Transfer Curves. In a 2^nR ladder the most unequal resistors can do is cause a nonuniform voltage step. Since a single voltage is across the ladder it must be monotonic. In a R2R ladder unequal resistors may cause a sign change in the transfer curve, causing it to be nonmonotonic.

The bottom resistor and the top resistor of the ladder network in figure 4 are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs eight iterations to approximate the input voltage. For any SAR-type converter, n interations are required for an n-bit converter. Figure 4 shows a typical example of a 3-bit converter with an input voltage of 1/4 full-scale. Since the initial approximation at 7/16 of full-scale is too high, a zero is posted for the most significant bit (MSB). The second approximation is too low, therefore a one is posted for the second bit. The final approximation is determined to be too high, so a zero is posted for the least significant bit (LSB). In the ADC0816/MM74C948 the approximation technique is extended to eight bits using the 256R network.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the respectability of the device. A chopper stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long-term drift, and input offset errors.

The design of this A/D converter has been optimized by incorporating the most desirable aspects of several conversion techniques. The ADC0816 offers high speed, high accuracy, low temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications such as process control, industrial control, and machine control.

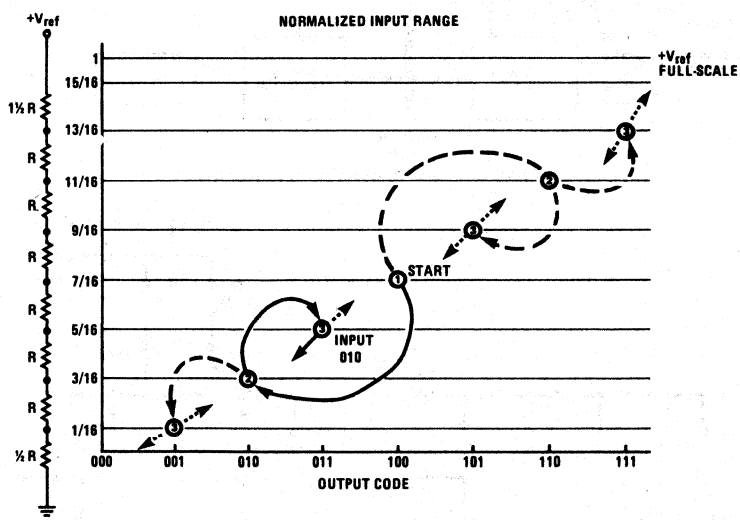


Figure 4. Offset-Adjusted 8 R Ladder gives ±½ LSB quantizing error of 3 bits with three comparisons. The output code is derived by posting a one when upward arrows are followed and a zero when downward arrows are followed to the input voltage.

CMOS A/D Converter Chips Easily Interface to 8080A Microprocessor Systems

National Semiconductor
Application Note 200
Jake Buurma
March 1978

SUMMARY

This paper describes techniques for interfacing National Semiconductor's new ADC3511 and ADC3711 microprocessor compatible analog-to-digital converter chips to 8080A microprocessor systems. The hardware interface and the software interrupt service routine will be described for single and multiple A/D converter data acquisition systems.

INTRODUCTION

The recent introduction of monolithic digital voltmeter chips has encouraged designers to consider their use as analog-to-digital converters in data acquisition systems. While the high accuracy afforded at low cost was attractive, certain difficulties in applying these devices in digital systems were encountered. Most of these difficulties were due to the DVM chip's output structure being oriented towards driving 7-segment displays with internally generated digit scanning rates. National Semiconductor has recently introduced a family of monolithic CMOS A/D converters—2 of these devices are directed towards LED display DPM and DVM applications (ADD3501 3 1/2-digit DPM and ADD3701 3 3/4-digit DPM) while the other 2 (ADC3511 3 1/2-digit A/D and ADC3711 3 3/4-digit A/D) have addressable BCD outputs. These last 2 devices allow easy interface to microprocessor and calculator-oriented (COPS) systems.

Single or multiple channel monitoring of physical variables can be achieved with high accuracy despite the lack of complexity and low overall cost.

A/D CONVERSION

All A/D converters in this family operate from a single 5V supply and convert inputs from 0 to ±2V. The converters use a pulse-width modulation technique which requires no precision components and exhibits low offset, low drift, high linearity and no rollover error. An additional advantage is that the voltage reference is of the same polarity as the supply.

Two resolutions are offered: the 3 1/2-digit types divide the input into 2,000 counts plus sign, while the 3 3/4-digit types provide 4,000 counts plus sign which is roughly equivalent to the resolution of a 12-bit plus sign binary converter. The 3 1/2-digit converters require 200 ms per conversion; 3 3/4-digit types require 400 ms.

The converters handle negative inputs by internally switching the inputs and forcing the sign bit low. While this technique allows conversion of positive and negative inputs with only a single supply, the supply must be isolated from the inputs. Without an isolated supply, only positive voltages may be converted.

The basic converter is shown in *Figure 1*. The actual conversion technique is described in Appendix A.

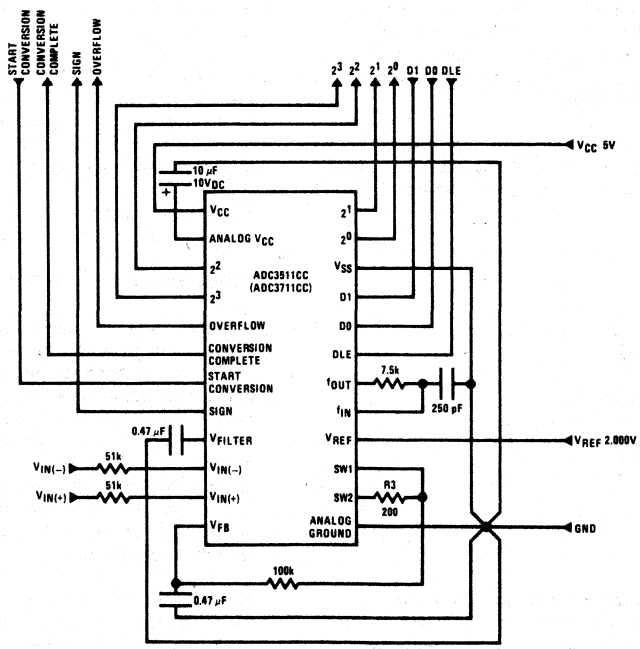


FIGURE 1. Basic A/D Converter

BCD OUTPUT DESCRIPTION

The ADC3511 and ADC3711 present the output data in BCD form on a single 4-line output port, plus a separate sign output. The desired digit is selected by a 2-bit address which is latched by a high level at the Digit Latch Enable input (DLE); a low level at DLE allows flow thru operation. Since the output is BCD, it is compatible with many standard instruments and can easily be converted into binary by the processor if this format should be desired. Overrange inputs are indicated by a hexidecimal "EEEE" plus an Overflow output.

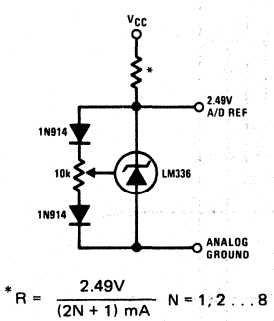
A new conversion is begun by a positive pulse or high level at the Start Conversion (SC) input. The analog section of the converter continuously tracks the analog input. The Start Conversion command controls only the transfer of new data to the output latches, consequently the delay from the SC pulse to the Conversion Complete (CC) signal may vary from several milliseconds to several hundred milliseconds. In interrupt driven systems the delay is no problem, since the processor does not execute delay instructions while waiting for the data. However, if in-line or program I/O is used where the program waits for the data to be ready, the maximum delay between SC and CC must be programmed into the wait routine. This type of I/O is therefore not as efficient as interrupt I/O.

The CC output goes low immediately after the SC pulse. At the end of a conversion, CC goes high and remains high until a new conversion is initiated. Continuous conversion operation is obtained by tying the SC input to V_{CC}.

REFERENCE VOLTAGE

The 2.000V reference is derived from the LM336, a recently announced monolithic reference which provides 2.5V with low drift at low cost. This active reference is adjusted for minimum thermal drift of about 20 ppm/°C by using a third terminal on the device to adjust its output to 2.490V.

Total reference current consumption is low, as the LM336 requires only 1 mA of bias current, and the resistor divider about 2 mA. The reference circuit is shown in *Figure 2*. One reference can be used for many A/D's. The value of the upper series resistor R1 depends on the number of converters used.



$$*R = \frac{2.49V}{(2N + 1)\ mA} \quad N = 1, 2 \ldots 8$$

FIGURE 2. A/D Converter Reference. The 10k Pot is Adjusted to a Voltage of 2.49V on the Output; at this Voltage Minimum Drift Occurs. The Reference can Supply up to 8 A/D Converters.

A SINGLE CHANNEL CONVERTER

A complete A/D port is seen in *Figures 3 and 4. Figure 3* shows a Dual Polarity converter and *Figure 4* a Positive Only Polarity converter. Each port contains an A/D converter, TRI-STATE® bus driver, and 2 gates to control I/O. This A/D port is easily used in single or multichannel systems. In multichannel systems a converter is used on every channel allowing digital multiplexing of the outputs.

Data from the A/D converter in a single channel system is easily processed using an OUT command to start a conversion and IN commands to read the data after the microprocessor has been interrupted by a Conversion Complete.

As seen in *Figure 5*, a single channel A/D port uses a 6-bit bus comparator to decode its assigned peripheral address from the lower address bits of the 8080A address bus.

When an interrupt is received, the present status of the processor is stored on the stack memory by a series of push commands. The interrupt is serviced by reading digit 4 (MSD) into the processor and checking the overflow bit. If the overflow bit is high, the converter input has exceeded its range and an error signal is generated, indicating that scaling must be done to attenuate the input signal. If the OFL is low, the sign bit is then checked to determine the polarity of the conversion. If the sign bit is low, a "1" is added to the MSB of digit 4. Since this bit would normally be low, (maximum converter range allows MSB $\leq$ 3 or 0011) a "1" in this position is used to denote a negative input voltage. The 4 bits of digit 4 which now include the sign are shifted into the upper half of the first byte and the 4 bits of digit 3 are packed into the lower half. Similarly, digits 2 and 1 are packed into the second byte and both bytes stored in memory.

Figure 6 and routine 1 are the flow chart and assembly language routine used to implement this action.

8-CHANNEL A/D WITH SOFTWARE PRIORITY

The basic A/D port can easily be expanded to multiple channel systems. An 8-channel system is seen in *Figure 7*. This system interrupts the processor when one of the Conversion Complete outputs goes high. The processor saves the current status and reads the status word of the A/D system. The status word is then compared to a priority table. Each level in the table corresponds to a priority level with high priority converters which are first in the table. If 2 or more converters have the same priority and are ready at the same time, the converter with the highest number gets serviced first.

The program determines which service routine to use by the bit position of "1's" in the status word. The routine loads the address pointer to digit 4 of the selected converter. The program then calls a subroutine which

goes through the process of checking overflow, sign and packs 4 BCD digits into 2 bytes. These 2 bytes are then stored in a table in the memory directly above the converter addresses. After a channel is serviced, the original processor status is restored and the interrupt enabled. If additional channels need service, they immediately interrupt so the new status word is then read and a new priority established.

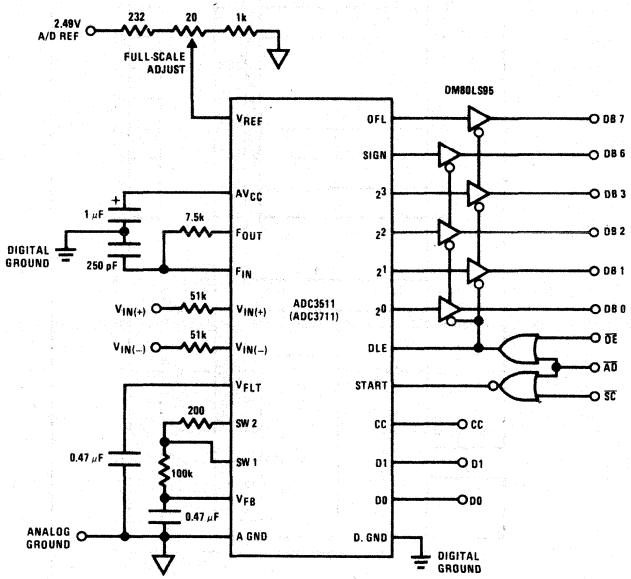


FIGURE 3. Dual Polarity A/D Requires that Inputs are Isolated from the Supply. Input Range is ±1.999V.

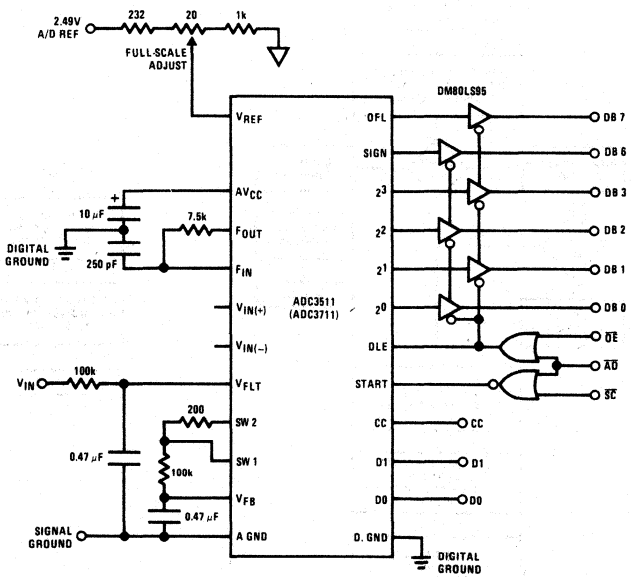


FIGURE 4. Positive Polarity A/D Operating from 5V Supply. Input Range is +1.999V.

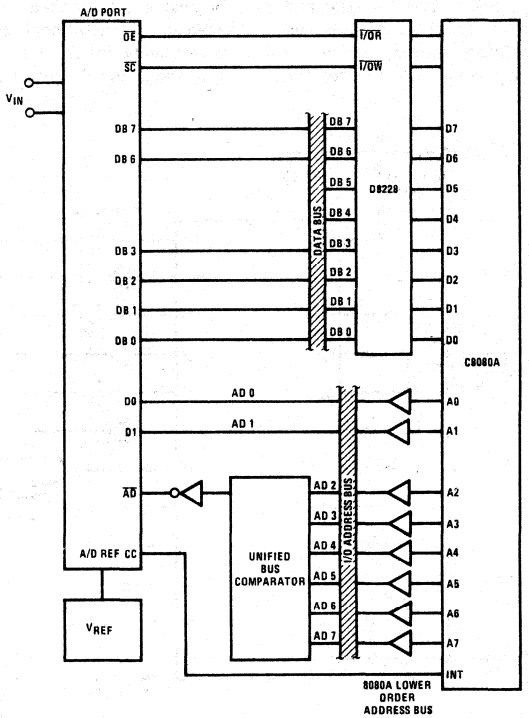


FIGURE 5. Single Channel A/D Interface with Peripheral Mapped I/O

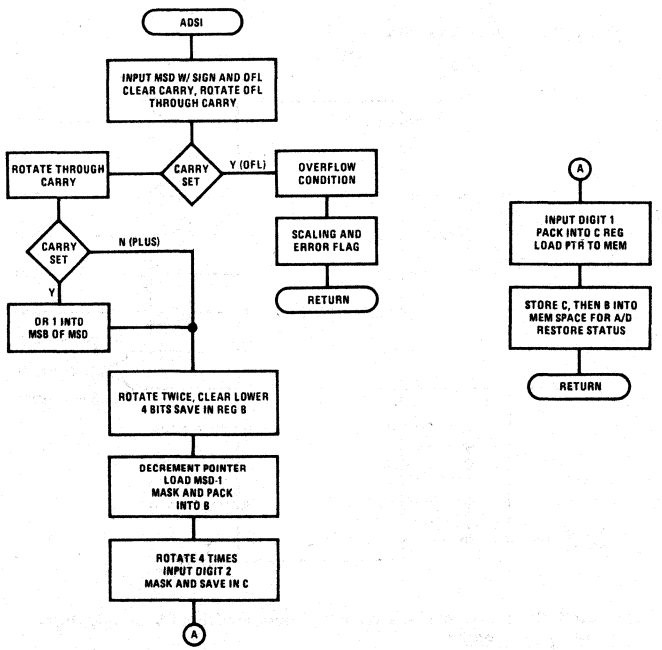


FIGURE 6. Flow Chart for Single Channel A/D Converter

LABEL	OPCODE	OPERAND	COMMENT
ADIS:	PUSH	PSW	; A/D interrupt service
	PUSH	H	; save
	PUSH	B	; current status
	IN	ADD 4	; input A/D digit 4
	IN	ADD 4	; delay
	ORA		; reset carry
	RAL		; rotate OFL thru carry
	JC	OFL	; overflow condition
	RAL		; rotate sign thru carry
	JC	PLUS	; positive input
	ORI	20H	; OR 1 into MSB, neg input
PLUS:	RAL		; shift
	RAL		; into position
	ANI	FO	; mask lower bits
	MOV	BA	; save in B
	IN	ADD 3	; input digit 3
	IN	ADD 3	; delay
	ANI	OF	; mask higher bits
	OR	B	; pack into B
	MOV	B, A	; save in B
	IN	ADD 2	; input digit 2
	IN	ADD 2	; delay
	RAL		; rotate
	RAL		; into
	RAL		; upper
	RAL		; 4 bits
	ANI	FO	; mask lower bits
	MOV	C, A	; save in C
	IN	ADD 1	; in digit 1
	IN	ADD 1	; delay
	ANI	OF	; mask upper bits
	OR	C	; pack
	MOV	C, A	; save in C
	LXI	H, ADMS	; load ptr to A/D Mem, space
	MOV	M, C	; save C in memory
	INX	H	; point next
	MOV	M, B	; save B in memory
	OUT	ADD 1	; start new conversion
	POP	B	; restore
	POP	H	; previous
	POP	PSW	; status
	EI		; enable interrupts
	RET		; return to main program

Routine 1. Single Channel Interrupt Service Routine

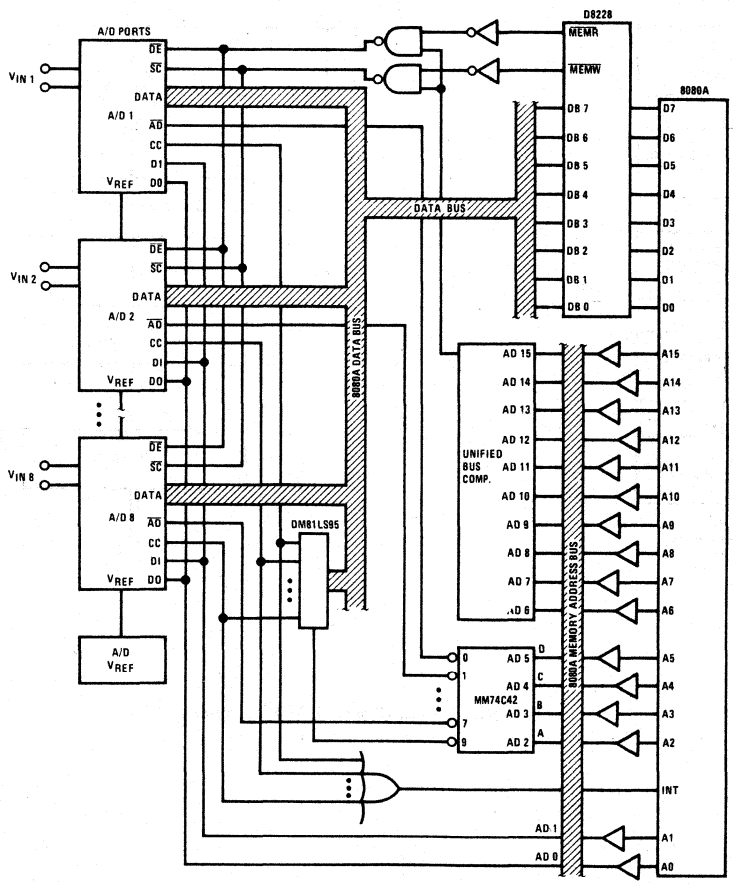


FIGURE 7. 8-Channel A/D System with Maskable Priority Interrupt Using Memory Mapped I/O

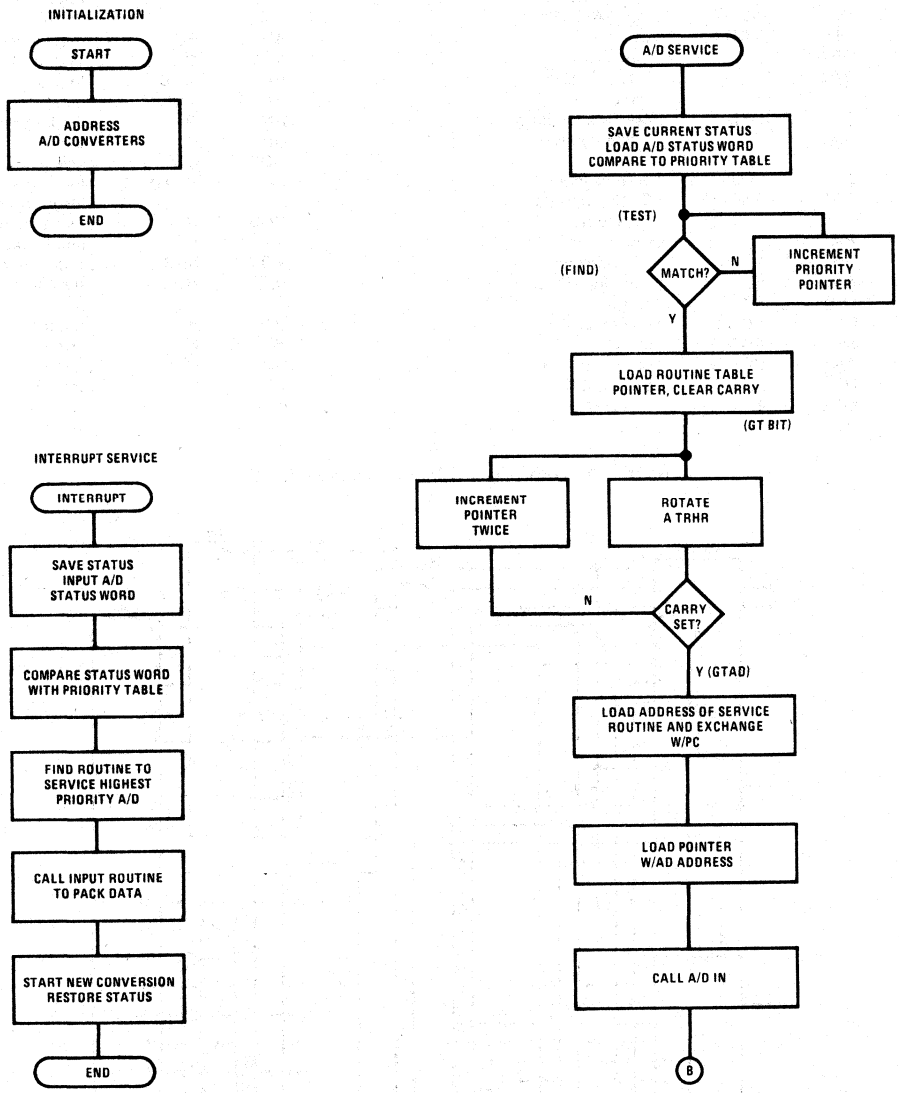


FIGURE 8. Flow Charts of A/D Routines

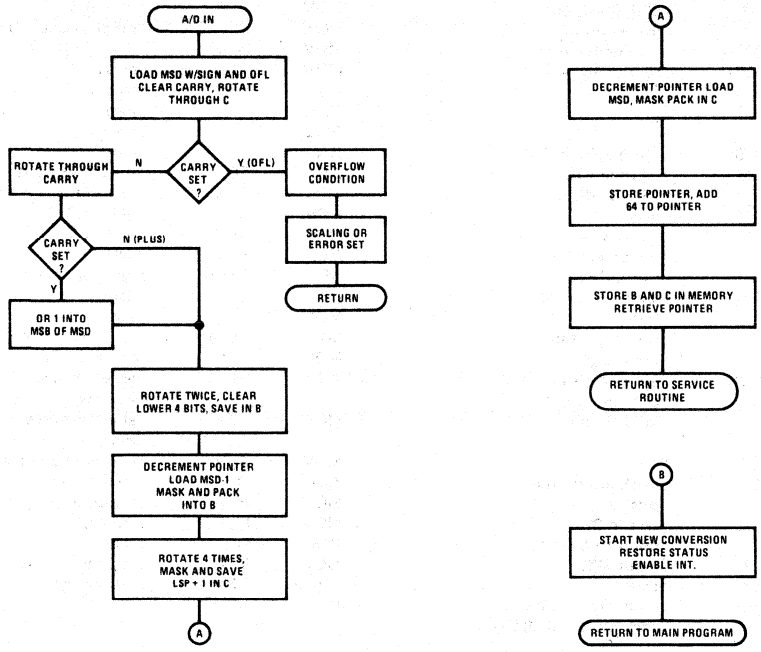


FIGURE 8. Flow Charts of A/D Routines (Continued)

```
LABEL   OPCODE   OPERAND     COMMENT
IAD:    PUSH     PSW        ; interrupt from A/D
        PUSH     H          ; save H & L on
                            stack
        PUSH     B          ; save B & C on
                            stack
        PUSH     D          ; save D & E on
                            stack
        LXI      H, ADWD    ; pickup A/D status
                            word
        MOV      6, M       ; move word into B
        LXI      H, PRTBL   ; pickup priority tbl
                            pointer
TEST:   MOV      A, B       ; place status word
                            in accum.
        ANA      M          ; mask with priority
                            table
        JNZ      FIND       ; match jump to
                            Find
        INX      H          ; point to lower
                            priority
        JMP      TEST       ; try again
FIND:   LXI      H, RTBL    ; pickup routine tbl
                            pointer
        ORA      A          ; reset carry
GTBIT:  RAR                 ; rotate thru carry
        JC       GTAD       ; bit was found
        INX      H          ; point to
        INX      H          ; next routine
        JMP      GTBIT      ; try again
GTAD:   MOV      E, M       ; move first byte
                            into E
        INX      H          ; point to next byte
        MOV      D, M       ; move second byte
                            into D
        XCGH                ; exchange DE, HL
        PCHL                ; jump to input
                            routine
INAD1:  LXI      H, AD1     ; pickup pointer to
                            A/D 1
        CALL     ADIN       ; call common input
                            routine
        MOV      M, A       ; start new conversion
        JMP      DONE       ; all done
INAD2:  LXI      H, AD2     ; pickup pointer to
                            A/D 2
        CALL     ADIN       ; call input routine
        MOV      M, A       ; start new conver-
                            sion
        JMP      DONE       ; all done
        .
        .
        .
DONE:   POP      D          ; restore D
        POP      B          ; restore B
        POP      H          ; restore H
        POP      PSW        ; restore PSW
        EI                  ; enable interrupts
        RET                 ; return to main
                            program
PRTBL:  DB       04H        ; 0000C100 AD3
                            highest priority
        DB       03H        ; 00000011 AD2 &
                            AD1 next priority
        .
        .
        .
```

Routine 2. 8-Channel Interrupt Service Routine with Software Priority

```
LABEL   OPCODE  OPERAND   COMMENT
PRTBL:  DB      10H       ; 00010000 AD5
                          lowest priority
RTBL:   DW      1000H     ; routine for A/D 1
        DW      100CH     ; routine for A/D 2
        .
        .
        .
        DW      1060H     ; routine for A/D 8
ADIN:   MOV     A, M      ; input MSD plus
                          OFL & SIGN
        MOV     A, M      ; delay
        ORA     A         ; reset carry
        RAL               ; rotate left thru
                          carry, OFL
        JC      OFL       ; jump to overflow
                          if set
        RAL               ; rotate left thru
                          carry, sign
        JC      PLUS      ; jump to plus if set
        OR1     20H       ; OR1 into BCD,
                          MSB for minus
PLUS:   RAL
        RAL
        ANI     FO        ; mask lower order
                          bits
        MOV     B, A      ; save in B
        DCR     H         ; point to MSD-1
        MOV     A, M      ; input MSD-1
        MOV     A, M      ; delay
        ANI     OF        ; mask higher 4 bits
        OR      B         ; pack MSD and MSD-1

LABEL   OPCODE  OPERAND   COMMENT
        MOV     B, A      ; save in B
        DCR     H         ; point to LSD + 1
        MOV     A, M      ; input LSD + 1
        MOV     A, M      ; delay
        RAL               ; rotate
        RAL               ; into
        RAL               ; upper
        RAL               ; 4 bits
        ANI     FO        ; mask lower bits
        MOV     C, A      ; save in C
        DCR     H         ; point to LSD
        MOV     A, M      ; input LSD
        MOV     A, M      ; delay
        ANI     OF        ; mask upper bits
        OR      C         ; pack
        MOV     C, A      ; save in C
        SHLD    TEMP      ; store HL in temp
        MOV     A, L      ; move L in accum.
        ACI     64        ; generate lower
                          address
        MOV     L, A      ; above memory
                          mapped
        MOV     A, H      ; converter addresses
        ACI     0         ; include carry
        MOV     H, A      ; to upper bits
        MOV     M, C      ; store C
        INX     H         ; then
        MOV     M, B      ; store B
        LHLD    TEMP      ; retrieve HL
        RET               ; return
```

Routine 2. 8-Channel Interrupt Service Routine with Software Priority (Continued)

ADJUSTMENT AND TESTING

Adjustment and testing of a single channel A/D is done by monitoring the memory space where the interrupt routine stores the data word. The microprocessor is forced to loop around a section of program with interrupts enabled. As the input voltage of the converter is changed, this data word should also change as the converter updates it. A precision voltage reference is connected to the input of the A/D and incremental voltage steps are applied. The A/D data word should also change according to the voltage steps.

At full-scale input voltage, the data word should be at its maximum value. If not, check the full-scale adjust on the A/D by adjusting it so the OFL bit goes high when the input is exactly 2.000V.

Multichannel systems are more difficult to check. Start by individually checking the full-scale adjustments so the converters overflow at 2.000V. Check the software priority routine by forcing all status bits of the status word high. This corresponds to all converters being ready at the same time, a very unlikely worst-case condition. The microprocessor should respond by outputting the address of all 4 digits of the A/D port with the highest priority along with the $\overline{\text{memR}}$ strobes, then with a $\overline{\text{memW}}$ strobe to start a new conversion. The next highest priority converter should then receive its addresses and $\overline{\text{memR}}$ strobes and so on down the line.

Once the priority routine has been debugged, each data word is monitored as the input to its converter is adjusted. Since a common input routine is used, once 1 channel operates, all the other channels should also.

Debugging may most easily be done by single stepping through the program at these critical areas. No timing problems should be encountered since the A/D port appears to be a standard peripheral or memory. In the ADC3511 and ADC3711 the desired output is merely addressed the same as a memory location.

The memory requirements of the interface depends, of course, on the complexity of the system. The single channel converter requires approximately 60 bytes of program storage plus 2 bytes for data storage and 4 peripheral addresses.

The multichannel system requires about 40 bytes for the priority routine and 10 bytes of program for each converter routine. The common input routine requires about 50 bytes of program and is used by all the converter routines in the form of a subroutine.

Memory mapped I/O causes 64 memory locations to be used to input an 8-channel system. The data space is located directly above the address space for the converters and 16 memory locations are used to store the data for 8 converters.

CONCLUSION

The ADC3511 and ADC3711 microprocessor compatible A/D converters eliminate the difficulties previously encountered in applying DPM chips to microprocessor systems. The low parts count and low cost per channel make distributed or remote A/D conversion practical for a variety of data acquisition applications.

APPENDIX A

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure A1*. The output of SW 1 is either at V_{REF} or 0V, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high, then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge, the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V, the comparator output will switch high. On the rising edge of the next clock, the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW 1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The low pass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

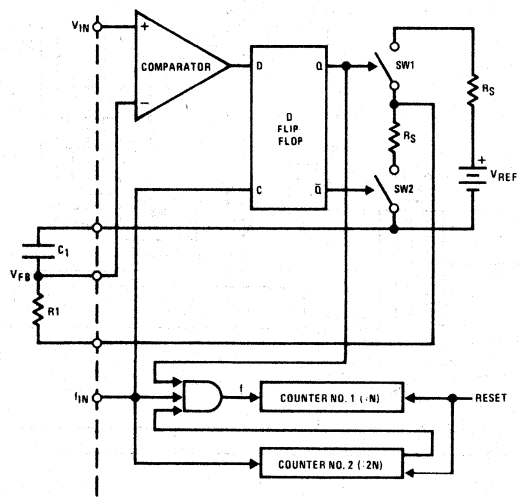
The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{count} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.
For the ADC3711 N = 4000.



$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE A1. Analog Loop Schematic Pulse Modulation A/D Converter

ELECTRICAL CHARACTERISTICS

ADC3511CC, ADC3711CC $4.75 \leq V_{CC} \leq 5.25V$; $-40°C \leq T_A + 85°C$, f_C = 5 conv./sec (ADC3511CC): 2.5 conv./sec (ADC3711CC); unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
	Non-Linearity	(Note 3)				
		V_{IN} = 0–2V Full-Scale	−0.05	±0.025	0.05	% of Full-Scale
		V_{IN} = 0–200 mV Full-Scale				
	Organization Error		−1		0	Counts
	Offset Error	V_{IN} = 0V, (Note 4)	−0.5	1.0	3.0	mV
	Rollover Error		−0		0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	T_A = 25°C	−5	1	5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals are given for T_A = 25°C.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore, 0.025% of full-scale = 1/2 counts and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore, 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 counts.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

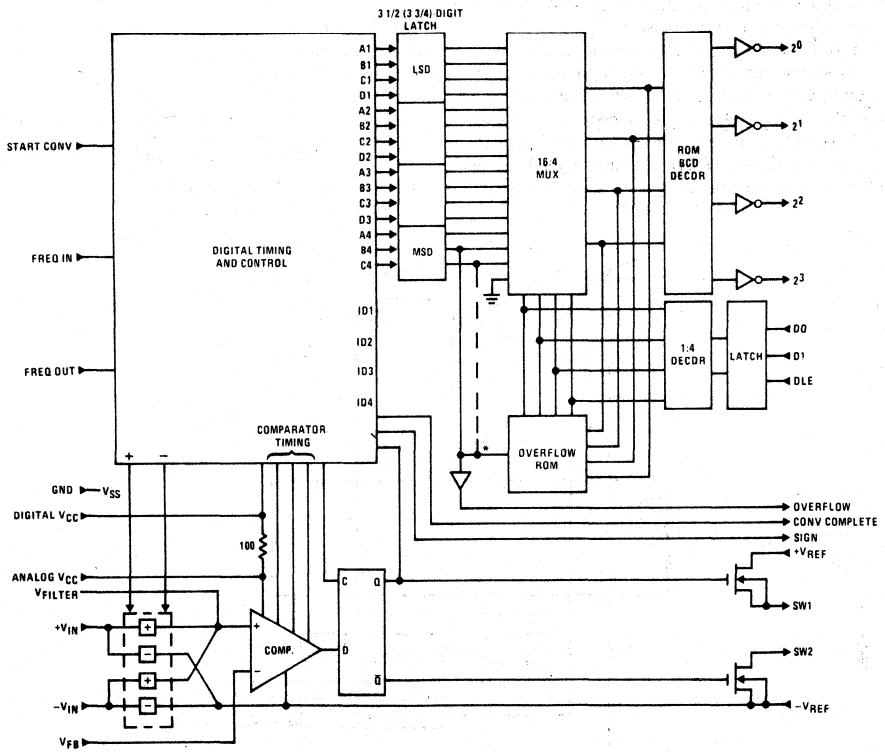


FIGURE A2. ADC3511 3 1/2-Digit A/D (*ADC3711 3 3/4-Digit A/D) Block Diagram

A Digital Multimeter Using the ADD3501

National Semiconductor
Application Note 202
Carson Chen
July 1978

INTRODUCTION

National Semiconductor's ADD3501 is a monolithic CMOS IC designed for use as a 3 1/2-digit digital voltmeter. The IC makes use of a pulse-modulation analog-to-digital conversion scheme that operates from a 2V reference voltage, functions with inputs between 0V and ±1.999V and operates from a single supply.

The conversion rate is set by an external resistor/capacitor combination, which controls the frequency of an on-chip oscillator. The ADD3501 directly drives 7-segment multiplexed LED displays, aided only by segment resistors and external digit buffers. The ADD3501 blanks the most significant digit whenever the MSD is zero; and, during overrange conditions, the display will read either +OFL or −OFL (depending on the polarity of the input).

These characteristics make the ADD3501 suitable for use in low-cost instrumentation. An example of such use is the inexpensive, accurate, digital multimeter (DMM) presented here—an instrument that measures AC and DC voltages and currents, and resistance.

CIRCUIT DESCRIPTION

Figure 1 shows the circuit diagram of the ADD3501-based DMM, and Table I summarizes its measurement capabilities. Since the accuracy of the ADD3501 is ±0.05%, the DMM's performance is mainly determined by the choice of discrete components.

Supporting the ADD3501 is a DS75492 digit driver, an NSB5388 LED display, and an LM340 regulator for the V_{CC} supply. A 2V reference voltage—derived from the LM336 reference-diode circuitry—permits the 3 1/2-digit system a 1 mV/LSD resolution (i.e., the ADD3501's full-scale count of 1999 or 1999 mV).

DC Voltage Measurement. The DMM's user places the (+) and (−) probes across the voltage to be measured, and sets the voltage range switch as necessary. This switch scales the input voltage, dividing it down so that the maximum voltage across the ADD3501's V_{IN} and $V_{IN}-$ pins is limited to 2 V full-scale on each input range. The ADD3501 performs an A/D conversion, and displays the value of the DMM's input voltage. The instrument's input impedance is at least 10 MΩ on all DC voltage ranges. Except for the 2V range, the DMM's survival voltage—the maximum safe DC input—is in excess of 1 kV. On the 2V range, the maximum allowable input is 700V.

AC Voltage Measurement. Switching the DMM to its AC VOLTS mode brings the circuit of *Figure 2* into function. This circuit operates as an averaging filter to generate a DC output proportional to the value of the rectified AC input; this value, in turn, is "tapped down" by R5 to a level equivalent to the input's rms value, which is the value displayed by the DMM.

Op amp A3 is simply a voltage follower that lowers the input-attenuator's source impedance to a value suitable to drive into A4. This impedance conversion helps eliminate some of the possible offset-voltage problems (the A4 input-offset-current source impedance IR drop, for example) and noise susceptibility problems as well. C1 blocks the DC offset voltage generated by A3.

A4 and A5 comprise the actual AC-to-DC converter; to see how it works refer again to *Figure 2*, and consider first its operation on the negative portion of an AC input signal. At the output of A4 are 2 diodes, D1 and D2, which act as switches. For a negative input to A4's inverting input, D1 turns on and clamps A4's output to 0.7V, while D2 opens, disconnecting A4's output from A5's summing point (the inverting input). A5 now operates as a simple inverter: R2 is its input resistor, R5 its feedback resistor, and its output is positive.

Now consider what happens during the positive portion of an AC input. A4's output swings negative, opening D1 and closing D2, and the op amp operates as an inverting unity-gain amplifier. Its input resistor is R1, its feedback resistor is R3, and its output now connects to A5's summing point through R4. D2 does not affect A4's accuracy because the diode is inside the feedback loop.

A positive input to A4 causes it to pull a current from A5's summing point through R4 and D2; the positive input also causes a current to be supplied to the A5 summing point through R2. Because A4 is a unity-gain inverter, the voltage drops across R2 and R4 are equal, but opposite in sign. Since the value of R2 is double that of R4, the net input current at A5's summing point is equal to, but opposite, the current through R2. A5 now operates as a summing inverter, and yields—again—a positive output. (R6 functions simply to reduce output errors due to input offset currents.)

Thus, the positive and negative portions of the DMM's AC voltage input both yield positive DC outputs from A5. With C2 connected across R5 as shown, the circuit becomes an averaging filter. As already mentioned, the tap on R5 is set so that the circuit's DC output is equivalent to the rms value of the DMM's AC voltage input, which is the value converted and displayed by the ADD3501.

DC Current Measurement. To make a DC current measurement, the user inserts the DMM's probes in series with the circuit current to be measured and selects a suitable scale. On any scale range, the DMM loads the measured circuit with a 2V drop for a full-scale

TECHNICAL SPECIFICATIONS

DC VOLTS	< ±1% ACCURACY
RANGES	2V, 20V, 200V, 2 kV
INPUT IMPEDANCE	2V RANGE, >10MΩ
	20V TO 2 kV RANGE, 10MΩ
AC RMS VOLTS	< ±1% ACCURACY
RANGES	2V, 20V, 200V, 2 kV
	(40 TO 5 kHz SINEWAVE)
DC AMPS	< ±1% ACCURACY
RANGES	200 μA, 2 mA, 20 mA, 200 mA, 2A
AC RMS AMPS	< ±1% ACCURACY
RANGES	200 μA, 2 mA, 20 mA, 200 mA, 2 A
OHMS	< ±1% ACCURACY
RANGES	200 Ω, 2 kΩ, 20 kΩ, 200 kΩ, 2 MΩ

Note 1: All V_{CC} connections should use a single V_{CC} point and all ground/analog ground connections should use a single ground/analog ground point.

Note 2: All resistors are 1/4 watt unless otherwise specified.

Note 3: All capacitors are ±10%.

Note 4: All op amps have a 0.1 μF capacitor connected across the V+ and V− supplies.

Note 5: All diodes are 1N914.

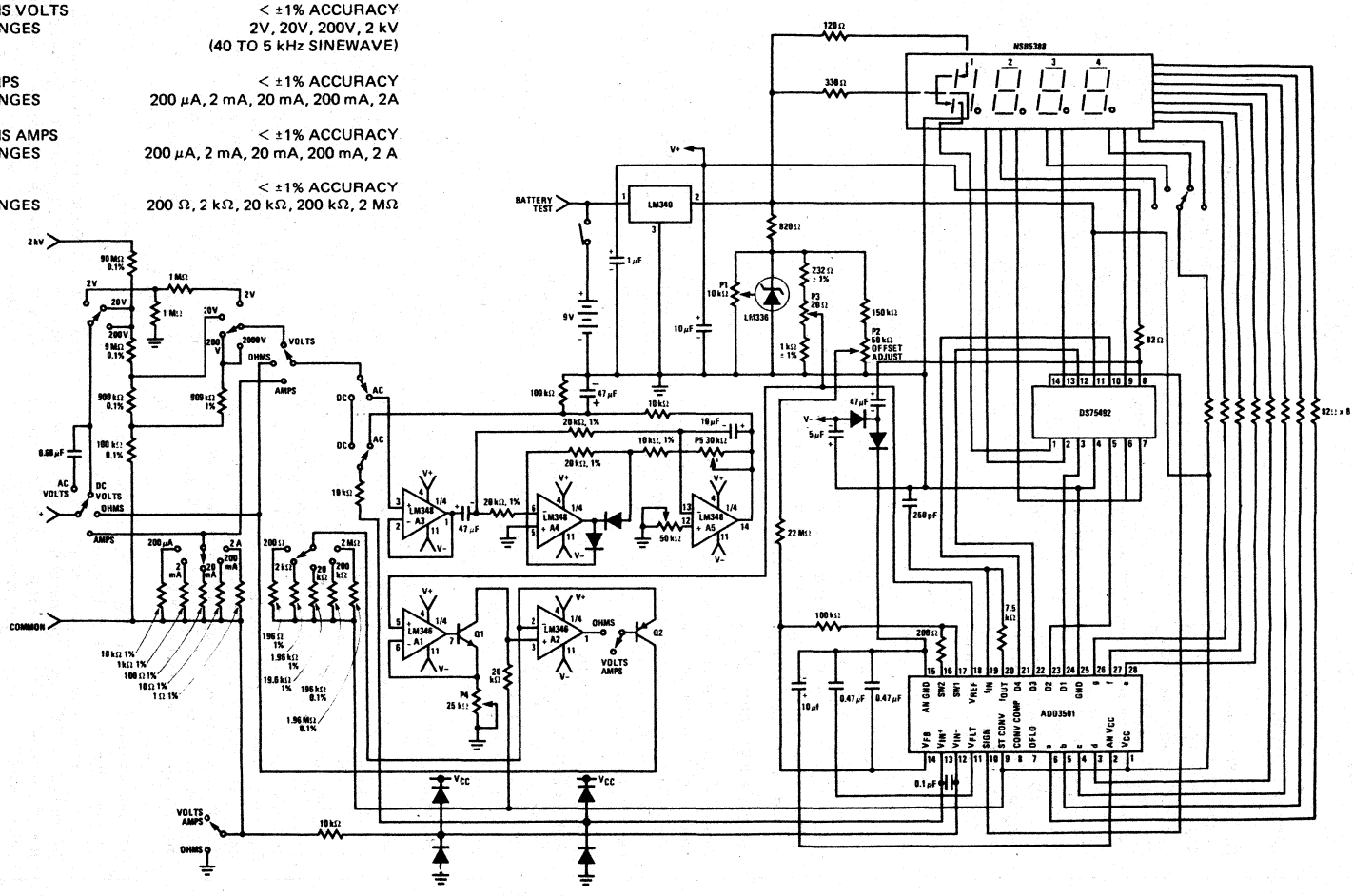


FIGURE 1. ADD3501 Low Cost Digital Multimeter

input.* The ADD3501 simply converts and displays the voltage drop developed across the DMM's current-sensing resistor.

AC Current Measurement. AC current measurements are made in a way similar to DC current measurements. The DMM is switched to its AMPS and AC settings. The in-circuit current is again measured by a drop across the DMM's current-sensing resistor, but now the AC voltage developed across this resistor is processed by A3, A4, and A5—exactly as described for AC voltage measurements—before being transferred to the ADD3501. Again, the DMM displays an rms value appropriate for the AC signal current being measured.

Resistance Measurement. This DMM measures resistance in the same way as do most multimeters: it measures the voltage drop developed across the unknown resistance by forcing a known, constant-current through it. Suitable scale calibration translates the voltage drop to a resistance value.

The resistance measurement requires the generation of a constant-current source that is independent of changes in V_{CC}, using the 2V, ground-referred reference voltage. The circuit of *Figure 3* accomplishes this.

In *Figure 3*, A1 establishes a constant-current sink by forcing node A to V_{REF}, the voltage level at A1's non-inverting input. With node A held constant at V_{REF} (2.000V), current through R2 is also fixed—since Q1's collector current is determined by the αI_E product—thus establishing V1 as

$$V1 = V_{CC} - \alpha(V_{REF}/R1)R2 \qquad (1)$$

Note that V_{REF} is derived from the LM336—a precision voltage source. Equation (1) shows, then, that (all else remaining constant) V1 varies directly with changes in V_{CC}; i.e., V1 tracks V_{CC}. The A1/Q1 pair thus establishes a voltage across R2 that floats, independent of changes in the ground-referenced potentials (V_{CC} and V_{REF}) that define it.

Now look at the A2/Q2 circuitry. The closed-loop operation of A2 tries to maintain a zero differential voltage between its input terminals. A2's non-inverting input is held at V1; thus, A2's inverting input is driven to V1. The current through R_L (Q2's emitter current) is therefore $(V_{CC} - V1)R_L$. Since V1 tracks V_{CC}, then $(V_{CC} - V1)$ — the voltage drop across R_L—is constant, thus producing I_{SOURCE} *(Figure 3)*—the constant source current needed for the resistance measurement.

Note, that varying R_X will not affect I_{SOURCE} so long as the voltage drop across R_X is less than $(V1 - V_{BE2})$. Should V_{RX} exceed $(V1 - V_{BE2})$, Q2 would saturate, invalidating the measurement. The ADD3501 eliminates this worry, however, because as soon as the drop across R_X equals or exceeds the 2V full-scale input voltage the ADD3501 will display an OFL condition.

Finally, SW1 *(Figure 3)* is required as part of the VOLTS/AMPS/OHMS mode selection circuitry; in the VOLTS/AMPS position it prevents Q2's base-emitter junction pulling the V− supply to ground through A2.

*This drop may be reduced to 200 mV; refer to the last section of this application note.

TABLE I. DMM PERFORMANCE

Measurement Mode	Range 0.2	2	20	200	2000	Frequency Response	Accuracy	Overrange Display
DC Volts	–	V	V	V	V	–	≤ 1% F.S.	± OFLO
AC Volts	–	V_{RMS}	V_{RMS}	V_{RMS}	V_{RMS}	40 Hz to 5 kHz	≤ 1% F.S.	+ OFLO
DC Amps	mA	mA	mA	mA	mA		≤ 1% F.S.	±OFLO
AC Amps	mA_{RMS}	mA_{RMS}	mA_{RMS}	mA_{RMS}	mA_{RMS}	40 Hz to 5 kHz	≤ 1% F.S.	+OFLO
Ohms	kΩ	kΩ	kΩ	kΩ	kΩ	–	≤ 1% F.S.	+OFLO

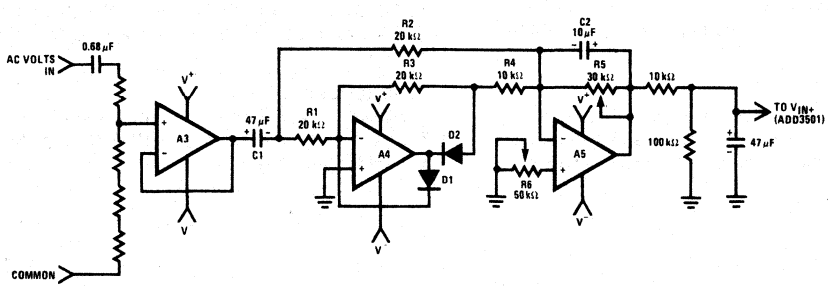


FIGURE 2. AC/DC Converter

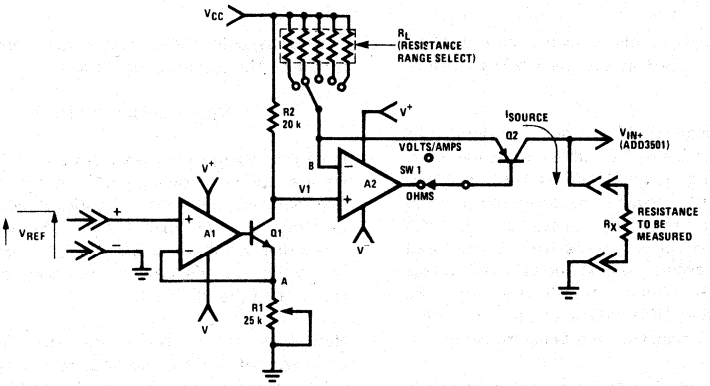


FIGURE 3. Constant-Current Source

CALIBRATION

Calibrate the DMM according to the following sequence of operations:

1. Adjust P1 until the cathode voltage of the reference diode, LM336, equals 2.49V. This reduces the diode's temperature coefficient to its minimum value.

DC Volts 2V Range
2. Short the (+) and (−) probe inputs of the ADD3501 and adjust P2 until the display reads 0000.

DC Volts 2V Range
3. Apply 1.995 volts across the (+) and (−) probe inputs and adjust P3 until the display reads 1.995.

Ohms 2 MΩ Range
4. Select a precision resistor with a value near full-scale or the 2 MΩ range, and adjust P4 until the appropriate value is displayed.

AC Volts 2V Range
5. Apply a known 1.995V_{rms} sinewave signal to the DMM and adjust P5 until the display reads the same.

PC BOARD LAYOUT

It is imperative to have only one, single-point, analog signal ground connection for the entire system. In a multi-ground layout, the presence of ground-loop resistances will cause the op amps' offset currents and AC response to have a devastating effect on system gain, linearity, and display LSD flicker. Similar precautions must also be taken in the layout of the analog and high-switching-current (digital) paths of the ADD3501.

A FINAL NOTE

The digital multimeter described in this note was developed with the goals of accuracy and low cost. For the high-end DMM market segments, however, improvements to the basic circuit of *Figure 1* are possible in the following areas:

1. Expand the VOLTS mode to include a 200 mV full-scale range;
2. Decrease the full-scale current-measurement loading voltage from 2V to 200 mV; and,
3. Provide a true-rms measurement capability.
4. Increase resolution by substituting the ADD3701—3 3/4-digit DVM chip—which is interchangeable and provides a maximum display count of 3.999.

The first 2 improvements involve a dividing down of the ADD3501 feedback loop by a ratio of 10:1, which reduces the 2V full-scale input requirement to 200 mV. This not only allows a 200 mV signal between the ADD3501's V_{IN+} and V_{IN-} inputs to display a full-scale reading, but implies that the maximum voltage dropped across the current-measuring-mode resistance also will be 200 mV. Note, though, that the values of the current-measurement resistors must be scaled down by a factor of ten.

Additionally, a 200 mV full-scale input implies a resolution of 100 μV/LSD. At such low input levels, the DMM may require some clever circuitry to eliminate the gain and linearity distortions that can arise from the offset currents in the AC-to-DC converter.

The third possible improvement—the reading of true-rms values—can be implemented by replacing the AC-to-DC converter of *Figure 2* with National's LH0091, a true-rms-to-DC converter, and appropriate interface circuitry.

REFERENCES:

1. ADD3501 Data Sheet.
2. LH0091 Data Sheet.
3. LM336 Data Sheet.
4. Application Note AN-20.
5. ADD3701 Data Sheet.

New Phase-Locked-Loops Have Advantages as Frequency to Voltage Converters (and more)

National Semiconductor
Application Note 210
Robert Pease
April 1979

A phase-locked-loop (PLL) is a servo system, or, in other words, a feedback loop that operates with frequencies and phases. PLL's are well known to be quite useful (powerful, in fact) in communications systems, where they can pluck tiny signals out of large noises. Here, however, we will discuss a new kind of PLL which cannot work with low-level signals immersed in noise, but has a new set of advantages, instead. It does require a clean noise-free input frequency such as a square wave or pulse train.

This PLL can operate over a wide frequency range, not just 1 or 2 octaves but over 1 or 2 or 3 decades. It naturally provides a voltage output which responds quickly to frequency changes, yet does not have any inherent ripple. Thus, it can be used as a frequency-to-voltage (F-to-V) converter which does not have any of the classical limitations or compromises of (large ripple) vs (slow response), which most F-to-V converters have.[1] The linearity of this F-to-V converter will be as good as the linearity of the V-to-F converter used, and this linearity can easily be better than 0.01%. Other advantages will be apparent as we study the circuit further.

The basic circuit shown in Figure 1 has all the functional blocks of a standard PLL. The frequency and phase detection do not consist of a quadrature detector, but of a standard dual-D flip-flop. When the frequency input is larger than F_2, Q1 will be forced high a majority of the time, and provide a positive error signal (via CR3, 4, 5, and 6) to the integrator.

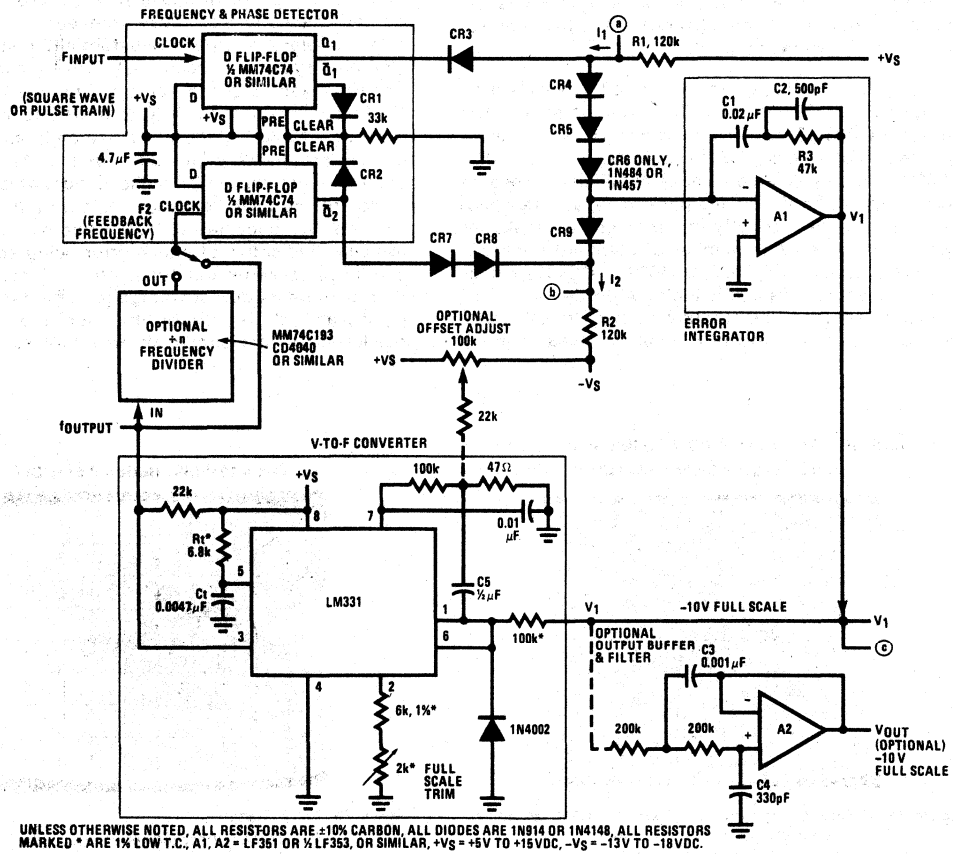


Figure 1. Basic Wide-Range Phase-Locked Loop

1. AN-207, V-to-F and F-to-V Converter Applications.

If F input and F_2 are the same, but the rising edges of F input lead the rising edges of F_2, the duty cycle of Q1 = HI will be proportional to the phase error. Thus, the error signal fed to the integrator will decrease to nearly zero, when the loop has achieved phase-lock, and the phase error between F_{IN} and F_2 is zero. Actually, in this condition, Q1 will put out 30 nanosecond positive pulses, at the same time that Q2 puts out 30 nanosecond negative pulses, and the net effect as seen by the integrator is zero net charge. The 30 nanosecond pulses at Q1 and Q2 enable both flip-flops to be CLEARED, and prepared for the next cycle. This phase-detector action is substantially the same as that of an MC4044 Phase-Detector, but the MM74C74 is cheaper and uses less power. It is fast enough for frequencies below 1 MHz. (At higher frequencies, a DM74S74 can be used similarly, with very low delays.)

The error integrator takes in the current from R1 or R2, as gated by the Q1 and $\overline{Q2}$ outputs of the flip-flop. For example, when F_{IN} is higher, and Q1 is HIGH, I_1 will flow through CR4, 5, and 6 and cause the integrator's output to go more negative. This is the direction to make the V-to-F converter run faster, and bring F_2 up to F input. Note that A1 does not merely integrate this current in C1 (a mistake which many amateur PLL designers make!). The resistor R3 in series with C1 makes a phase *lead* in the loop response, which is essential to loop stability. The small capacitor C2 across R3 is not essential, but has been observed to offer improved settling at the voltage output.

The output of the integrator, V1, is fed to a voltage-to-frequency (V-to-F) converter. The example shown here utilizes a LM331. This converter runs on a single supply, and responds quickly with nonlinearity better than 0.05% (even though an op-amp is not used nor needed). The output of the VFC is fed back to F_2, as a feedback frequency, either directly or through an (optional) frequency divider. Any number of standard frequency dividers such as MM74C193, CD4029, or CD4018, can be used, subject to reasonable limits. A divider of 2, 3, 10, or 16 is often used. The output voltage of the integrator will be proportional to the F input, as linearly as the V-to-F can make it. Thus, the integrator's output voltage V1 can be used as the output of an ultralinear F-to-V converter. However during the brief pulses when the flip-flop is CLEARing itself, there will be small glitches found on the output of A1. The RMS value of this noise may be very small, typically 0.5 to 5 mV, but the peak amplitude, sometimes 10 to 100 mV, can be annoying in some systems. And, no additional filtering can be added in the main loop's path, for any further delay in the route to the VFC would cause loop instability. Instead, the output may be obtained from a separate filter and buffer which operates on a branch path. A2 provides a simple 2-pole active filter (as discussed in Reference 1) which cuts the steady-state ripple and noise down below 1 mV peak-to-peak, an excellent level for such a quick F-to-V (as we shall see).

What is not obvious about A2 is that its output can settle (within a specified error-band such as ±10 millivolts from the final DC value) earlier and more quickly than A1's output. The waveforms in Figure 2 show F_{IN} stepping up instantly from 5 kHz to 10 kHz; it also shows F_2 stepping up very quickly. The error signal at Q1 is also shown. The critical waveforms are shown in Figure 3, the outputs of A1 and A2. While A1 puts out large spikes (caused by I1 flowing through R3), these large spikes cause the V-to-F converter to jump from 5 kHz to 10 kHz without any delay. There is, as shown in Figure 2, a significant phase error between F_{IN} and F_2, but an inspection of these frequencies shows that frequency lock has been substantially instantaneous. Not one cycle has been lost! The phase lock and settling takes longer to achieve. Still, we know that if the frequency out of the VFC is 10 kHz, its input voltage must be −10 VDC. If there is noise on it, all we have to do is filter it in A2. Figure 3 shows that A2 settles very quickly — actually, in 2.0 milliseconds, which is just 20 cycles of the new frequency. A2's output has settled (i.e., the frequency has settled), while A1's output error (which is indicative of phase error being servo'ed out) continues to settle out for another 12 ms. Thus, this filter permits its output voltage to settle faster than its input, and it is responsible for the remarkable quickness of this circuit as an F-to-V converter. The

Vertical sensitivity = 10 V/DIV (CMOS logic levels)
Horizontal sensitivity = 0.5 ms/DIV

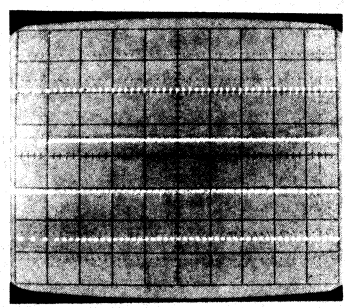


Figure 2a. F output steps up from 5 kHz to 10 kHz as quickly as the input, never missing a beat.
Top Trace = input "F_{IN}" to PLL.
Bottom Trace = output "F_{OUT}" from PLL.

Vert = 10 V/DIV, Horiz = 0.5 ms/DIV

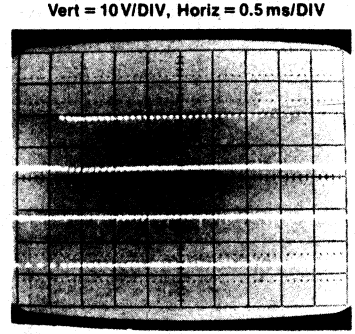


Figure 2b. Error Signal.
Top Trace = error signal at Q1.
Bottom Trace = output "F_{OUT}" from PLL.

waveforms of Figure 3 can be compared to the response (shown in Figure 4) of a conventional F-to-V converter. The upper trace is the output of a conventional FVC after a 4-pole filter[2] and the lower trace is the output of the circuit of Figure 1. The phase-locked-loop F-to-V converter is quicker yet quieter.

2. AN-207, V-to-F and F-to-V Converter Applications.

Vert = 2V/DIV, Horiz = 2ms/DIV

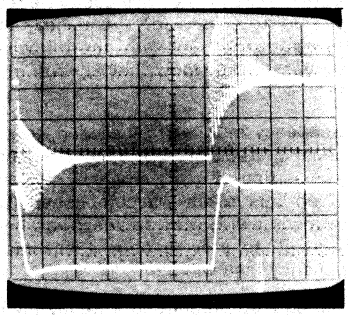


Figure 3a. Settling waveforms, as F_{IN} goes from 5kHz to 10kHz and back again, using circuit of Figure 1.
Top Trace = output of integrator (V1).
Bottom Trace = output of filter (V_{OUT}).

Vert = 2V/DIV, Horiz = 0.5ms/DIV

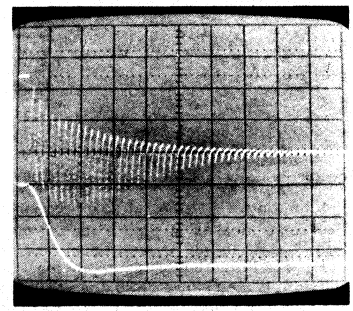


Figure 3b. PLL Settling Waveforms.
The same waveform as in Figure 3a, but time base is expanded to 0.5ms/DIV to show fine detail of settling.

Vert = 2V/DIV, Horiz = 20ms/DIV

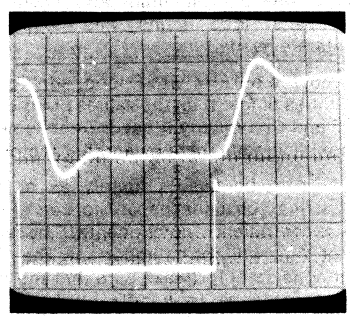


Figure 4a. FVC Response vs PLL Response.
The PLL can settle rather more quickly than a conventional F-to-V converter.
Top Trace = conventional F-to-V converter with 4-pole active filter, responding to a 5kHz to 10kHz step.
Bottom Trace = PLL FVC, with the same input, circuit of Figure 1.

Vert = 2V/DIV, Horiz = 20ms/DIV

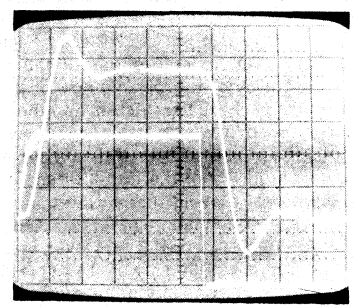


Figure 4b. FVC Step Response.
This waveform is similar to that in Figure 4a, but the frequency change covers a 10:1 ratio, from 10kHz to 1kHz and back to 10kHz. For this waveform, the adaptive current sources of Figure 5 connect to Figure 1 (whereas for Figure 4a R1 = R2 = 120k).

Vert = 2V/DIV, Horiz = 5ms/DIV

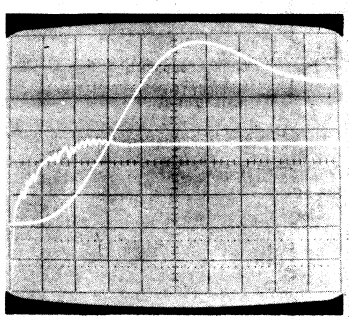


Figure 4c. FVC Response.
The same as Figure 4b, but time base expanded to 5ms/DIV, to show detail of rise time.
Top Trace = conventional FVC.
Bottom Trace = PLL FVC.

Vert = 2V/DIV, Horiz = 5ms/DIV

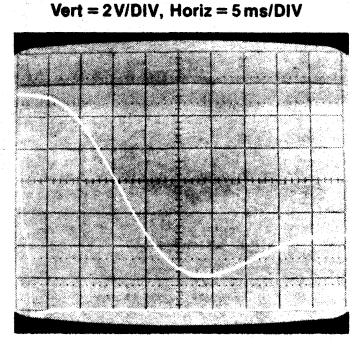


Figure 4d. FVC Response.
The same as Figure 4b, but expanded to 5ms/DIV to show details of fall time.
Top Trace = conventional FVC.
Bottom Trace = PLL FVC.

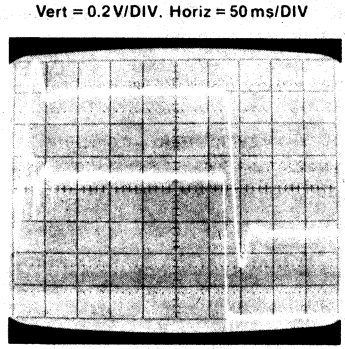


Figure 4e. PLL Settling Waveforms at Low Frequencies. The same idea as in Figure 4b, but 10× slower, from 1.0 kHz to 100 Hz (and back). The settling to 1 kHz is still distinctly faster for the PLL, but at 100 Hz, it is a bit slower. Still, the PLL is faster than the FVC at all speeds from 200 Hz to 10 kHz.

So far we have shown a PLL which operates nicely over a frequency range of about 3:1. If the frequency is decreased below 3 kHz, the loop gain becomes excessive, and the currents I1 and I2 are large enough to cause loop instability. The loop gain increases at lower frequencies, because a given initial phase error will cause the fixed current from R1 or R2 to be integrated for a *longer* time, causing a *larger* output change at the integrator's output, and a *larger* change of frequency. When the frequency is thus corrected, and the period of one cycle is changed, at a low frequency it may be *over-corrected,* and the phase error on the next cycle may be as large as (or larger than) the initial phase error, but with reversed sign.[3] To avoid this and to maintain loop stability at lower frequencies, e.g. 0.5 to 1 kHz, R1 and R2 can be simply raised to 1.5 MΩ. However, response to a step will be proportionally slower. To achieve a wide frequency range (20:1), and optimum quickness at all frequencies, it is necessary to servo I1 and I2 to be *proportional to the frequency.* Fortunately, as V1 is normally proportional to F, it is easy to generate current sources I1′ and I2′ which are proportional to F. The circuit of Figure 5 can be connected to the basic PLL, instead of R1 and R2, and provides good, quick loop stability over a 30:1 frequency range, from 330 Hz to 10 kHz. For best results over a 30:1 frequency range, change R3, the damping resistor in Figure 1, from 47k to 100k. However, if the frequency range is smaller (such as 2:1 or 3:1), constant resistors for R1 and R2 or very simple current sources may give adequate response in many systems. (To cover wider frequency ranges than 30:1 with optimum response, the circuits in the precision phase-locked-loop, below, are much more suitable.)

Often a frequency multiplier is needed, to provide an output frequency 2 or 3 or 10 or n times higher than the input. By inserting a ÷n frequency divider in the feedback loop, this is easily accomplished. [Of course, a ÷m frequency divider can be inserted ahead of the frequency input, to provide correct scaling, and the output frequency then will be $F_{IN}(n/m)$.]

To obtain good loop stability in a frequency multiplier with n = 2, remember that a 20 kHz V-to-F converter followed by a ÷2 circuit has exactly the same loop response and stability needs as a 10 kHz V-to-F converter, because it *is* a 10 kHz V-to-F converter, even though it provides a useful 20 kHz output. Thus, the frequency of the F_2 (minimum and maximum) will determine what loop gains and loop damping components are needed.

To accommodate a 1 kHz V-to-F loop, simply make C1 and C2 10 times bigger than the values of Figure 1; treat C3, C4, C5 and Ct similarly if used. To accommodate a 100 Hz V-to-F, increase them by another factor of 10.

If the PLL is to be used primarily as a frequency multiplier, it may be unnecessary to use stable, low-temperature-coefficient components, because the accuracy of V_{OUT} will not be important. The parts cost can be cut considerably. (Make sure that the VFC does not run out of range to handle all frequencies of interest.) On the other hand, the damping components will be chosen quite a bit differently if slow, stable jitter-free response is needed or if quick response is required. The circuits shown are just a starting place, to start optimizing your own circuit.

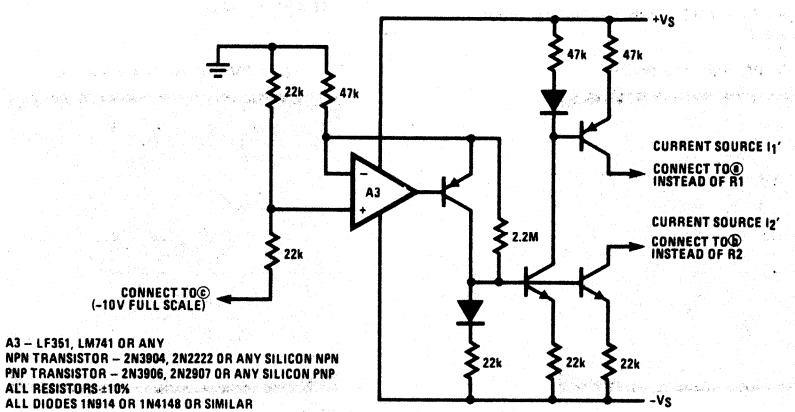


Figure 5. Proportional Current Source for Basic PLL

3. Optimize phase-lock loops to meet your needs or determine why you can't. Andrzej B. Przedpelski, *Electronic Design,* September 13, 1978.

A Single-Supply PLL

The single-supply PLL is shown in Figure 6 as an example of a simple circuit which is effective when battery operation or single-supply operation is necessary. This circuit will function accurately over a 10:1 frequency range from 1 kHz to 10 kHz, but will not respond as quickly as the basic PLL of Figure 1. The reason is the use of the CD4046 frequency detector. When an F_{IN} edge occurs ahead of a F feedback pulse, pin 13 of the CD4046 pulls up on C1 via R1 = 1 kΩ. This current cannot be controlled or manipulated over as wide a range as "I1" in Figure 1. As a consequence, the response of this PLL is never as smooth nor fast-settling as the basic PLL, but it is still better behaved than most F-to-V converters. As with the basic PLL, the detector feeds a current to be integrated in C1 (and R2 provides the necessary "lead"). A1 acts simply as a buffer for the R1, C1 integrator. A3, optional, can provide a nicely filtered output. And A2 servos Q1, drawing a current out of C6 which is proportional to V2. Here the LM331 acts as a current-to-frequency converter, and F output is precisely proportional to the collector current of Q1. As with the basic circuit, this PLL can be used as a quick and/or quiet F-to-V converter, or as a frequency multiplier. One of the most important uses of an F-to-V is to demodulate the frequency of a V-to-F converter, which may be situated at a high common-mode voltage, isolated by photo-isolators, or to recover a telemetered signal. An F-to-V converter of this sort can provide good bandwidth for demodulating such a signal.

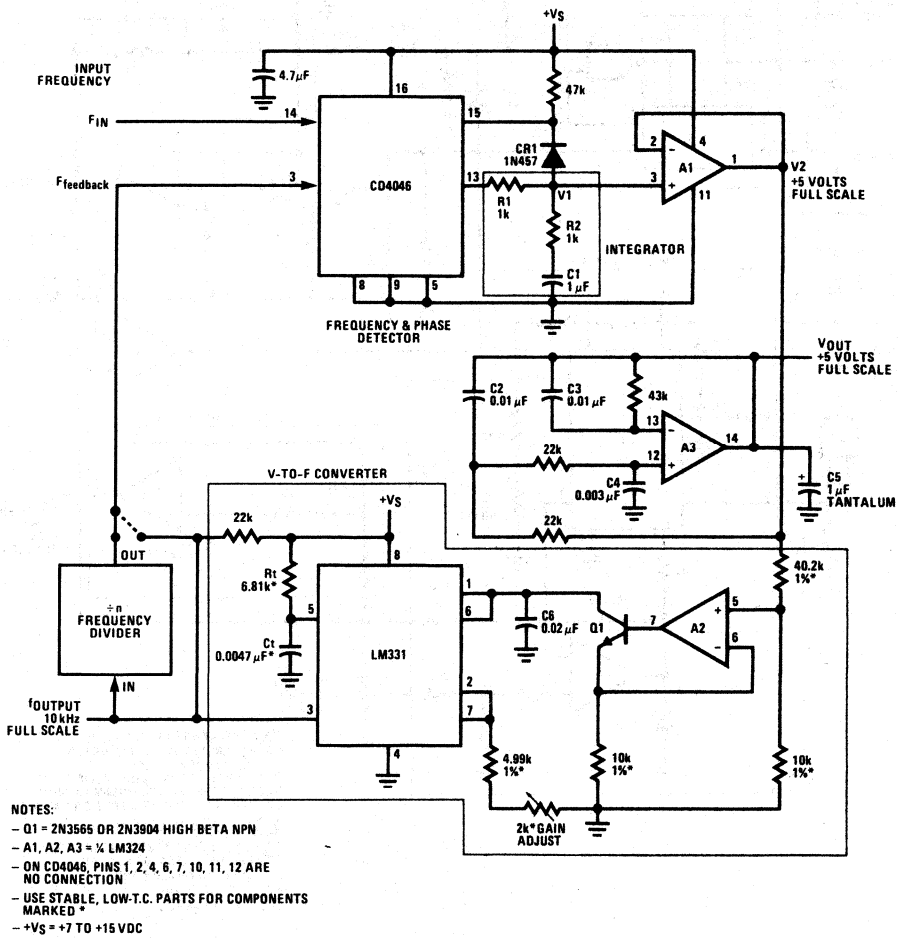


Figure 6. Single Supply Phase Locked Loop

The precision PLL in Figure 7 acts very much the same as the basic PLL, with refinements in various places.

- The flip-flops in the detector have a gate G1 to CLEAR them, for quicker response.
- The currents which A1 integrates are steered through Q1, Q2 and Q3, Q4 because transistors are quicker than diodes, yet have much lower leakage.
- The V-to-F converter uses A2 as an op-amp integrator, to get better than 0.01% nonlinearity (max).
- G2 is recommended as an inverter, to invert the signal on the LM331's pin 3, avoid a delay, and improve loop stability. (However, we never found any *real* improvement in loop stability, despite theories that insist it must be there. Comments are invited.)

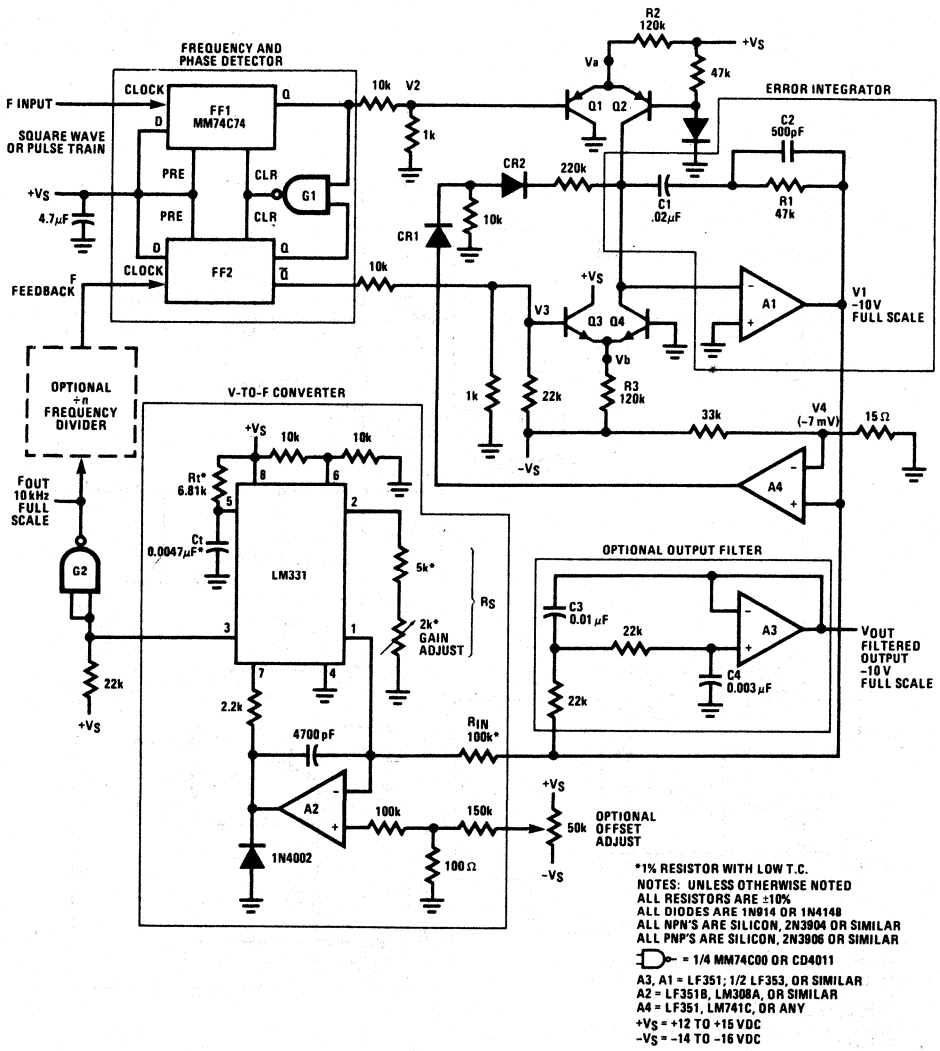


Figure 7. Precision PLL

- A4 is included as an (optional) limiter, to prevent V1 from ever going positive. This will facilitate quick startup and recovery from overdrive conditions.

Also, in Figure 8, the wide-range current pump for the precision PLL is a "semiprecision" circuit, and provides an output current proportional to −V1, give or take 10 or 15%, over a 3-decade range. The 22MΩ resistors prevent the current from shutting off in case −V becomes positive (probably unnecessary if A4 is used). For best results over a full 3-decade range (11kHz to 9Hz), do use A4, delete the four 22MΩ resistors, and insert the (diode parallel to the 470kΩ) in series with the R_G as shown. This will give good stability at all frequencies (although stability cannot be extended below 1/1500 of full scale without extra efforts).

This PLL has been widely used in testing of VFCs, as it can force the LM331 to run at a crystal-controlled frequency (established as the F input), and the output voltage at V_{OUT} is promptly measured by a 6-digit (1ppm nonlinearity, max) digital voltmeter, with much greater speed and precision than can be obtained by forcing a voltage and trying to read a frequency. While at 10kHz, the advantages are clearcut; at 50Hz it is even more obvious. Measuring a 50Hz signal with ±0.01Hz resolution cannot be done (even with the most powerful computing counter-timer) as accurately, quickly, and conveniently as the PLL's voltage output settles.

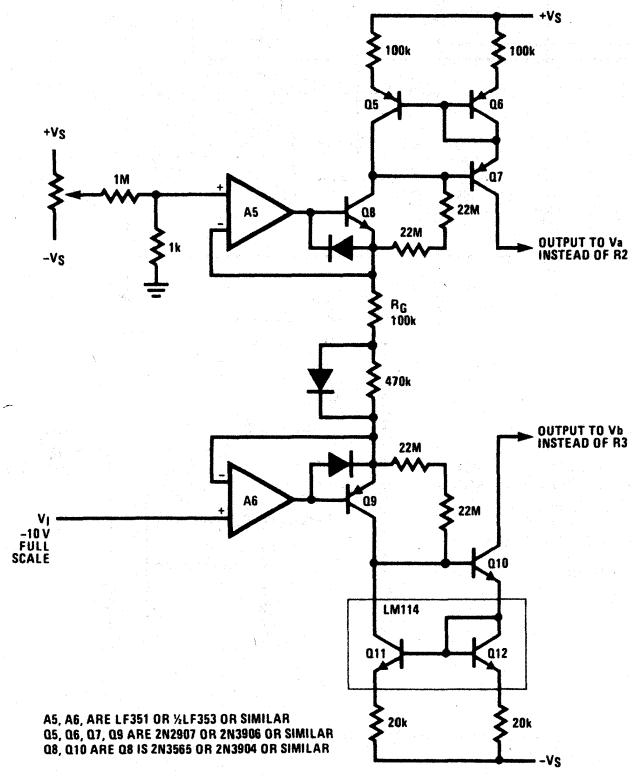


Figure 8. Wide Range Current Pumps for Precision PLL of Figure 7

One final application of this PLL is as a wide-range sine generator. The VFC in Figure 9 puts out an adequate sine-shaped output, but does not have good V-to-F linearity, and its frequency stability is not much better than 0.2%. An LM331 makes an excellent linear stable V-to-F converter, with a pulse output; but it can not make sines. But it can command, via a PLL, to force the sine VFC to run at the correct frequency. Simply connect the sine VFC of Figure 9 into one of the PLLs, instead of the LM331 VFC circuit. Then use a precise linear low-drift VFC based on the LM331 to establish the F_{IN} to the PLL. If the voltage needed by the sine VFC to put out a given frequency drifts a little, that is okay, as the integrator will servo and make up the error. The use of a controlled sine-wave generator in a test system was the first of many applications for a wide-range phase-locked-loop.

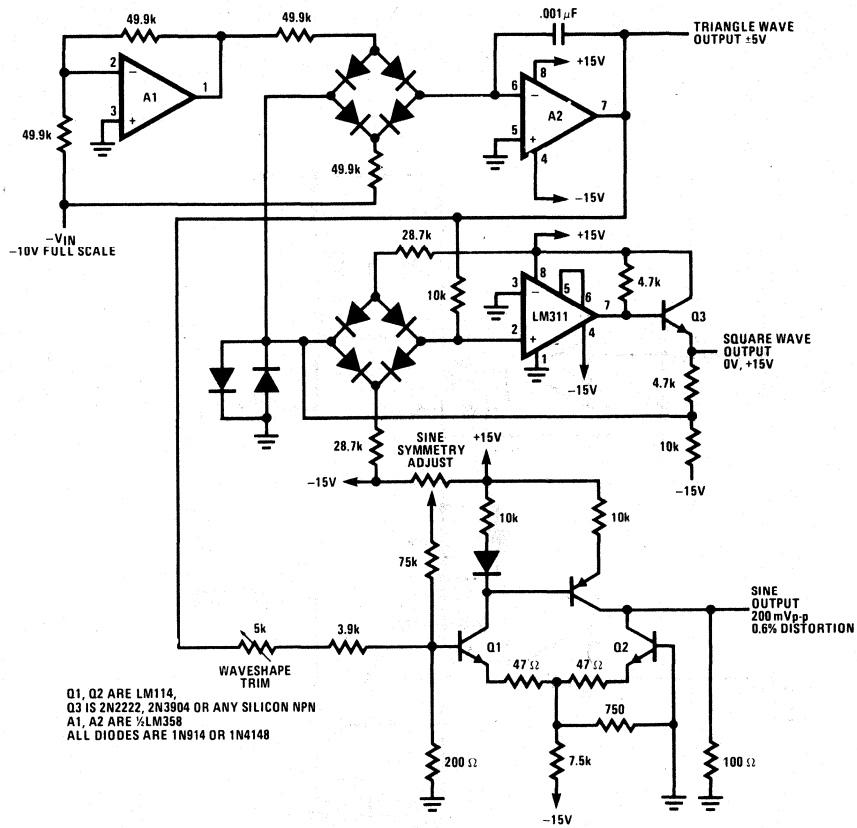


Figure 9. Sine-Wave VFC to Use with PLL

A Pressure Microcontroller: Pressure Controlled by Microprocessor with Digitally Interfaced Pressure Transducer and Solenoid Valves

National Semiconductor
Application Note 218
Duane Tandeske
February 1979

SUMMARY

A board-level circuit is presented that monitors and delivers programmed pressures. Features include autoreferencing, 8-bit accuracy, and user programmed software. The key components are National Semiconductor's monolithic pressure transducer, single chip data acquisition system, SC/MP microprocessor, and NIBL MAXI-ROM®. Simple variations and additions of hardware and software offer application flexibility so as to accommodate a broad spectrum of robotic measurement and control.

PRESSURE CONTROLLED SYSTEMS

In all hydraulic or pneumatic measurement and control applications, one or more values of pressure need to be delivered to 1 or more pressure actuated machines from 1 or more pressure sources. The job of the pressure controller is to measure and control the values, sequence, and timing of pressure delivery. The simplest such system is shown in *Figure 1.*

PRESSURE ACTUATED MACHINES

Typical pressure actuated machines resemble a piston-cylinder mechanism in principle. As shown in *Figure 2,* though found in various states and degrees of camouflage, there are usually 2 pressure chambers, 1 on either side of the piston.

The pressure difference between the 2 chambers determines the direction and magnitude of force that the piston exerts against a spring. If the spring is part of the machine, then the job of the machine is usually to position a tool attached to the piston relative to some work object. If the spring is part of the work object, then the job of the machine is usually to create a force between the tool and the work object.

PRESSURE SOURCES

Primary pressure sources include the ocean, the atmosphere, compressors, and pumps. Generally, the primary pressure source is chosen so as to be capable of delivering higher pressure values than those required by the pressure actuated machine. Most commonly, a pressure controlled system incorporates a pressure vessel as a secondary pressure source to the machine. As shown in *Figure 3,* one job of a pressure controller may be to regulate the value of pressure delivered from the primary source to the pressure vessel. In simple systems, one of the chambers of the pressure actuated machine can also serve as the pressure vessel.

FIGURE 1. Pressure Controlled System

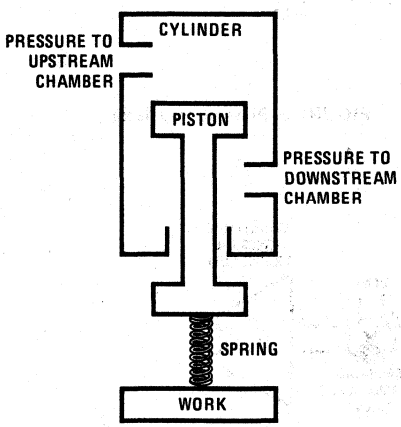


FIGURE 2. Pressure Actuated Machine

FIGURE 3. Regulated Pressure Source

PRESSURE MICROCONTROLLER

The primary job of the pressure microcontroller as indicated in *Figure 1* is to control the sequence, timing, and value of pressure delivered from the pressure source to the pressure actuated machine. As shown in *Figure 2,* this involves controlling the pressure difference between the upstream and downstream chambers of a piston-cylinder mechanism. Also, as shown in *Figure 3,* the control function may involve regulating the pressure delivered from the primary source to a pressure vessel, which vessel may in fact be a chamber of the machine. To accomplish these ends, the pressure microcontroller includes control plumbing, a pressure transducer, and control electronics. *Figure 4* shows a pressure transducer based pressure microcontroller.

PRESSURE REGULATION

A secondary job that can be performed by the pressure microcontroller of *Figure 4* is to serve as the pressure regulator of *Figure 3.* In this function, the pressure to be delivered to the pressure actuated machine is that of the pressure vessel. This pressure is measured by the pressure transducer. The microcontroller decides whether to increase or decrease the pressure of the pressure vessel. To increase the pressure, the 2-way solenoid valve (S3) is energized by the microcontroller such that pressure is delivered from the primary source to the pressure vessel. To decrease the pressure, the 2-way solenoid valve (S4) is energized such that the pressure vessel is bled to atmosphere. *Figure 5* is a schematic of this kind of pressure regulator. To simplify this subject matter, the hardware and software of the pressure regulation will be left to a future publication. For this article, the pressure source is assumed to be a regulated source.

BASIC CONTROL PLUMBING

Figure 6 shows the basic valve control plumbing necessary to deliver pressure from the regulated source to a pressure actuated machine as programmed. The regulated pressure source of *Figure 6* need be such that the desired delivery pressure be within the regulation range. For example, the pressure source may be regulated by the method shown in *Figure 5,* such that its pressure cycles between 20 psig and 30 psig. Further, suppose the desired delivery pressure is 25 ±1 psig. Then, it is the job of the control plumbing to deliver pressure whenever the regulated pressure source is at the desired delivery pressure.

Unenergized, the 3-way solenoid valve for measurement (S1) shorts pressure points 2 and 3. This is the auto-referencing condition, wherein the transducer reads atmospheric pressure regardless of the pressure at point 1. When energized, S1 shorts pressure points 1 and 2. This is the source measurement condition

Unenergized, the 2-way solenoid valve for pressure delivery (S2) blocks the path from pressure point 1 to point 4. When the measured pressure is between 24 psig and 26 psig, S2 is energized and shorts pressure points 1 and 4.

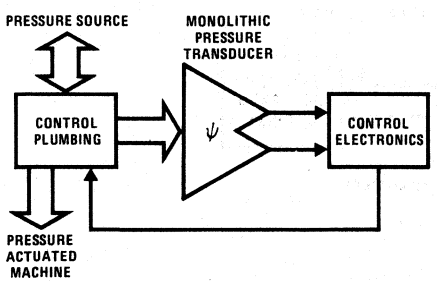


FIGURE 4. Pressure Microcontroller

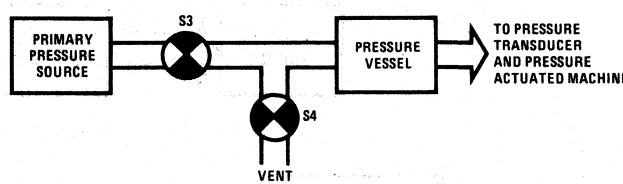


FIGURE 5. Pressure Regulator

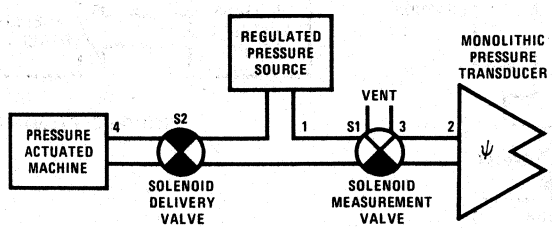


FIGURE 6. Basic Control Plumbing

TRANSDUCER AND CONTROL ELECTRONICS

The pressure transducer and control electronics of the pressure microcontroller comprise 4 printed circuit cards. The first card, or pressure control card, includes the pressure transducer, signal conditioning, analog to digital conversion, sample and hold, decode logic, and valve driving. The circuitry of the pressure control card is described in detail within this publication. The other 3 cards are the SC/MP CPU microprocessor card, the NIBL ROM program language card, and a 2k x 8-bit RAM memory card. These cards are the subject of other National Semiconductor publications and will not be described in detail within this publication. For those interested in developing more complex pressure control systems, it should be noted that the SC/MP, NIBL, and RAM card set can control several pressure control cards.

Figure 7 is a schematic of the transducer and control electronics portion of a pressure microcontroller, indicating the 4 card functions.

PRESSURE CONTROL CARD

The functions included within the pressure control card are pressure transduction, transducer signal conditioning, analog to digital conversion (A/D), sample and hold (S/H) address decode logic, and valve driving. *Figure 8* is a schematic of the circuit functions comprising the pressure control card. A prototype pressure control card is shown in photo on page 8. The total circuit of the pressure control card is shown in *Figure 9*.

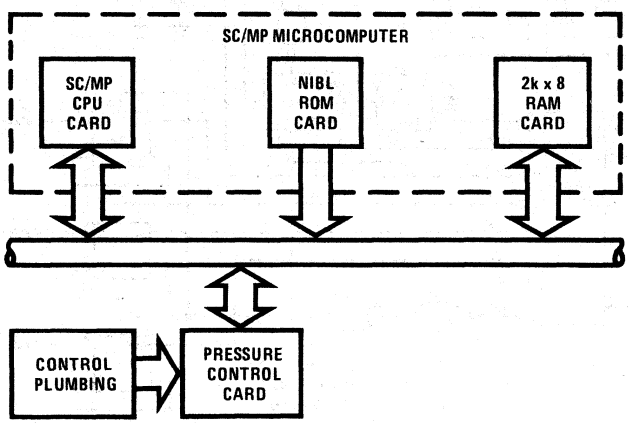


FIGURE 7. Transducer and Control Electronics

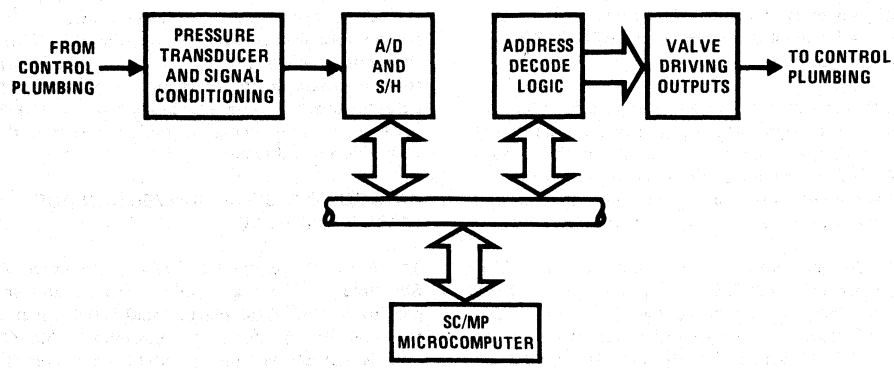


FIGURE 8. Pressure Control Card Functions

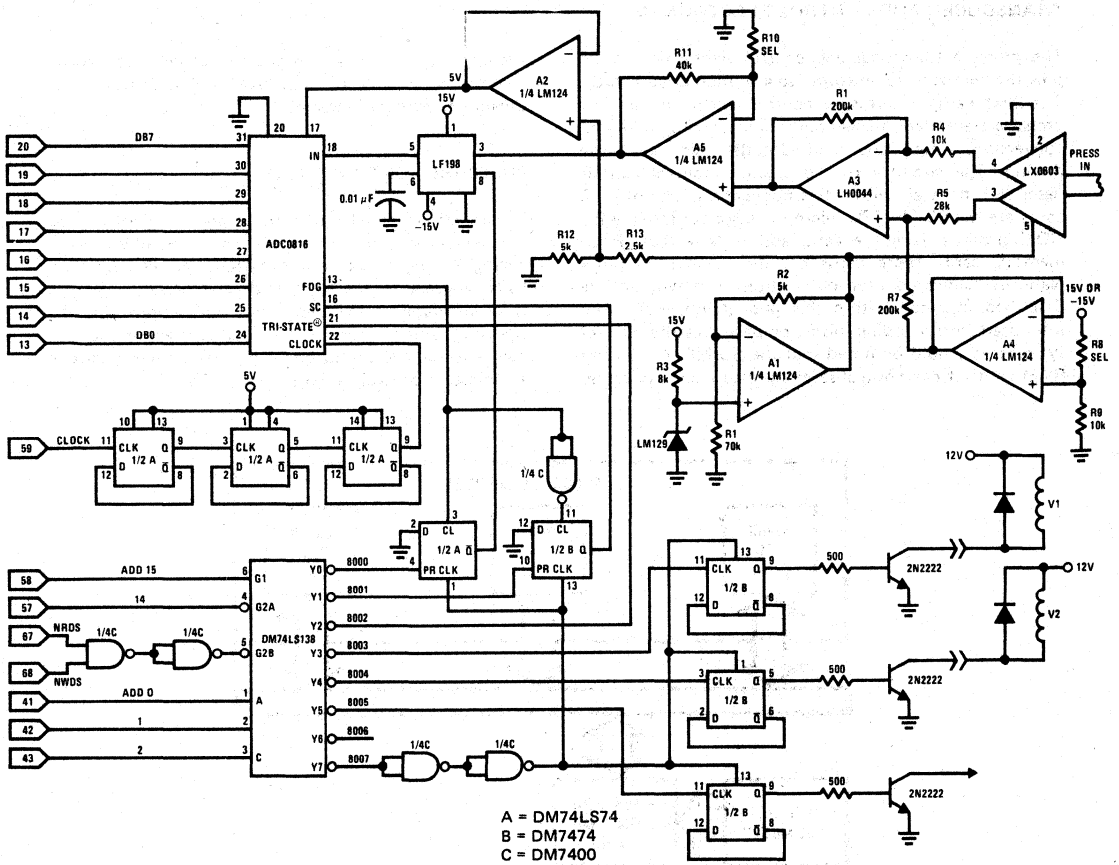


FIGURE 9. Pressure Control Card Circuit

PRESSURE TRANSDUCER AND SIGNAL CONDITIONING

The upper right quadrant of *Figure 9* shows the pressure transducer and signal conditioning portion of the pressure control card circuit. The pressure transducer selected is a National Semiconductor LX0603GB monolithic gage transducer.

The transducer circuitry has been designed for a 0.5V to 4.5V span corresponding to a 0 psig to 30 psig pressure range. The 4V span is directly compatible with the input of an ADC0816 analog to digital converter (A/D) and allows for correction of common-mode errors associated with time and temperature of as much as ±0.5V.

The LM129 and amplifier A1 make a stable 7.5V reference for the LX0603GB. Amplifier A3 is a fixed gain of 10 stage which converts the differential output of the LX0603GB to a single ended output for driving amplifier A5. Resistors R4 through R7 should be matched to within 1% to optimize common-mode rejection. Amplifier A5 is the gain stage used to adjust sensitivity. R10 is selected to achieve a 4V output change corresponding to a 30 psig change in pressure. Divider R8/R9 and amplifier A4 make up the offset adjust circuit. If the offset is negative, resistor R8 is selected and connected to +15V to set the output of amplifier A5 to +0.5V at 0 psig. If the offset is positive, resistor R8 is connected to −15V for the same adjustment. It should be noted that transducer sensitivity has been temperature compensated within the LX0603GB. Further, note that no special circuitry need be incorporated to compensate errors in transducer offset due to temperature changes (one source of common-mode error) because autoreferencing is employed within the basic plumbing and software.

ANALOG-TO-DIGITAL CONVERSION AND SAMPLE AND HOLD

The upper left quadrant of *Figure 9* shows the A/D and S/H circuitry. The signal conditioned transducer output goes to an LF198 sample and hold (S/H) which supplies the input to the A/D. The multiplexer (MUX) in the A/D is not shown, but could be connected between several transducer outputs and the S/H to allow conversion of multiple inputs. The +5V reference for the A/D is supplied by amplifier A2. The 4 MHz SC/MP system clock is divided by 8 via 3 cascaded "D" flip-flops (DM74LS74) to serve as the clock input for the A/D. The output of the A/D is an octal TRI-STATE® latch, making it compatible with the microprocessor.

ADDRESS DECODE LOGIC

The lower left quadrant of *Figure 9* shows the address decode logic circuit. Since the SC/MP microprocessor treats any interfaced device as a memory location, the designer is obliged to do likewise. Benefits to the user are the capabilities to cause actions as a direct result of the address decode (data are irrelevant).

A useful tool is an illustration depicting memory that is used (i.e., a memory map). This map provides the designer with an overall picture of the memory locations occupied by RAM, ROM and addressable operating hardware.

In this case, the hardware consists of A/D *start* and *enable output control*, S/H, and valve drivers. The sequence of events in this system is *holding* the S/H, *starting* the A/D, *enabling* A/D output and *turning* valves ON or OFF. *Figure 10* illustrates the memory map of this system.

Addressing is achieved by hardware decoding of the address bits (up to 16), using a DM74LS138. The decoder is activated when address bit 15 is 'Hi' and bit 14 is 'Lo' and a read or write strobe is present. The address decode of location 8007 causes the *init* or set command. In similar fashion, decoding 8007 sets the S/H to sample state, sets *start convert* low, and de-energizes the valves. The decode of 8000 sets the S/H to *hold* state. Decoding 8001 triggers *start convert* to the A/D. The *end of convert* signal from the A/D resets the S/H and *start convert* flip-flops. Decoding 8002 enables the TRI-STATE outputs of the A/D on the SC/MP data bus. Decoding 8003, 8004 or 8005 produces a pulse that toggles the valve driver latches. These latches are set up as toggle flip-flops so that they change state each time they are addressed. For multiple inputs, the decode of 8006 could be used to control the 16-channel input multiplexer on the ADC0816. To use the multiplexer, the pins should be connected as shown in *Figure 11*. To address channels 1 through 16, write 0 through 15 via the data bus to location 8006.

Note that the NIBL interpreter must occupy address space 0000 0FFF (hexadecimal). Support RAM for NIBL must start at 1000 and as a minimum, continue through location 111D. Also, when using address decode with the SC/MP CPU card, insure that a logic "0" is presented to pin 65 (MEMSEL) whenever user memory devices are accessed. Alternatively, pin 65 can be hard grounded.

VALVE DRIVING

The valve drivers are set up to drive $12V_{DC}$ valves. Clippard EV or EVO series or Linear Dynamics series 11 valves were used in breadboarding the system. A separate 12V supply should be used for the valves to avoid inductive spikes on the power supplies. Address memory locations 8003 through 8005 *toggle* the 3 valves.

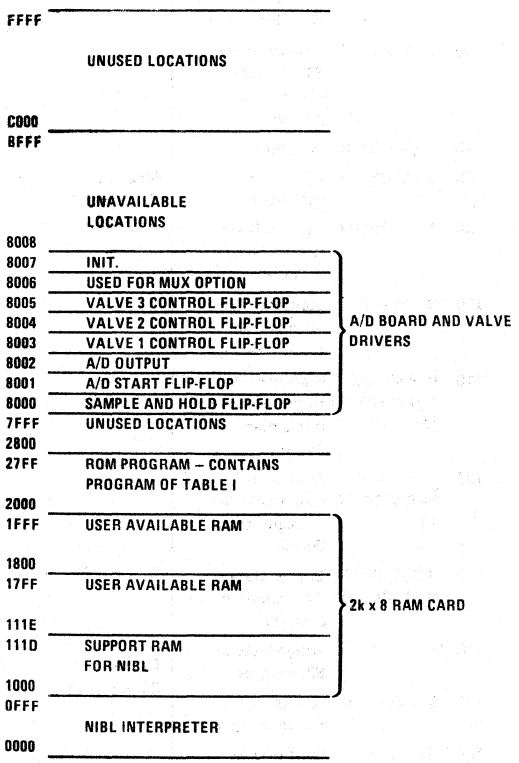


FIGURE 10. Memory Map

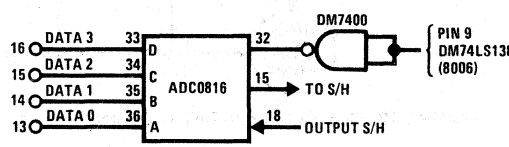


FIGURE 11. MUX Connection Diagram

SOFTWARE

The NIBL ROM card allows the use of high level language (Tiny Basic) for programming of the pressure microcontroller. It is best to demonstrate software by treating a typical control problem. As was discussed in the treatment of control plumbing *(Figure 6)*, let us assume the pressure source is preregulated by some means (perhaps by the method indicated in *Figure 5*) such that the source pressure periodically varies between 20 psig and 30 psig. Further, suppose it is desired to deliver pressure to (or actuate) the machine whenever the source pressure is between 24 psig and 26 psig. From the viewpoint of the machine, this is the equivalent of further regulating the source at 25 ±1 psig.

Figure 12 is the flow diagram and Table I shows the NIBL program to regulate pressure delivered to the machine at 25 psig. Instructions 10 through 50 initialize and autoreference. Instructions 60 through 100 measure pressure. Instructions 110 and 120 compare measured pressure with desired pressure. Instructions 130 through 160 deliver desired pressure continuously, if available, and provide continuous measurement.

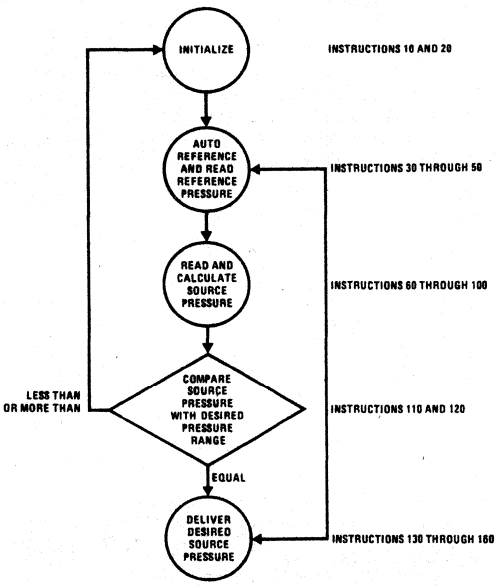


FIGURE 12. Flow Diagram to Deliver Desired Pressure

The comparison numbers in instructions 110 and 120 need explanation. NIBL requires that data be entered in binary numbers, or in number of least significant bits (LSB). As was indicated in the discussion of the pressure transducer (LX0603GB) and signal conditioning, the output voltage span (N) for an input pressure (P) of 30 psig is 4V. Equation (1) gives the sensitivities of the signal conditioned pressure transducer in mV per psi.

$$S = \frac{N}{P} = \frac{4V}{30\ psi} = 133\ mV/psi \qquad (1)$$

The 8-bit A/D can convert a maximum of 5V with 1-bit resolution. Equation (2) gives the binary resolution (R) of the A/D.

$$R = \frac{5V}{256} = 19.5\ mV/LSB \qquad (2)$$

Therefore, the binary limits of instructions 110 and 120 are given by Equations (3) and (4).

$$\text{Binary 24 psig} = \frac{133\ mV/psi}{19.5\ mV/LSB} \times 24\ psi = 166 \qquad (3)$$

$$\text{Binary 26 psig} = \frac{133\ mV/psi}{19.5\ mV/LSB} \times 26\ psi = 179 \qquad (4)$$

TABLE I. NIBL PROGRAM TO DELIVER 25 PSI

10	@ #8007 = 0	Initialize valves, *de-energize;* Initialize S/H, *sample;* Initialize A/D, *ready.*	Initialize and Autoreference
20	B = 0	Assign state of S2, *de-energize;*	
30	@ #8000 = 0	S/H, *hold.*	
40	@ #8001 = 0	A/D, *start conversion.*	
50	Z = @ #8002	Read A/D and store atmospheric (REF) pressure.	
60	@ #8003 = 0	Change state of S1, *energize;* read source pressure.	Measure Source Pressure
70	@ #8000 = 0	S/H, *hold.*	
80	@ #8001 = 0	A/D, *start conversion.*	
90	A = @ #8002	Read A/D and store source pressure.	
100	N = A – Z	Subtract REF reading from source reading.	
110	If N < 166 THEN GO TO 10	Start over if source pressure is less than 24 psi.	Compare
120	If N > 179 THEN GO TO 10	Start over if source pressure is greater than 26 psi.	
130	If B=0 THEN @ #8004 = 0	Change state of S2 if required, *energize.*	Deliver 25 psi
140	B=1	Assign state of S2, *energize.*	
150	@ #8003 = 0	Change state of S1, *de-energize.*	
160	GO TO 30	Start over at autoreferencing.	

ADDITIONAL SOFTWARE

Starting with the basic pressure microcontroller, a sophisticated measurement system can be constructed by the simple addition of software. As an example, consider the requirements of a microcontroller system designed to test the characteristics of other pressure transducers. That is, one wherein several transducers in a manifold need to be pressurized, data taken and stored, and parameters subsequently calculated. A program can be developed such that several different pre-selected pressures are sequentially supplied to the manifold. This is, of course, exactly the process shown in *Figure 12,* where the pressure actuated machine is replaced by a test manifold. The additional MUX capability of the A/D can be used to scan the transducers on test at each pressure and store their readings. Arithmetic routines in the characterization program allow comparison of each transducer's output with a programmed reference pressure characteristic. The calculated deviations can be used to display pass/fail decisions.

Such transducer test systems are in construction at National Semiconductor for internal use. A future publication will give detailed hardware and software description.

ADDITIONAL HARDWARE

The basic pressure microcontroller can be extended in function to provide feedback for robotic control. In fact, a sophisticated robot can be created with the addition of some software and hardware to the pressure microcontroller. The keyword is "feedback" for that is what distinguishes a robot from the aforedescribed microcontroller. The major function described thus far has been to select a desired pressure as it became available from a pressure source and ccuse that pressure to be delivered to the machine. A variation on this theme was described in less detail wherein pressure was regulated by the pressure microcontroller, then selected and delivered to the machine. But, in neither case was the pressure at the machine measured. Nor was the pressure microcontroller used in the control of pressure actuated machine functions.

If, in addition to the pressure source, the machine pressure or pressures were measured, and if those measurements were used in the actuation and control of the machine, then a true robot would be created. In concept, notice that the robotic system of *Figure 13* differs from the pressure controlled system of *Figure 1* by the mere addition of 1 arrowhead representing feedback from the machine.

FIGURE 13. Pressure Controlled Robot

Once again, it is best to treat a specific application as an example of robotic control. As was indicated in the discussion of pressure actuated machines, a piston-cylinder mechanism can be used to exert a force between a tool and a work object. Consider the case wherein the tool is a welding electrode attached to the piston and the work is the body of an automobile to be projection welded. The addition of one 3-way solenoid valve to the piston-cylinder mechanism of *Figure 2* allows the pressure microcontroller to vent the lower chamber of the cylinder when the delivered pressure represents the electrode force. When the lower chamber is vented, the upper chamber loads the electrode against the work object. *Figure 14* is one station of such a welding machine.

It should be noted that the pressure control card provides a third output stage which can be used to control the extra value of *Figure 14.* As indicated in the discussion of control electronics, 1 set of microprocessor (SC/MP), memory (RAM), and program language (NIBL) boards can control many pressure control boards. Thus, regulation of the pressure source and operation of many welding stations only requires additional pressure control boards, logic, valves, and software to expand the basic pressure microcontroller into a larger, more complex system. Considerable imagination is encouraged in treat-

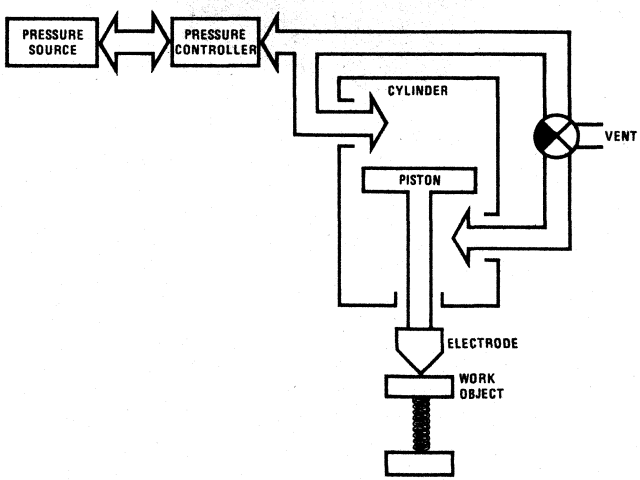


FIGURE 14. Robot Welding Station

ing this application since, in reality, a total welding machine of this kind may occupy a sizeable building that ingests steel and spits out car bodies. More detailed treatment of this system and other applications where the basic pressure microcontroller serves as the heart of sophisticated robots will be given in future publications.

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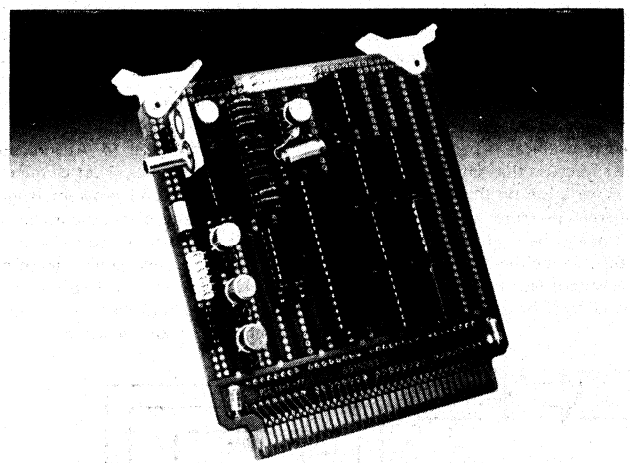
PRESSURE CONTROL CARD



The A/D Easily Allows Many Unusual Applications

National Semiconductor
Application Note 233
September 1979

Accommodation of Arbitrary Analog Inputs

Two design features of the ADC0801 series of A/D converters provide for easy solutions to many system design problems. The combination of differential analog voltage inputs and a voltage reference input which can range from near zero to $5V_{DC}$ are key to these application advantages.

In many systems the analog signal which has to be converted does not range clear to ground ($0.00V_{DC}$) nor does it reach up to the full supply or reference voltage value. This presents two problems: 1) a "zero-offset" provision is needed — and this may be volts, instead of the few millivolts which are usually provided; and 2) the "full scale" needs to be adjusted to accommodate this reduced span. ("Span" is the actual range of the analog input signal, from $V_{IN\,MIN}$ to $V_{IN\,MAX}$.) This is easily handled with the converter as shown in Figure 1.

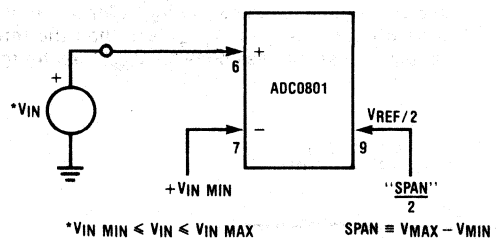


Figure 1. Providing Arbitrary Zero and Span Accommodation

Note that when the input signal, V_{IN}, equals $V_{IN\,MIN}$ the "differential input" to the A/D is zero volts and therefore a digital output code of zero is obtained. When V_{IN} equals $V_{IN\,MAX}$, the "differential input" to the A/D is equal to the "span" (for reference applications convenience, there is an internal gain of two to the voltage which is applied to pin 9, the $V_{REF}/2$ input), therefore the A/D will provide a digital full scale. In this way a wide range of analog input voltages can be easily accommodated.

An example of the usefulness of this feature is when operating with ratiometric transducers which do not output the complete supply voltage range. Some, for example, may output 15% of the supply voltage for a zero reading and 85% of the supply for a full scale reading. For this case, 15% of the supply should be applied to the $V_{IN(-)}$ pin and the $V_{REF}/2$ pin should be biased at one-half of the span, which is ½ (85% − 15%) or 35% of the supply. This properly shifts the zero and adjusts the full scale for this application. The $V_{IN(-)}$ input can be provided by a resistive divider which is driven by the power supply voltage and the $V_{REF}/2$ pin should be driven by an op amp. This op amp can be a unity-gain voltage follower which also obtains an input voltage from a resistive divider. These can be combined as shown in Figure 2.

This application can allow obtaining the resolution of a greater than 8-bit A/D. For example, 9-bit performance with the 8-bit converter is possible if the span of the analog input voltage should only use one-half of the available 0V to 5V span. This would be a span of approximately 2.5V which could start anywhere over the range of 0V to $2.5V_{DC}$.

The RC network on the output of the op amp of Figure 2 is used to isolate the transient displacement current demands of the $V_{REF}/2$ input from the op amp.

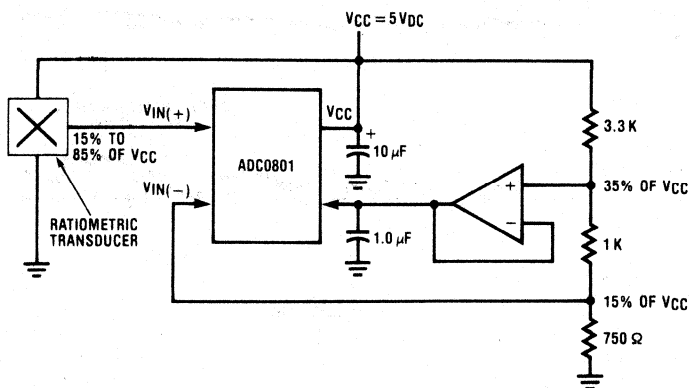


Figure 2. Operating with a Ratiometric Transducer which Outputs 15% to 85% of V_{CC}

Limits of $V_{REF}/2$ Voltage Magnitude

A question arises as to how small in value the span can be made. An ADC0801 part is shown in Figure 3 where the $V_{REF}/2$ voltage is reduced in steps: from A), 2.5V (for a full scale reading of 5V); to B), 0.625V (for a full scale reading of 1.25V — this corresponds to the resolution of a 10-bit converter over this restricted range); to C), 0.15625V (for a full scale reading of 0.3125V — which corresponds to the resolution of a 12-bit converter). Note that at 12 bits the linearity error has increased to ½ LSB.

For these reduced reference applications the offset voltage of the A/D has to be adjusted as the voltage value of the LSB changes from 20mV to 5mV and finally to 1.25mV as we go from A) to B) to C). This offset adjustment is easily combined with the setting of the $V_{IN\,MIN}$ value at the $V_{IN(-)}$ pin.

Operation with reduced $V_{REF}/2$ voltages increases the requirement for good initial tolerance of the reference voltage (or requires an adjustment) and also the allowed changes in the $V_{REF}/2$ voltage over temperature are reduced.

An interesting application of this reduced reference feature is to directly digitize the forward voltage drop of a silicon diode as a simple digital temperature sensor.

A 10-Bit Application

This analog flexibility can be used to increase the resolution of the 8-bit converter to 10 bits. The heart of the idea is shown in Figure 4. The two extra bits are provided by the 2-bit external DAC (resistor string) and the analog switch, SW1. Note that the $V_{REF}/2$ pin of the converter is supplied with 1/8 V_{REF} so each of the four spans which are encoded will be:

$$2 \times \frac{1}{8} V_{REF} = \frac{1}{4} V_{REF}$$

In an actual implementation of this circuit, the switch would be replaced by an analog multiplexer (such as the CD4066 quad bilateral switch) and a microprocessor would be programmed to do a binary search for the two MS bits. These two bits plus the 8 LSBs provided by the A/D give the 10-bit data. For a particular application, this basic idea can be simplified to a 1-bit ladder to cover a particular range of analog input voltages with increased resolution. Further, there may exist *a priori* knowledge by the CPU which could locate the analog signal to within the 1 or 2 MSBs without requiring a search algorithm.

A Microprocessor Controlled Voltage Comparator

In applications where set points (or "pick points") are set up by analog voltages, the A/D can be used as a comparator to determine whether an analog input is greater than or less than a reference DC value. This is accomplished by simply grounding the $V_{REF}/2$ pin (to provide maximum resolution) and applying the reference DC value to the $V_{IN(-)}$ input. Now with the analog signal applied to the $V_{IN(+)}$ input, an all zeros code will be output for $V_{IN(+)}$ less than the reference voltage and an all ones code for $V_{IN(+)}$ greater than the

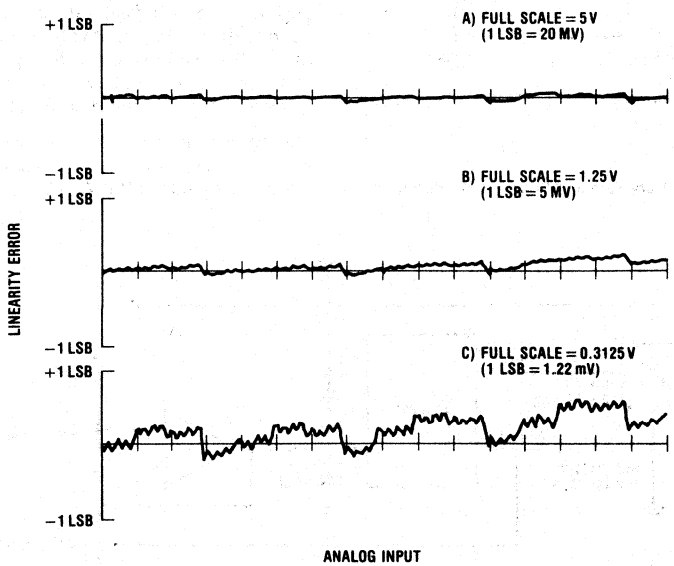


Figure 3. Linearity Error for Reduced Analog Input Spans

reference voltage. This reduces the computational loading of the CPU. Further, using analog switches, a single A/D can encode some analog input channels in the "normal" way and can provide this comparator operation, under microprocessor control, for other analog input channels.

DACs Multiply and A/Ds Divide

Computation can be directly done with converter components to either increase the speed or reduce the loading on a CPU. It is rather well known that DACs multiply — and for this reason many are actually called "MDACs" to signify "multiplying DAC." An analog product voltage is provided as an output signal from a DAC for a hybrid pair of input signals — one is analog (the V_{REF} input) and the other is digital.

The A/D provides a digital quotient output for two analog input signals. The numerator or the dividend is the normal analog input voltage to the A/D and the denominator or the divisor is the V_{REF} input voltage.

High speed computation can be provided external to the CPU by either or both of these converter products. DACs are available which provide full 4-quadrant multiplications (the MDACs and MICRO-DACs™), but A/Ds are usually limited to only one quadrant.

Combine Analog Self-Test with Your Digital Routines

A new innovation is the digital self-test and diagnostic routines which are being used in equipment. If an 8-bit A/D converter and an analog multiplexer are added, these testing routines can then check all power supply voltage levels and other set point values in the system. This is a major application area for the new generation converter products.

Control Temperature Coefficients with Converters

The performance of many systems can be improved if voltages within the system can be caused to change properly with changes in ambient temperature. This can be accomplished by making use of low cost 8-bit digital to analog converters (DACs) which are used to introduce a "dither" or small change about the normal operating values of DC power supplies or other voltages within the system. Now, a single measurement of the ambient temperature and one A/D converter with a MUX can be used by the microprocessor to establish proper voltage values for a given ambient temperature. This approach easily provides non-linear temperature compensation and generally reduces the cost and improves the performance of the complete system.

Save an Op Amp

In applications where an analog signal voltage which is to be converted may only range from, for example, $0V_{DC}$ to $500mV_{DC}$, an op amp with a closed-loop gain of 10 is required to allow making use of the full dynamic range ($0V_{DC}$ to $5V_{DC}$) of the A/D converter. An alternative circuit approach is shown in Figure 5. Here we, instead, attenuate the magnitude of the reference voltage by 10:1 and apply the 0 to 500 mV signal directly to the A/D converter. The $V_{IN(-)}$ input is now used for a V_{OS} adjust, and due to the "sampled-data" operation of the A/D there is essentially no V_{OS} drift with temperature changes.

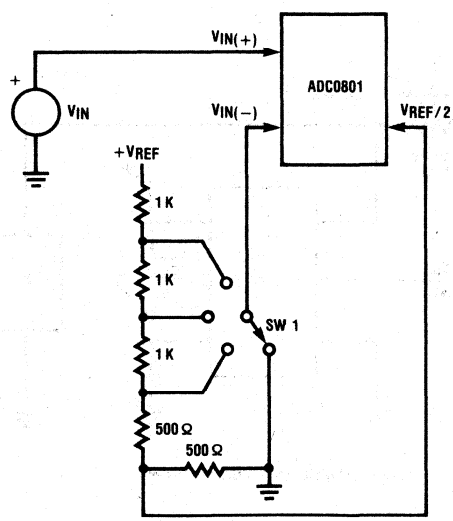


Figure 4. 10-Bit A/D Using the 8-Bit ADC0801

As shown in Figure 5, all zeros will be output by the A/D for an input voltage (at the $V_{IN(+)}$ input) of $0V_{DC}$ and all ones will be output by the A/D for a $500mV_{DC}$ input signal. Operation of the A/D in this high sensitivity mode can be useful in many low cost system applications.

Digitizing a Current Flow

In system applications there are many requirements to monitor the current drawn by a PC card or a high current load device. This typically is done by sampling the load current flow with a small valued resistor. Unfortunately, it is usually desired that this resistor be placed in series with the V_{CC} line. The problem is to remove the large common-mode DC voltage, amplify the differential signal, and then present the ground referenced voltage to an A/D converter.

All of these functions can be handled by the A/D using the circuit shown in Figure 6. Here we are making use of the differential input feature and the common-mode rejection of the A/D to directly encode the voltage drop across the load current sampling resistor. An offset voltage adjustment is provided and the $V_{REF}/2$ voltage is reduced to 50 mV to accommodate the input voltage span of 100 mV. If desired, a multiplexer can be used to allow switching the $V_{IN(-)}$ input among many loads.

Conclusions

At first glance it may appear that the A/D converters were mainly designed for an easy digital interface to the microprocessor. This is true, but the analog interface has also been given attention in the design and a very useful converter product has resulted from this combination of features.

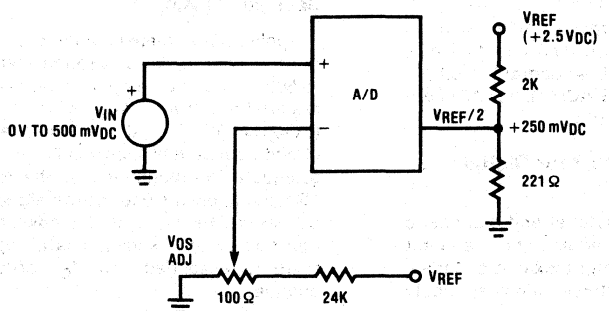


Figure 5. Directly Encoding a Low Level Signal

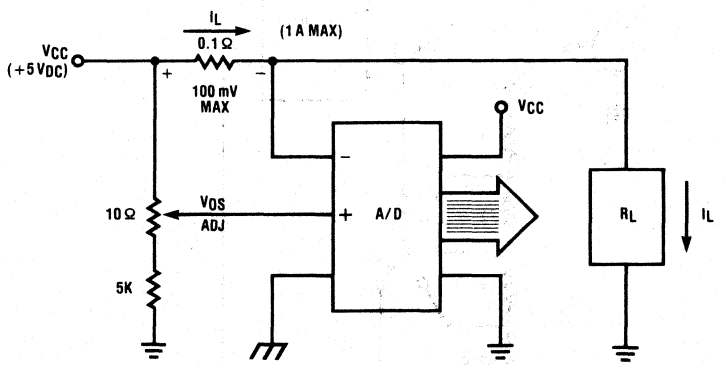


Figure 6. Digitizing a Current Flow

A Microprocessor Controlled Pressure Regulator

National Semiconductor
Application Note 234
Duane Tandeske
July 1979

Introduction

In pneumatic systems, some form of pressure regulation is usually required. The most popular method has been the mechanical pressure regulator. For more than one pressure or vacuum, however, multiple pressure regulators must be employed. Using a microcontroller[1] with a pressure transducer and suitable valving, multiple values of both pressure and vacuum can be controlled by a single system. The microcontrolled regulator can be used for either specific or delta pressures and lends itself to generation of pressure cycles. The entire system is under program control, providing additional advantages of flexibility, self-test, and improved reliability.

Basic Pressure Regulator

To implement the pressure regulator, the microcontroller is used in a closed-loop configuration. As shown in Figure 1, the microprocessor alternately measures the chamber pressure then pulses the appropriate supply and bleed valves to bring the pressure to the desired value. Photo 1 shows a valve arrray for pressure control. Each pressure measurement is auto-referenced,[2] to compensate for measurement offset[3] errors, and chamber pressure is corrected with a coarse/fine valve system, which allows a simple microprocessor interface yet maintains regulator speed and accuracy.[3] The total system accuracy is determined by the repeatability and resolution of each measurement.

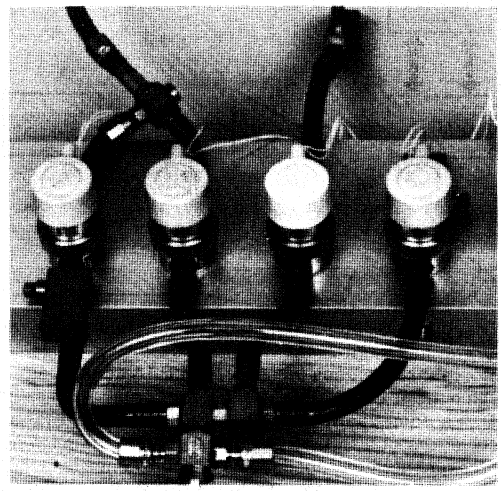


Photo 1. Pressure Regulator Valve Array.

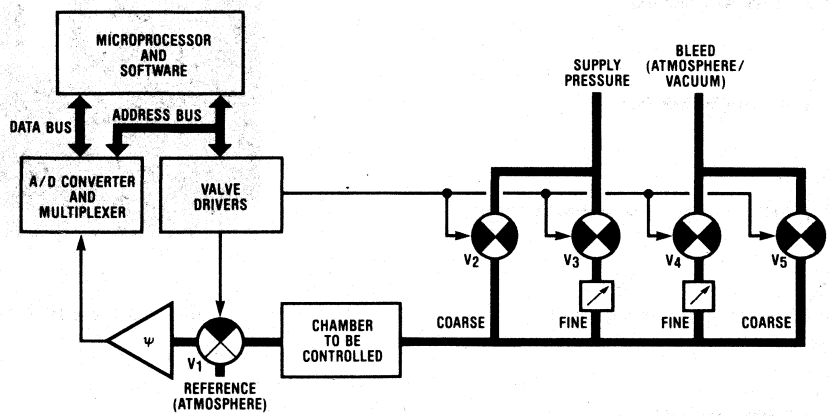


Figure 1. Basic Microcontrolled Pressure Regulator.

Pressure Measurement — Auto-Referencing

As shown in Figure 2, the chamber pressure is measured with an A/D converter and a pressure transducer connected to the chamber via a three-way valve. This valve allows the measurements to be corrected for offset errors by auto-referencing to a stable reference pressure. To control either specific gage pressure or delta pressures, the stable reference can be the ambient atmosphere. (Delta pressure can be the difference in the pressures of two chambers at the same time or of one chamber at different times.)

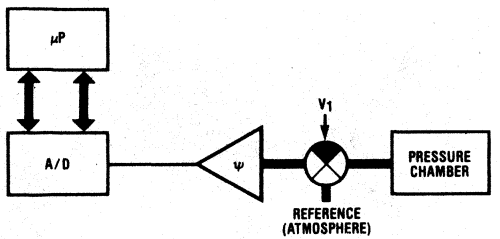


Figure 2. Pressure Measurement Channel.

The program steps required for autoreferencing are shown in Figure 3. The microprocessor first reads and stores the reference pressure then subtracts the stored value from each measurement of chamber pressure. This automatically corrects each measurement for offset errors due to time and temperature. The reference pressure normally needs to be read only once for a large number of measurements, since offset drift is slow by comparison.

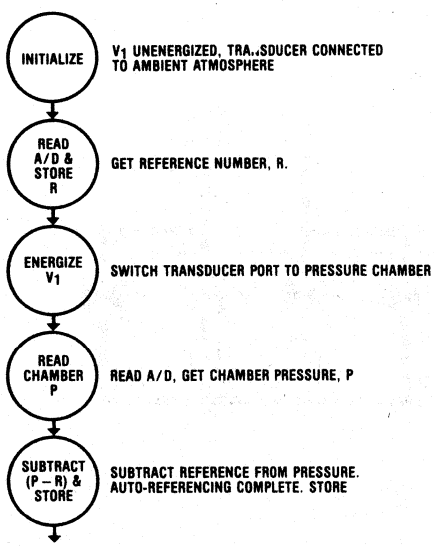


Figure 3. Pressure Measurement Cycle.

In designing the measurement channel, the transducer and A/D converter should be treated as a single component, with individual linearity,[3] resolution, and temperature coefficients[3] combined to determine resolution and accuracy. This is straightforward arithmetically, but finding an A/D converter and pressure transducer that are directly compatible in voltage level (offset) and swing (span)[3] may not be an easy task.

Most A/D manufacturers have standardized input ranges of 0 to 5V, 0 to 10V, or −5V to +5V; whereas, the output levels of pressure transducers can vary widely. This means that some form of signal conditioning,[4] such as level shifting or span adjustment, will most likely be required.

In addition, care must be taken to ensure that time and temperature-induced errors do not cause the transducer output to exceed the input range of the A/D converter.

For example, if the chosen A/D converter has an input range of 0 to 10V, and the transducer has a maximum offset drift of ±0.4V, the transducer output should be 0.5V to 9.5V for the desired pressure range. For transducer errors that increase with applied pressure, it may be necessary to allow a larger margin at the upper limit. This will ensure that the transducer output never exceeds the A/D converter limits over the working temperature range. Photo 2 shows a 12-bit A/D and 16 channel MUX Card.

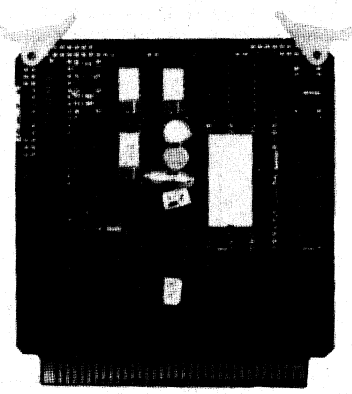


Photo 2. A/D and MUX Card.

Pressure Control — Coarse/Fine Valves

After measuring pressure the microcontroller corrects the chamber pressure by pulsing solenoid valves. These connect the chamber to *bleed* if pressure is too high and to *supply* if too low. The pressure change resulting

from a single pulse will depend on chamber volume, source pressure, pulse duration, and size of the valve orifice.

While individual fine valves could be used for *supply* and *bleed* corrections, improved accuracy versus speed can be achieved using coarse and fine valves with different orifice sizes. The function of the valves is analogous to an A/D converter, as shown in Figure 4. A "counting" A/D, which is similar to the fine valve approach, is much slower because of the high number of counts required. The use of several degrees of coarseness is similar to the successive approximation A/D, where the number of bits determines accuracy and speed is constant. The higher order bits get close to the desired value, and the low order bits determine tolerance. Analogously, in the coarse/fine regulator, the coarse valve quickly brings the pressure near the desired value, then the fine valve brings it within tolerance.

Coarse/fine control is implemented in the program by setting up fine and coarse limits, as shown in Figure 5. If the measured pressure is outside the coarse limits, the coarse valve is activated. This brings the pressure within the coarse limits, after which the fine valve is used. Within the fine limits, the pressure is within tolerance, and no correction is needed. To avoid hunting, the following conditions should hold:

Fine Increment $\leq 2x \pm$ Fine Limit
Coarse Increment $\leq 2x \pm$ Coarse Limit

Appropriate delays may also be needed in the program to allow pressure to change by the desired amount.

The Control Program

The flow diagram for the basic pressure regulator (Figure 1) is shown in Figure 6. This program must include the values and limits for each pressure to be controlled, with separate limits for the coarse and fine valves. These values will probably have to be entered as binary numbers.

The initial valve conditions are: V_2 through V_5 are closed, and V_1 is connected to atmosphere; and the system is ready to read and store the first atmospheric pressure value. Since atmospheric pressure changes slowly, it may be read only once for each major cycle, which may include many pressure settings.

With the atmospheric pressure stored in memory, the program "gets" the control pressure value then reads the chamber pressure. The microprocessor then performs the auto-reference step by subtracting atmospheric pressure from chamber pressure. The auto-referenced value is subtracted from the control pressure value, then the difference is compared with the coarse limits. If it is outside coarse limits, a coarse adjustment is made; if inside, a fine adjustment is made; until the chamber pressure is within tolerance.

For example, if the tolerance is ±0.15 psi, the fine limits are set to ±0.15 psi, and the fine valves can be set for 0.2 psi increments to avoid hunting:

$|0.2| \leq 2x| \pm 2.6|$.

Likewise, if the coarse increment is set for 5 psi, the coarse limits could be set for ±2.6 psi.

Then, if the first control pressure value is 12 psig, and the chamber is initially at atmospheric pressure, 0 psig, or 12 psi below control pressure, the coarse valve is actuated. The chamber pressure is then read again as 5 psig, 7 psig below the desired value. A second coarse pressure increment brings the chamber to 10 psig, which is 2 psi low but within the coarse limits (±2.6 psi).

Next, the chamber pressure error is compared with the fine limits. Since the pressure is 2 psi low, the fine valve will be pulsed 10 times and the chamber pressure read after each pulse. After the tenth pulse, the chamber pressure is read to be within the fine limits, now 12 psig ±0.15 psi, and the system can either continue regulating to that pressure or get the next control pressure value.

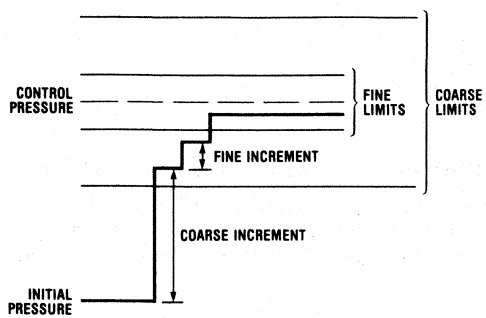


Figure 4. Single vs Multiple Valves.

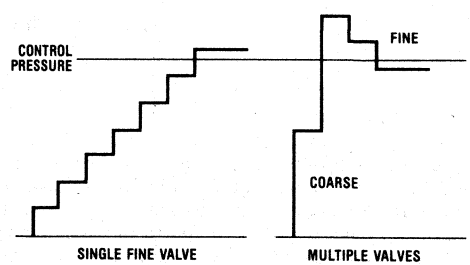


Figure 5. Fine and Coarse Limits.

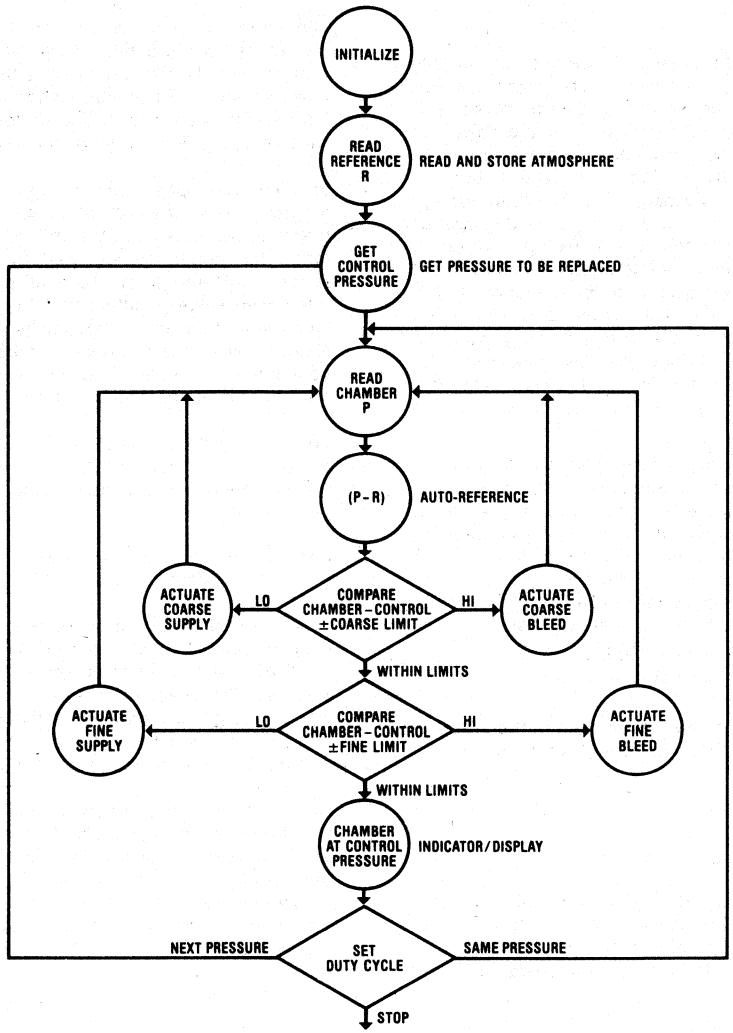


Figure 6. Flow Diagram for Basic Pressure Regulator.

To minimize tolerance build-up for delta pressure readings, the last pressure reading should be saved and used as a base for the next control pressure value. For example, if the control pressures are 12 psig, 17 psig, and 28 psig, 5 psi would be added to the last 12 psig reading to obtain the 17 psig control value, and 11 psi would be added to the last 17 psig reading to obtain the 28 psig value. The deltas would then be 5 psi ±0.15 psi and 11 psi ±0.3 psi. If the specific pressure is important, rather than the delta value, the numeric value of each control pressure would be entered and used as the basis for regulation.

Options and Expansion — Additional Hardware

The microcontrolled pressure regulator is highly flexible and can be modified or expanded to provide improved accuracy and reliability as well as additional functions.

With one additional valve, the source pressure could be monitored and an alarm or pump command given if it goes below a certain value. Displays indicating when chamber pressures are within tolerance could also be added (Figure 6).

If a wide range of pressures are to be controlled, additional measurement channels can enhance accuracy at lower pressures, as shown in Figure 7. An extra channel can also provide self-test and improved reliability. If additional chambers are to be controlled, the regulator can be expanded by adding a 3-way valve and a 2-way valve for each additional chamber, as shown in Figure 8.

An external timer, or analog inputs to the A/D converter, would allow the regulator to generate specific pressure-time sequences, with additional programming, of course. Another use of the timer would be coarse/fine pressure control using pulse length variation rather than multiple valves with different orifice sizes.

With additional software, the pressure chamber could be checked for leaks or usage rate, or statistical data, such as numbers of cycles per day or week, could be recorded automatically.

Summary

As evidenced by easily available hardware and the simplicity of programming, the microcontrolled pressure regulator is a viable alternative to the mechanical type regulators used in the past. Yet, because of its high degree of flexibility, it can be much more: a total solution to the problem of pressure control, with all the advantages of easy software control of system parameters, self-test, monitoring, and display.

References — National Semiconductor Publications

1. AN218, A Pressure Microcontroller, Duane Tandeske.
2. 1977 Pressure Transducer Handbook, Section 7.
3. 1977 Pressure Transducer Handbook, Sections 3 and 16.
4. 1977 Pressure Transducer Handbook, Section 8.

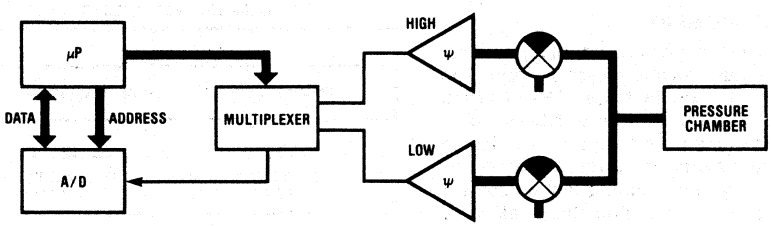


Figure 7. Dual Transducers for Wide Pressure Range.

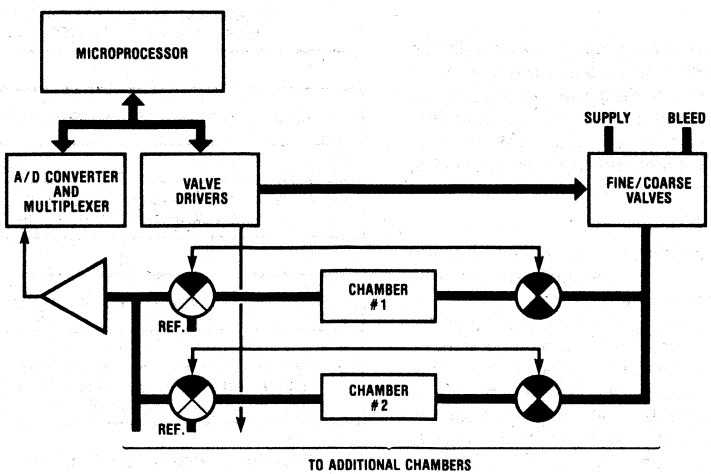


Figure 8. Expansion to Multiple Chambers.

AUTOMATIC MULTIPOINT PRESSURE MEASUREMENT: Pressure is Measured and Controlled by Microcomputer with 12-Bit A/D Resolution

National Semiconductor
Application Note 235
Milt Schwartz
November 1979

ABSTRACT

Pressure transducers are interfaced with a microprocessor for the purpose of transducer test and characterization by multipoint measurement. The design principles and resulting equipment have broader applications in robotic control.

INTRODUCTION AND SUMMARY

This note provides a step-by-step procedure for developing a multipoint pressure measurement system. The main purpose of the system is to provide low-cost, accurate testing and characterization of NSC's monolithic pressure transducers. However, the design approach can provide a model for automated pressure system development, and the resulting test equipment can be useful to transducer users, either stand-alone, or as part of a larger measurement or control system.

For the transducer user, the most obvious value of a multipoint pressure measurement system is incoming quality assurance. More often, however, the user requires further characterization and selection of transducers for end-use equipment. Less obvious, but more important, the automatic measurement system can be incorporated as a cost-effective part of end-use equipment for pressure measurement or control applications.

In either case, a methodical approach to system design is recommended. This note offers a description of NSC's development procedure, including the make/buy decision, functional definition of the system, and design considerations for both pneumatic and electronic circuits. The appendix includes detailed descriptions of circuits, microprocessor programs, and data formats.

MAKE OR BUY

The advantages of building a test system include capability of custom tailoring, designing-in flexibility, and having full understanding of system operation. However, implementation may require capability for servicing and documentation. In addition, the time to bring up the system may be greater than with off-the-shelf equipment. Of course, the decision is simplified if no commercial equipment exists, which was the case at National Semiconductor's pressure transducer operation. A system with the needed flexibility for characterizing new devices was unavailable.

PROBLEM ANALYSIS

A clear picture of the transducer test problem is shown in the function diagram of *Figure 1.*

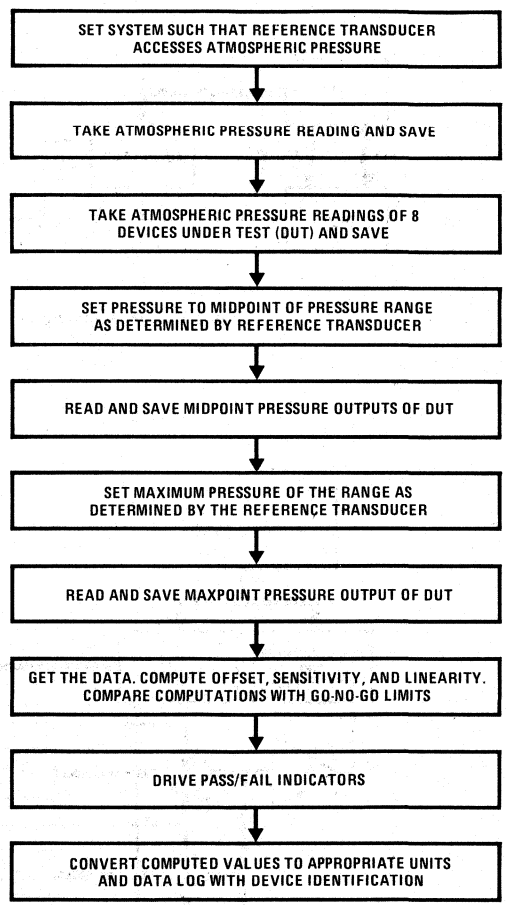


FIGURE 1. Basic Functions Required for Testing 8 Gage Sensors

The required testing could be implemented with manual valves, pressure regulators, and a voltmeter. The chief advantage of manual implementation is flexibility, but this approach would require an operator possessing dexterity as well as mathematical skills. A tireless hand would also be necessary to perform the calculations and log data. Other disadvantages include slow testing and possibility of read, record, and calculation errors, as well as excessive use of skilled labor.

For these reasons an automatic measuring system was considered necessary, and a microprocessor-based system appeared to be a viable choice to perform the envisioned tasks. The INS8060 microprocessor was chosen for the following reasons:

- Engineering was familiar with the processor and its development system
- System and prototyping cards were readily available
- Hardware interfacing appeared to be straightforward
- An interpreter with I/O commands was available to speed up coding time and provide on-line debug

The function chart *(Figure 1)* and block diagram (*Figure 2*), plus prior experience in developing a pressure microcontroller,[1] indicated a need for the following hardware:

- Array of valves for measurement and control of pressure, with a custom card containing circuitry to drive the valves and indicator lights
- A/D card with 12-bit resolution and analog multiplexer (MUX) with capability to accept differential and single ended input
- ROM card(s) for program and RAM card(s) for data storage
- A terminal for debug as well as operator interaction in the final system

The resulting transducer test system may be used as a data-logger, histogram generator, and a go/no-go production tester. It has the capability of testing and data-logging 8 absolute, gage, or differential pressure devices with differential outputs; or 16 absolute, gage, or differential pressure devices with single ended output. Also included is a diagnostic check for system leakage.

PRELIMINARY SYSTEM DESIGN

The heart of this robotic system is a microcomputer-controlled pressure regulator[2], as shown in *Figure 3*. The input fluid is compressed air, allowing the simple plumbing and valve array of photo 1. This regulator applies specified values of pressure to the "9" position of the dead-end manifold, as shown in *Figure 4* and in photographs 2 and 3. The pressures are measured by the reference transducer, an NSC LX1730G, which is connected to the pressure/vacuum input line that feeds the manifold. This transducer is periodically calibrated using a precision pressure standard. Its sole function is to measure the pressure in the manifold. To achieve the required 2% system accuracy, auto-referencing techniques were employed[3]. The INS8060 microcomputer used for digital control consists of:

- CPU application card
- NIBL ROM card (National Industrial Basic Language Interpreter)
- Two standard 4k x 8 PROM cards which contain the operating program
- Standard 2k x 8 RAM card
- Custom 12-bit A/D card
- Custom solenoid valve/LED driver card
- System peripherals: a terminal for data recording and input commands, six solenoid two-way valves, and a panel of go/no-go LED indicators

The resulting system architecture is shown in *Figure 5*.

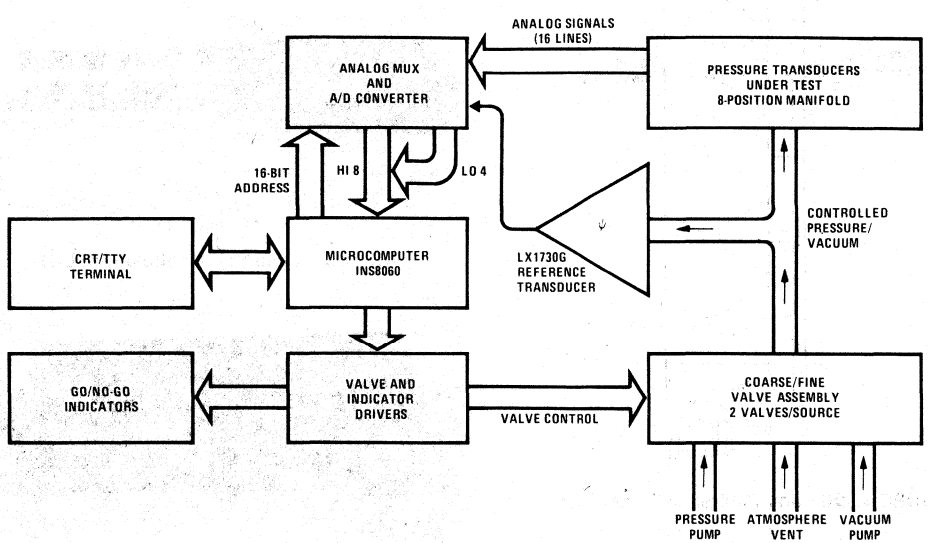


FIGURE 2. Functional Block Diagram

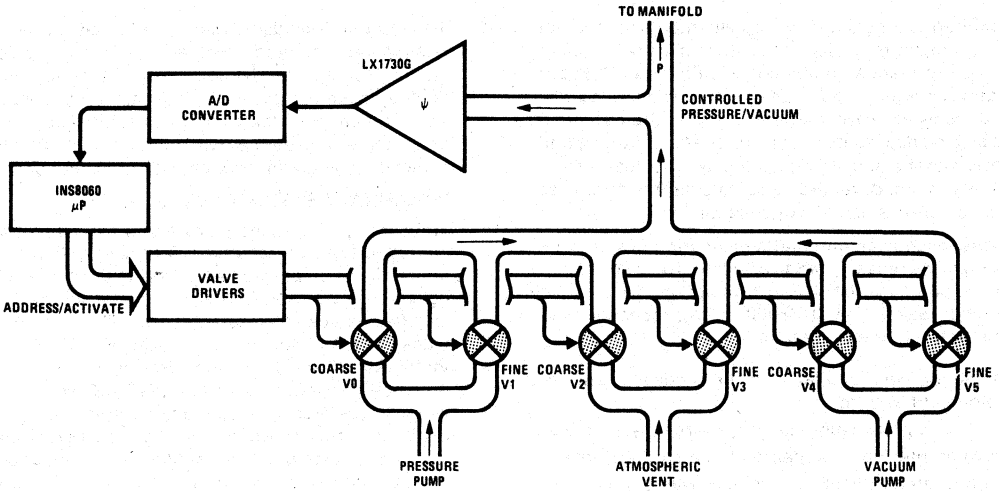


FIGURE 3. Pressure Control Loop

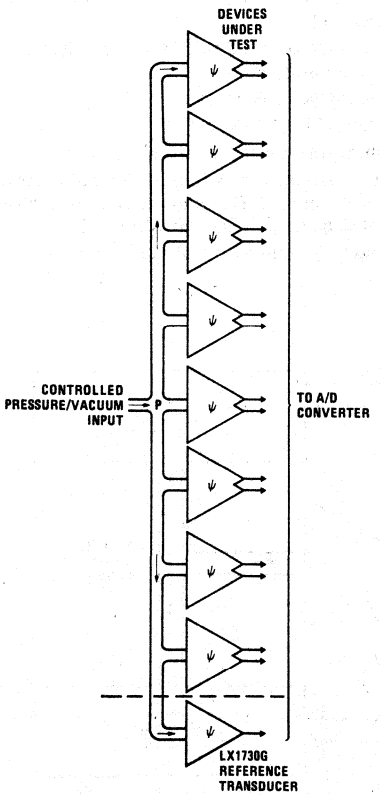


FIGURE 4. DUT and Reference Transducer

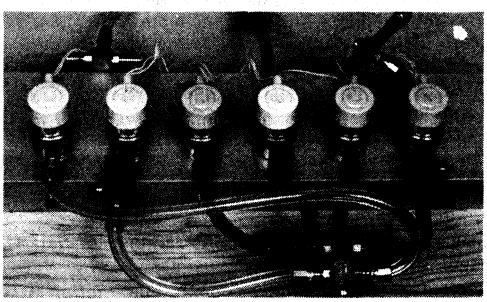


PHOTO 1. Solenoid Valve Array

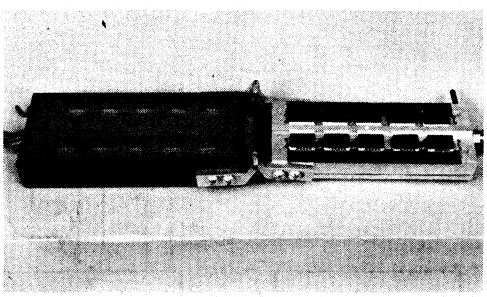


PHOTO 2. Open Test Manifold with DUT

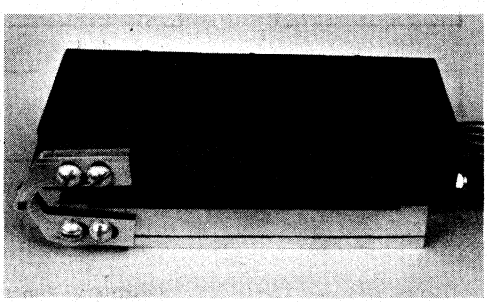


PHOTO 3. Closed Test Manifold

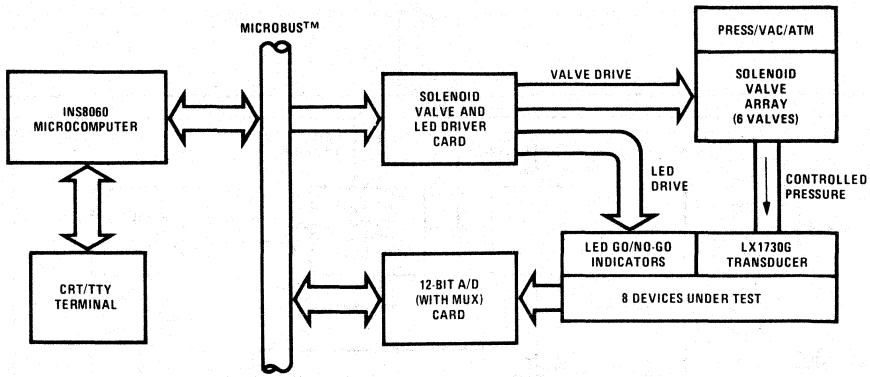


FIGURE 5. System Architecture

SYSTEM HARDWARE DESIGN

The electronic hardware design reflects consideration of measurement requirements. It was known that the monolithic devices under test (DUT) provide differential outputs that range from 2.5 mV/psi to 8.5 mV/psi over a 30 psi range. Also, offset (output at 0 psi) could be on the order of ± 100 mV. The worst case output value over a 30 psi range was expected to be ±355 mV (span + offset)[4]. The reference transducer (LX1730G) has an output span of 1V for a 30 psi range.

The LX1730G was chosen because its 1V output span for a range of 30 psi is about the same as that of the monolithic DUT. Therefore all transducers can share the same amplifier without sacrificing system accuracy. For greater system flexibility with respect to choice of reference and DUT, additional amplifiers and analog switches may be included.

It was determined that an amplifier gain of 15 in conjunction with a 12-bit A/D, set for ± 10V input, would be the best compromise to interface the microprocessor. Bipolar operation of the A/D was necessary to accommodate devices producing opposite polarity voltage. This configuration results in a maximum input to the A/D of ± 7.5V, thus ensuring that the A/D does not saturate. The reference transducer is scaled such that the output changes from − 0.5V to + 0.5V for a pressure change of 0 psi to 30 psi. The resulting amplifier output changes from − 7.5V to + 7.5V.

Analog multiplexing was required to read the 8 DUT as well as the reference transducer output. The digital circuitry was designed to allow A/D interface and mode selection so that the microprocessor communicates with the analog circuitry. These functions are shown in *Figure 6*. Detailed schematics and a photograph of the data acquisition card are shown in Appendix A.

SOLENOID VALVE AND LED DRIVER DESIGN

A solenoid valve/LED indicator driving card was required, with several addressable latches to drive transistors capable of sinking 100 mA. It appeared that 24 outputs would be adequate for most NSC needs. The board was designed with the capability of expansion to 56 outputs. *Figure 7* shows the functional diagram for this card. Detailed schematic, photo and address control are given in Appendix B.

DATA INTERPRETATION

In the configuration chosen, the 12-bit A/D converter will respond to an input voltage change of 20V (− 10V to 10V). Since a 12-bit binary converter resolves 2^{12} (4096) counts, each bit corresponds to 4.9 mV (20V/4096 counts).The reference transducer has a sensitivity of 33 mV/psi. The amplifier has a gain of 15. Thus, the input sensitivity of the A/D is 495 mV/psi. Each psi of pressure change is represented by 101_{10} counts out of 4096_{10} counts (495 mV/psi/4.9 mV/bit). For our calculations, 100_{10} counts per psi were used. Therefore, 0.1 psi (ten counts) is easily resolved by the 12-bit converter. Since the microprocessor data word is 8 bits wide and the A/D output is 12 bits wide, two read instructions must be executed to retrieve the 12-bit data. The two bytes of data (Hi 8 and Lo 4) are stored in memory. The A/D board appears as a block of memory locations (hexadecimal 8000 to 81FF) to the microcomputer as shown in the memory map of *Figure 8*.

DATA RETRIEVAL

The analog data from the transducers must be routed to the analog MUX outputs. The transducer signals are hard-wired to the inputs of both MUXs *(Figure 6)*. The program presents digital address and data configurations in specified sequences which appear at the inputs of the address decoder, channel select latches, and the mode select latch. The first instruction applies addresses to the address decoders, 8000 (hexadecimal for MUX A) and 8001 (hexadecimal for MUX B). The decode of these addresses produces a signal which causes the data at the inputs of the channel select latches to be presented to the channel select ports of the MUXs.

The second instruction simultaneously enables the MUX outputs and latches the analog switches. Thus, the analog data is steered through the analog switches and presented to the S/H via the instrumentation amplifier. This is accomplished by presenting address 8002 (hexadecimal) to the address decoder which enables the mode latch such that control data bits are presented to the analog switch circuit and MUXs.

The next instruction causes the analog data to be held in the S/H in preparation for conversion. Data holding is accomplished by a one-bit change in the data to the mode latch which in turn sets the S/H to hold.

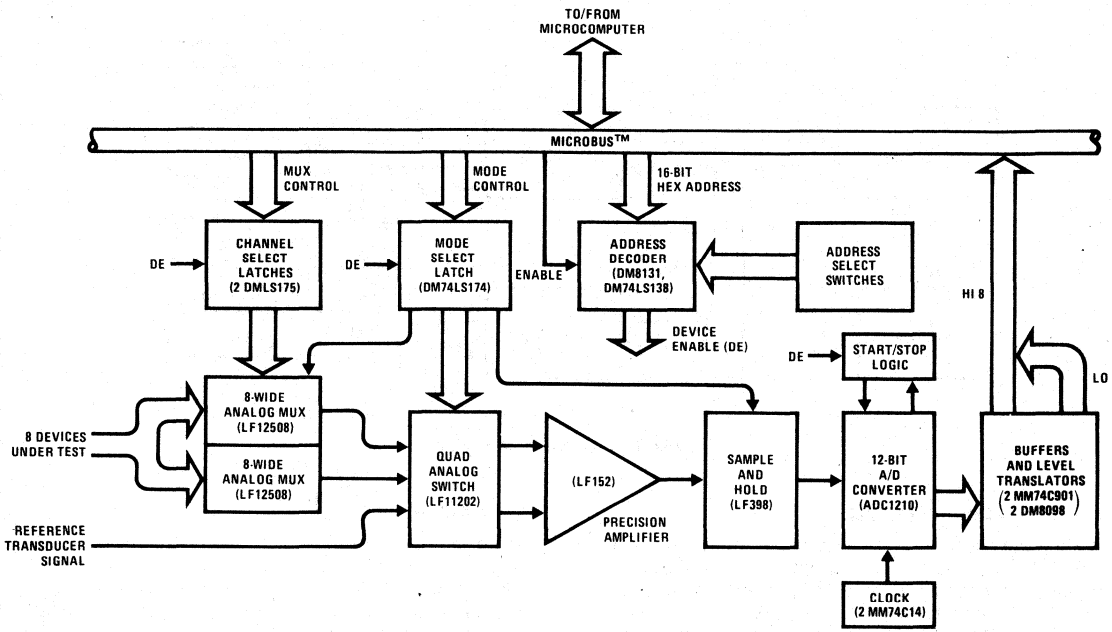


FIGURE 6. A/D Converter and Multiplex Card

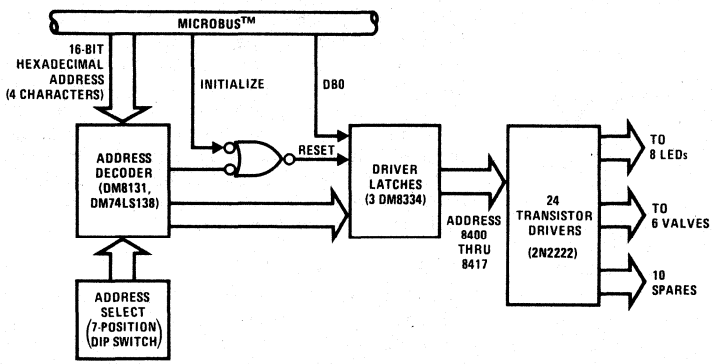


FIGURE 7. LED/Valve Driver Card

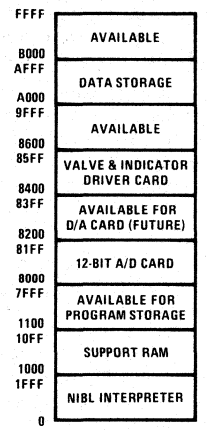


FIGURE 8. System Memory Map

The analog signal at the S/H is hardwired to the A/D circuit input. To start conversion, the first sequential instruction causes 8003 (hexadecimal) to appear on the address bus. The address decoder then produces a pulse to the start circuit *(Figure 6)*.

When conversion is complete, the microprocessor is signaled so that the data may be retrieved. Two read instructions are then executed. The first presents address 8004. The decode of 8004 enables the Hi 8 buffer which presents the high order 8 bits of the result to the data bus. The second presents address 8005, which in like fashion enables the low order 4 bits of the result to the data bus. Refer to the program sequence in Appendix C for detailed program of data retrieval.

ACTUATION DETAIL

At initialization, all 24 transistors are off (*Figure 7* and Appendix B). This is caused by a pulse on the INIT* signal line which occurs at power-on. To turn an output transistor on or off, an instruction is executed which produces address and data that appear at the inputs of the address decoder and octal driver latches. The address decoder produces an enabling signal to one of the three driver latches. This enabling signal allows one of the eight flip-flops in the selected driver latch to be either set or cleared. When the data bit (DB0) is a logic one, the selected flip-flop is set, so as to turn on the corresponding output transistor. When DB0 is a logic zero, the flip-flop is cleared, turning off the corresponding output transistor. Twenty four individual instructions in any desired sequence are executed to achieve the desired on/off pattern for all the outputs.

SYSTEM OPERATION

The INS8060 microcomputer and a 6 valve array act as a finely tuned pressure regulator[2]. The regulator presents the sets of pressure values to the 8 DUT. In the testing of NSC monolithic gage devices the pressure values are atmospheric, atmospheric +15 psi, and atmospheric +30 psi. In the testing of NSC monolithic absolute devices, the pressure values are vacuum, vacuum +15 psi, and vacuum +30 psi. Each case results in a span of 30 psi, which is the specified range for these devices.

Readings are made via the 12-bit A/D and are saved in memory. Software algorithms transform the data into 3 meaningful outputs . . . offset, span, and linearity. These outputs are compared against set point limits. LED (go/no-go) indicators for each DUT are activated. The operator may ask for the actual parametric data via the terminal.

Prior to each set of readings, the system is auto-referenced, thus, eliminating common-mode errors. Two checks (one hardware, the other software) inform the operator that the system is working correctly. First, each of the 6 pressure/vacuum/vent valves has its own indicator light that turns on and off with valve actuation. During a normal pressure cycle, the valves are switched many times. Thus, by observation of the valve indicators, system operation can be confirmed.

Second, if the manifold fails to reach the desired pressure within a fixed time, the terminal indicates a mechanical problem. This constitutes the leak test.

The pressure control algorithm employs successive approximation. An example of detail operation when testing a monolithic gage sensor *(Figure 3)* is as follows:

1. Position valve V6 to atmosphere and read the reference transducer. Save value. Position valve V6 to manifold
2. Vent the manifold to atmosphere by first closing pressure and vacuum valves, then open vent valves
3. Read manifold pressure and compare with value from step 1. When values are the same, manifold is at local atmospheric pressure
4. Read the 8 DUT and save data
5. Close vent valves
6. Apply a pressure pulse by toggling valve V0 (coarse adjust). Read manifold pressure and compare to coarse set point limits. If pressure is not within coarse limits, repeat. If pressure is within coarse limits then perform similar sequence using valve V1 (fine adjust). If the pressure becomes too high, sequence the vent valves in similar fashion until final pressure is obtained
7. Read 8 DUT and save data
8. Repeat steps 6 and 7 for remaining pressure values
9. Calculate offset, linearity and sensitivity using the stored values
10. Compare calculated values against limits. Activate go (green) or no-go (red) indicator for each of the 8 DUT. Log the failures with device identification and the parameter that failed

See Appendix D for typical data-log of failed parts, engineering data-log, and histogram output. Appendix E shows the program instructions.

RESULTS

The prototype system, now being used in production, has resulted in a throughput rate of 160 devices/hr, a fivefold increase over manual testing.

Measurement accuracy of the system is:

Offset: ±1 mV = 2% typical

Sensitivity: ±0.1 mV/psi = 2% typical

Accuracy when compared with a precision pressure standard is also 2%, which was adequate for NSC needs. Potential improvements to the system include adding a programmable instrumentation amplifier so that a family of DUT can be tested and other reference transducers used. Accuracy in the existing NSC system is not limited by the reference transducer nor by the A/D converter, but rather by the 16-bit fixed point arithmetic of the existing software. Adding a machine language floating point arithmetic package can improve both accuracy and throughput.

OVERVIEW

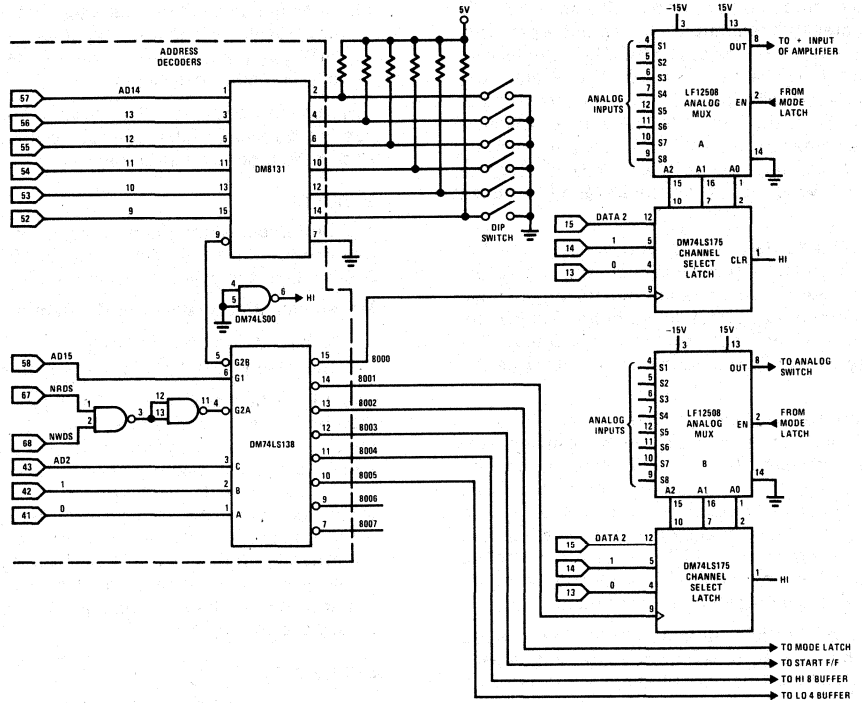
As implied by the title and stated in the introductory paragraphs, much broader application of the system can be implemented than for characterization of NSC monolithic pressure transducers. The system, as presented, is equally applicable with transducers measuring pressure, temperature, flow, load and position. The techniques used extend easily to automotive diagnostics, machine controls, process controls, and commercial controls (HVACR).

In implementing the multipoint measurement system, the imminent practicality of automated control has been demonstrated. The advantages are flexibility, cost savings, and potential applications limited principally by design ingenuity. This lends strong credibility and motivation toward development of future feedback systems necessary for robotic control.

BIBILIOGRAPHY

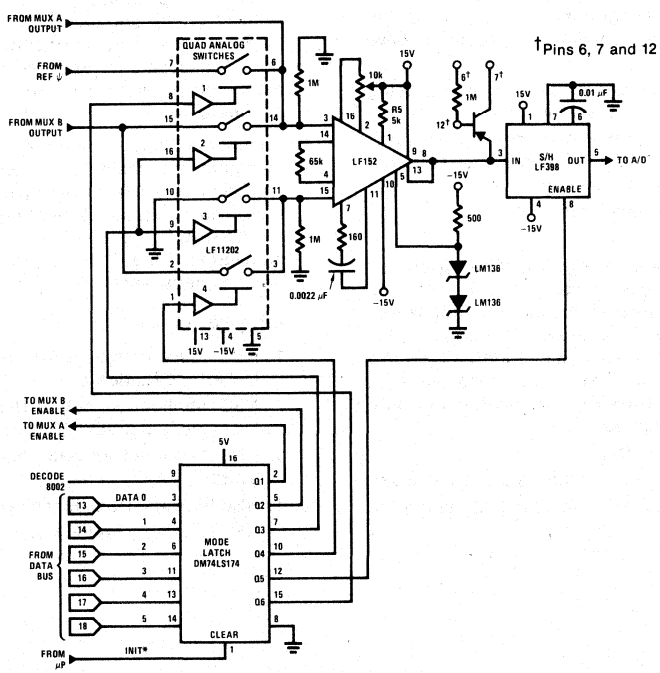
1. NSC application note AN-218 "A Pressure Microcontroller", D. Tandeske
2. NSC application note AN-234 "A Microcontrolled Pressure Regulator", D. Tandeske
3. NSC Pressure Transducer Handbook (1977), Sections 3 and 7
4. NSC Pressure Transducer Handbook (1977), Section 16
5. NSC Data Acquisition Handbook (1978)

APPENDIX A
DATA ACQUISITION CARD



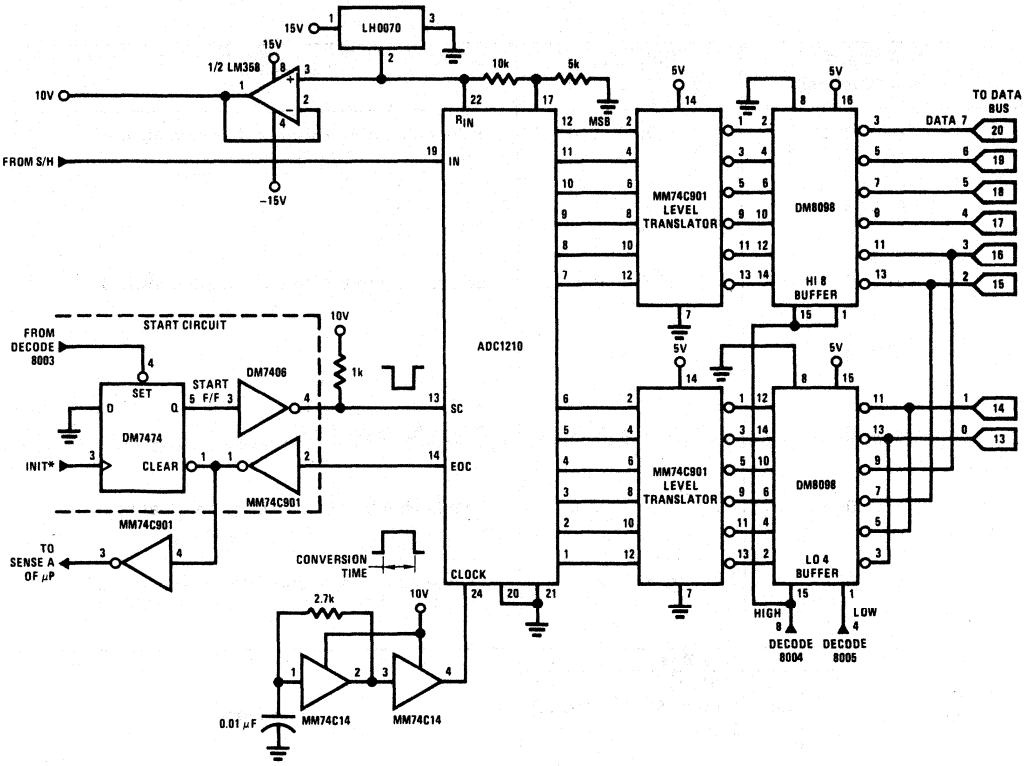
ADDRESS DECODERS AND MUXs

FIGURE A1. Data Acquisition Card Schematic



ANALOG CHANNEL AND MODE LATCH

FIGURE A2. Data Acquisition Card Schematic



LEVEL TRANSLATOR AND A/D CONVERTER
FIGURE A3. Data Acquisition Card Schematic

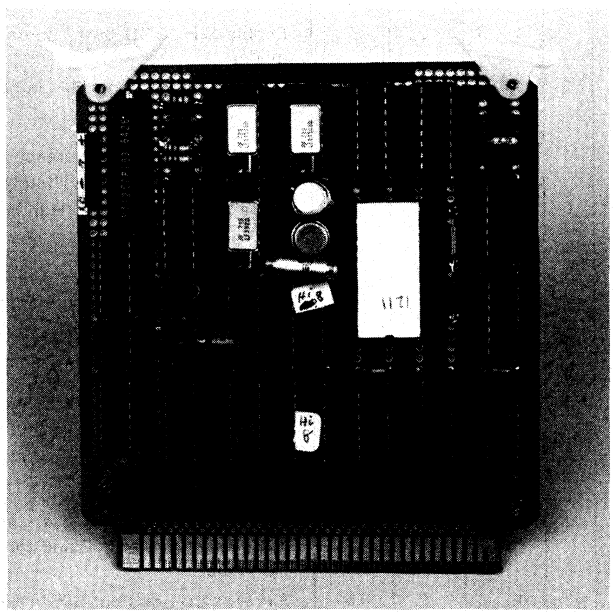


PHOTO A1. 12-Bit Data Acquisition Card

Address (Hexadecimal)	Data Bits 5 4 3 2 1 0	Comments
8 0 0 0	X X X 0 0 0	Select channels 1 thru 8 of analog MUX A
8 0 0 0	X X X 1 1 1	
8 0 0 1	X X X 0 0 0	Select channels 1 thru 8 of analog MUX B
8 0 0 1	X X X 1 1 1	
8 0 0 3	X X X X X X	Start A/D converter
8 0 0 4	X X X X X X	Enable Hi 8 bits of converter onto data bus
8 0 0 5	X X X X X X	Enable Lo 4 bits of converter onto data bus

Address (Hexadecimal)	Data Bits						Comments
	Refr. ψ	S/H	Diff/ Single Control		MUX B	MUX A	
	5	4	3	2	1	0	
8 0 0 2	0	0	0	0	0	0	Initialize condition, analog MUXs disabled, analog switches open, S/H in hold mode
8 0 0 2	0	1	1	1	0	0	Enable S/H, GND both inputs to amplifier (auto zero mode)
8 0 0 2	0	0	1	1	0	0	Same as previous but S/H in hold mode
8 0 0 2	1	1	0	1	0	0	Enable S/H, connect reference transducer to ⊕ input of amplifier and ground ⊖ input (single ended mode)
8 0 0 2	1	0	0	1	0	0	Same as previous but S/H in hold mode
8 0 0 2	0	1	0	1	1	0	Enable S/H, enable MUX A and connect to ⊕ input of amplifier, ground ⊖ input. (single ended mode)
8 0 0 2	0	0	0	1	0	1	Same as previous but S/H in hold mode
8 0 0 2	0	1	0	1	1	0	Enable S/H, enable MUX B and connect to ⊕ input of amplifier, ground ⊖ input (single ended mode)
8 0 0 2	0	0	0	1	1	0	Same as previous but S/H in hold mode
8 0 0 2	0	1	1	0	1	1	Enable S/H, enable MUX A and connect to ⊕ input of amplifier, enable MUX B and connect to ⊖ input (differential mode)
8 0 0 2	0	0	1	0	1	1	Same as previous but S/H in hold mode

FIGURE A4. Data Acquisition Card Operation Summary

APPENDIX B
LED/VALVE DRIVER CARD

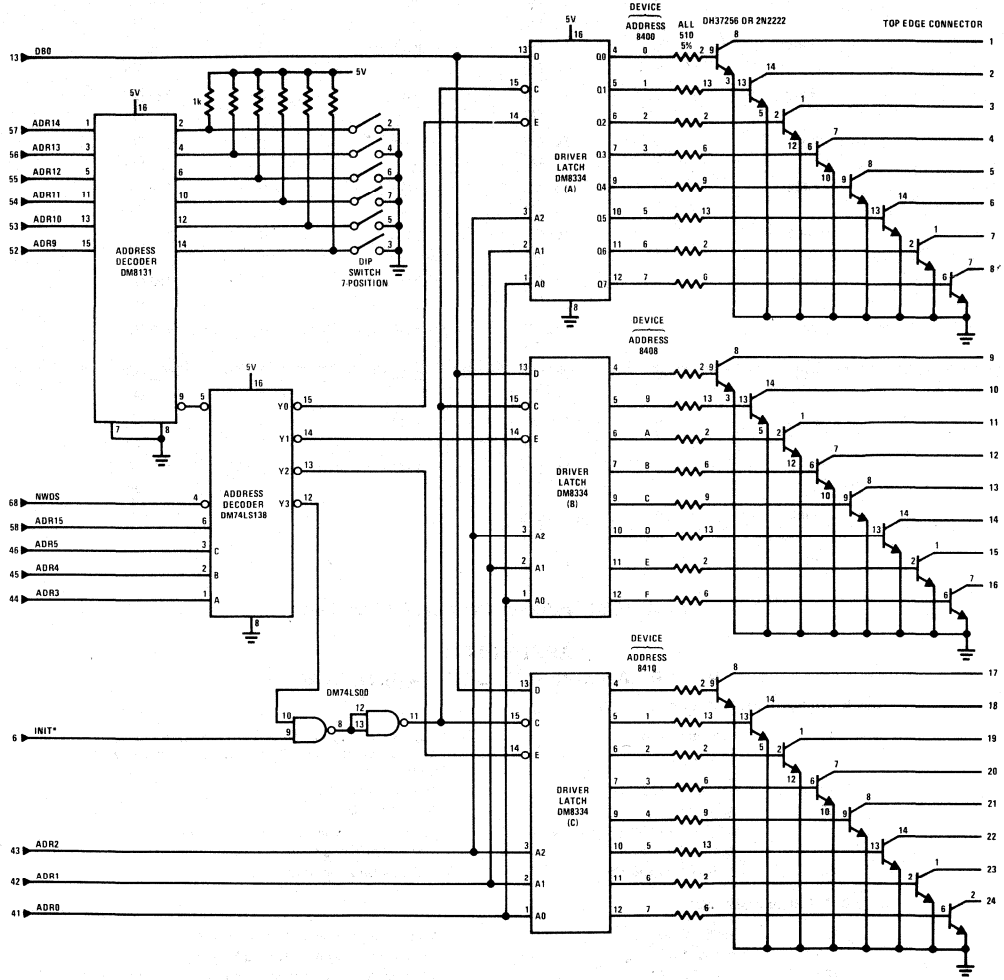


FIGURE B1. Solenoid Valve and LED Indicator Driver Schematic

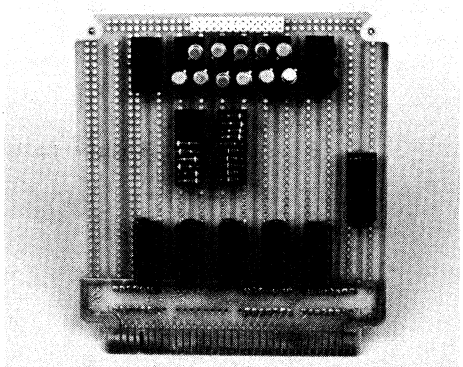


PHOTO B1. Solenoid Valve and LED Indicator Driver Card

Address (Hexadecimal)	DB0	Result	Address (Hexadecimal)	DB0	Result
8400	0	T1 Off	840D	0	T14 Off
	1	On		1	On
8401	0	T2 Off	840E	0	T15 Off
	1	On		1	On
8402	0	T3 Off	840F	0	T16 Off
	1	On		1	On
8303	0	T4 Off	8410	0	T17 Off
	1	On		1	On
8404	0	T5 Off	8411	0	T18 Off
	1	On		1	On
8405	0	T6 Off	8412	0	T19 Off
	1	On		1	On
8406	0	T7 Off	8413	0	T20 Off
	1	On		1	On
8407	0	T8 Off	8414	0	T21 Off
	1	On		1	On
8408	0	T9 Off	8415	0	T22 Off
	1	On		1	On
8409	0	T10 Off	8416	0	T23 Off
	1	On		1	On
840A	0	T11 Off	8417	0	T24 Off
	1	On		1	On
840B	0	T12 Off			
	1	On			
840C	0	T13 Off			
	1	On			

FIGURE B2. Address Control of Driver Card

APPENDIX C
PROGRAM SEQUENCE FOR DATA RETRIEVAL

Read Reference Transducer (Single Ended)

10	@#8002 = #34	Turn on analog switch corresponding to reference transducer, ground one side of amplifier, enable sample and hold
20	@#8002 = #23	Put S/H in hold mode
30	@#8003 = 0	Start A/D converter
40	If (STAT) and (#10) < >0 go to 40	Wait for conversion complete signal
50	@#A000 = @#8004	Get Hi 8 bits and save
60	@#A001 = @#8005	Get Lo 4 bits and save

Read DUT (Differential Mode)

100	@#8000 = 0	Select 1st channel in analog MUX A
110	@#8001 = 0	Select 1st channel in analog MUX B
120	@#8002 = #1B	Connect MUX outputs thru analog switches to the amplifier and enable the sample and hold
130	@#8002 = #B	Put sample and hold in hold mode
140	@#8003 = 0	Start A/D converter
150	If (STAT) and (#10) < >0 go to 150	Wait for conversion complete
160	@#A002 = @#8004	Get Hi 8 bit result and save
170	@#A003 = @#8005	Get Lo 4 bit result and save

Note: # means hexadecimal
@ means contents of

APPENDIX D
TEST RESULT PRINTOUTS

Failure Printout

You can unload the units and wait
Rej 3 Sen
Rej 4 Sen
Rej 4 Lin
Rej 5 Lin
Rej 7 Sen
Rej 7 Lin

Engineering Data Printout

	Offset mV	Sensitivity 10X mV/psi	Linearity 100X psi
1 - 1	26	34	- 19
1 - 2	33	31	59
1 - 3	39	40	- 8
1 - 4	43	39	4
1 - 5	26	29	11
1 - 6	34	29	22
1 - 7	38	34	24
1 - 8	42	31	26

HISTOGRAM PRINTOUT

Offset Histogram - Unit in mV

< – 150 = 10
< – 130 = 0
< – 110 = 0
< – 90 = 0
< – 70 = 0
< – 50 = 1
< – 30 = 0
< – 10 = 0
< 30 = 134
< 50 = 141
< 70 = 10
< 90 = 0
< 110 = 0
< 130 = 0
< 150 = 6

APPENDIX E
SYSTEM PROGRAM

```
Page N   50    Goto K                                                    Initialize and
         100   @#8400 = 0 :@#8401 = 0 :@#8402 = 1 :@#8403 = 1            go to program
         110   @#8404 = 0 :@#8405 = 0 :B = #8000 :Q = 1                  on next page
         112   G = 25000 :Page = Page + 1
-------------------------------------------------------------------------------------
         115   Do
         116   I = #A200
         117   PR "Ready for testing? (Yes or No)" :Input $I
         118   IF @ I = 89 Goto 125
         120   G = 10000 :Page = Page + 1
         125   for I = #8406 to #840D :@ I = I :Next I                   Main program
         126   B = #8000                                                 Test loop
         130   Gosub 6000 :Gosub 4500 :E = T
         240   V = #A000 :Gosub 1200 :F = 0
         250   Gosub 4000
         225   If F = 1 then Goto 420
         300   V = #A030 :Gosub 1200
         310   Gosub 4000
         320   If F = 1 then Goto 420
         360   V = #A060 :Gosub 1200
         365   @#8402 = 1 :@#8403 = 1
         366   PR "You can unload the units and wait"
         370   Gosub 7000
         415   Q = Q + 1
         420   until Q = 0
         430   Goto 100
-------------------------------------------------------------------------------------
         1200  For I = 0 to 7
         1210  @ (B) = I :@ (B + 1) = I :@ (B + 2) = 27 :Gosub 6500     Set routine
         1220  V = V + 1 :@ V = H :V = V + 1 :@ V = L                    for reading DUT
         1231  Next I
         1235  Return
```

```
2500   @#A300=0 :If E<T Goto 2650
2510   If E>T Goto 2800
2650   @#8404=1
2651   @#8404=0
2660   Gosub 3500 :J=R
2661   V=1
2662   If @#A300>50 Goto 9000 ------------------------------------------ Abort, excessive
2665   If J>(E+50) then Goto 2650                                        time to pressur-
2666   If J<(E+50) then Goto 2940                                        ize system alarm
2667   If J>(E+5) then Goto 2950                                         operator
2668   If J<(E-5) then Goto 2900
2680   Goto 3100
2700   @#8402=1 :Rem C VE
2701   @#8402=0 :Goto 2810                                               Pressure con-
2750   @#8403=1 :Rem F VE for PR                                         trol routine
2755   @#8403=0 :Goto 2810
-------------------------------------------------------------
2800   @#8400=1                                                          Apply pressure
2805   @#8400=0                                                          pulse
-------------------------------------------------------------
2810   Gosub 3500 :J=R
2812   If @#A300>50 then Goto 9000
2815   If J<(E-50) then Goto 2800
2816   If J>(E+50) then Goto 2700
2817   If J<(E-5) then Goto 2850
2820   If J>(E+5) then Goto 2750
2825   Goto 3100
2850   @#8401=1 :Rem F PR
2851   @#8401=0 :Goto 2810
2900   @#8403=1 :Rem F VE
2905   @#8403=0 :Goto 2660
2940   @#8401=1
2942   @#8401=0 :Goto 2660
2950   @#8405=1 :Rem F VA
2955   @#8405=0 :Goto 2660
3100   Return
-------------------------------------------------------------------------------------------
3500   @(B+2)=52 :@(B+2)=36 :@(B+3)=0
3510   If (STAT and #10)<>0 then Goto 3510
3515   H=@ (B+4) :L=@ (B+5) and #F                                       Read reference
3520   R=H*16+L                                                          unit and save
3522   @#A300=@A300+1                                                    data
3525   Return
-------------------------------------------------------------------------------------------
4000   E=E+1500 :Gosub 2500
4010   Return
4500   @#8402=1 :@#8403=1 :Gosub 4600
4510   Gosub 3500 :T=R
4520   @#8402=0 :@#8403=0
4530   Return
4600   For R=0 to 100 :Next R
4620   Return
6000   @ (B+2)=12 :@ (B+2)=28 :@ (B+2)=12 :@ (B+3)=0
6010   If (STAT and #10)<>0 then Goto 6010
6015   @ (B+2)=16
6020   H=@ (B+4) :L=@ (B+5) and #F
6025   R=H * 16+L :W=R
6030   Return
-------------------------------------------------------------------------------------------
6500   @ (B+2)=11
6501   @ (B+3)=0
```

```
          6505   If (STAT and #10)< >0 then Goto 6505                    Read DUT
          6510   @ (B+2)=16 :H=@ (B+4) :L=@ (B+5) and 15
          6520   Return
-------------------------------------------------------------------------------------
          7000   I=0
          7040   V=#A000 :Gosub 8000 :O=R
          7070   V=#A030 :Gosub 8000 :M=R
          7100   V=#A060 :Gosub 8000 :S=R
          7110   X=(S+O)/2 -M
          7120   P=(S+O)*10/90
          7121   If P=0 then P=1                                          Retrieve data
          7125   O=O/3                                                    and make cal-
          7130   X=(1000/P/3)*X/2                                         culations
          7150   G=9000 :Page=Page +1
          7160   I=I+1
          7170   If I<8 then Goto 7040
          7175   B=#8000 :Z=0
          7180   Return
-------------------------------------------------------------------------------------
          8000   V=V+2*I :V=V+1 :H=@V :V=V+1 :L=@V :R=H*16+L :R=R-W
          8050   Return
          9000   PR "Mechanical problem in the system"
          9200   PR "Check if one of the units is leaking!"
          9210   @#8402=1 :@#8403=1
          9220   F=1 :Goto 3100
          14000  For I=#A1A0 to #A1D0 :@ I=0 :Next I
          14010  End
-------------------------------------------------------------------------------------
          15000  PR "Offset Histogram - Unit in mV"
          15010  B=-150
          15020  For V=#A1A0 to #A1AF
          15030  PR "<", B, "=", @V
          15040  B=B+20 :Next V
          15050  PR "Sensitivity Histogram - Unit in 10X mV/psi"
          15060  B=1
          15070  For V=#A1B0 to #A1BF
          15080  PR "<", B, "=", @V
          15090  B=B+5 :Next V
          15100  PR "Linearity Histogram - Unit in 100X psi"
          15110  B=-75 :R=0
          15120  For V=#A1C0 to #A1CF                                     Print histogram
          15130  PR "<", B, "=", @V                                      data
          15140  B=B+10 :R=R+@V :Next V
          15150  PR "Total number of units tested =", R
          15160  End
          16000  B=#8000 :Gosub 3500
          16010  PR "Reference at vent =", R, "Counts"
          16020  G=10000 :Page=Page+1
-------------------------------------------------------------------------------------
Page N+1  1000   Goto G
          8000   V=V+2*I :V=V+1 :H=@V :V=V+1 :L=@V :R=H*16+L :R=R-W
          8010   Return
          9000   If Z=1 Goto 9300
          9010   L=0 :H=1 :R=0 :V=0 :J=O :C=#A1A0
          9015   B=-150 :S=20 :E=150
          9020   Gosub 20000
          9030   L=0 :H=1 :V=0 :R=0 :J=P :C=#A1B0
          9035   If J<0 then J=-1*J
          9040   B=1 :S=5 :E=76
          9050   Gosub 20000
          9060   L=0 :H=1 :V=0 :R=0 :J=X :C=#A1C0
```

```
9070    B = -75 :S = 10 :E = 75
9080    Gosub 20000
9100    Goto 13000
9200    K = 7160 :Page = Page - 1
9310    I = 7 :Goto 9200
10000   I = #A200
```

```
10100   PR "What do you want to do?"
10110   Input $I
10120   If @I = 71 then Goto 11000 :Rem Go
10130   If @I = 82 then Goto 11020 :Rem reference
10140   If @I = 84 then Goto 11010 :Rem test
10145   If @I = 80 then Gosub 15000 :Rem print
10150   If @I = 78 Goto 11030 :Rem new device
10155   Goto 10000
```

Entry to different test routines

```
11000   K = 117 :Page = Page - 1
11010   K = 125 :Z = 1 :Page = Page - 1
11020   K = 16000 :Page = Page - 1
11030   Q = 0 :K = 420 :Page = Page - 1
```

```
13000   If (O < A) or(O > Y) then Gosub 14000
13005   If P < 0 the P = -1 * P
13010   If (P < D) or (P > N) then Gosub 14050
13020   If (X < -U) or (X > U) then Gosub 14100
13030   Goto 9200
```

Test parametric data against limits

```
14000   @(#8406 + I) = 0
14010   PR "Rej", I + 1, "Off"
14020   Return
14050   @(#8406 + I) = 0
14060   PR "Rej", I + 1, "SEN"
14070   Return
14100   @(#8406 + I) = 0
14110   PR "Rej", I + 1, "LIN"
14120   Return
```

Activate go/no-go indicators and print failed parameter

```
15000   PR "          Offset          Sensitivity          Linearity"
15001   PR "          mV              10X mV/psi           100X psi"
15005   I = 0 :DO
15010   V = #A000 :Gosub 8000 :O = R
15020   V = #A030 :Gosub 8000 :M = R
15030   V = #A060 :Gosub 8000 :S = R
15040   X = (S + O)/2-M :P = (S - O)/9
15050   If P = 0 then P = 1
15060   O = O/3
15065   X = (1000/3) * X/P
15066   X = X/2
15070   I = I + 1
15080   PR Q - 1, "-", I," ",O," ",P," ",X
15095   Until I = 8
15100   Return
```

Print parametric data and device identification

```
20000   If J > B then Goto 20010
20005   @C = @C + 1 :Goto 20090
20010   DO
20020   If J > (B + L) then V = 1
20030   L = L + S
20040   If J < = (B + L) then R = 1
20050   If (V = 1) and (R = 1) then Gosub 21000
20060   V = 0 :R = 0 :H = H + 1
20070   Until H = 15
```

```
20080   If J > = E then @ (C + H) = @ (C + H) + 1
20090   Return
21000   @ (C + H) = @ (C + H) + 1
21010   H = 14
21020   Return
```

```
25000   PR "Device type to be tested?"
26010   PR "Type IE :SZ 34147, LX0603G etc"
25020   I = #A200 :Input $I                                   Part of
25030   PR "Enter offset low limit" :Input A :PR A            initialization
25040   PR "Enter offset high limit" :Input Y :PR Y
25050   PR "Enter sensitivity low limit" :Input D :PR D
25060   PR "Enter sensitivity high limit" :Input N :PR N
26010   PR "Enter high linearity limit" :Input U : PR U
27000   K = 115 :Page = Page – 1
```

Application of the ADC1210 CMOS A/D Converter

National Semiconductor
Application Note 245
James Wong
May 1980

Introduction

The ADC1210 is the answer to a need for analog to digital conversion in applications requiring low power, medium speed, or medium to high accuracy for low cost. The versatile input configurations allow many different input scale ranges and output logic formats.

The wide supply voltage range of 5V to 15V readily adapts the device to many applications. The very low power dissipation yields remarkable conversion linearity over the full operating temperature range. *Table I* below summarizes the typical performance of the ADC1210.

TABLE I
ADC1210 Performance Characteristics

Resolution	12 bits
Linearity Error, $T_A = 25°C$	±0.0122% FS MAX
Over Temperature	±0.0244% FS MAX
Full Scale Error, $T_A = 25°C$	0.1% FS MAX
Zero Scale Error, $T_A = 25°C$	0.1% FS MAX
Quantization Error	±½ LSB MAX
Conversion Time	200 μs MAX

This note expands the scope of application configurations and techniques beyond those shown in the data sheet. The first section discusses the theory of operation. The remaining sections are devoted to applications that extract the optimum potential from the ADC1210.

Theory of Operation

Like most successive approximation A to D's, the ADC1210 consists of a successive approximation register (SAR), a D to A converter, and a comparator to test the SAR's output against the unknown analog input. In the case of the ADC1210, these elements are connected to allow unusual versatility in matching performance to the user's applications.

The SAR is a specialized shift register programmed such that a start pulse applies a logical low to the most significant bit (MSB) and logical highs to all other bits, thus applying a half scale digital signal to the DAC. If the comparator finds that the unknown analog input is below half scale, the low is shifted to the second bit to test for quarter scale. If, on the other hand, the comparator finds that the analog input is above half scale, the "low" state is not only shifted to the second bit, but also retained in the MSB, thus forming the digital code for three quarters scale. Upon completing the quarter (or three-quarter) scale test, the next clock pulse sets the SAR to test either ⅛, ⅜, ⅝, or ⅞ full scale, depending on the input and the previous decisions. This successive half-the-previous-scale approximation sequence continues for the remaining lower order bits. The thirteenth clock pulse shifts the test bit off the end of the working register and into the conversion complete output. *Figure 1* shows the schematic diagram of the device.

Operating Configurations

Figures 2 through *5* show four operating configurations in addition to those presented in the data sheet.

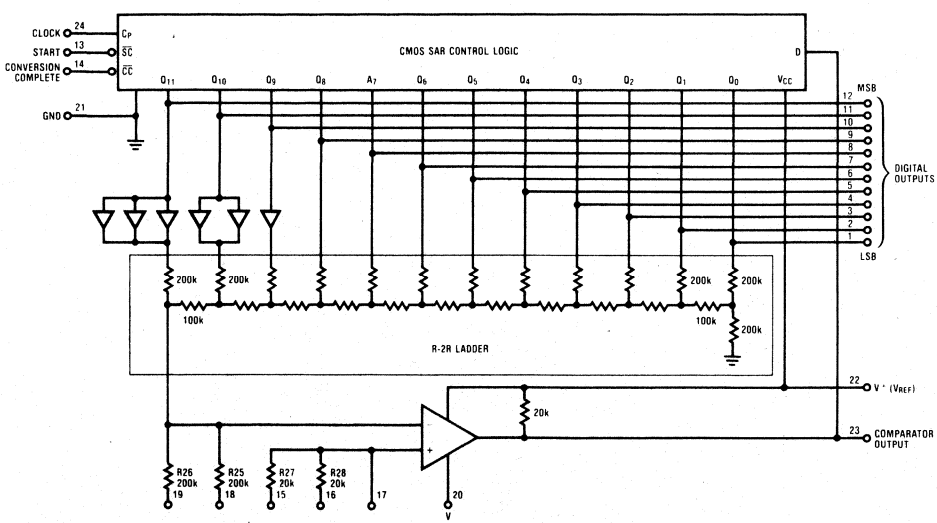


Figure 1. Schematic Drawing

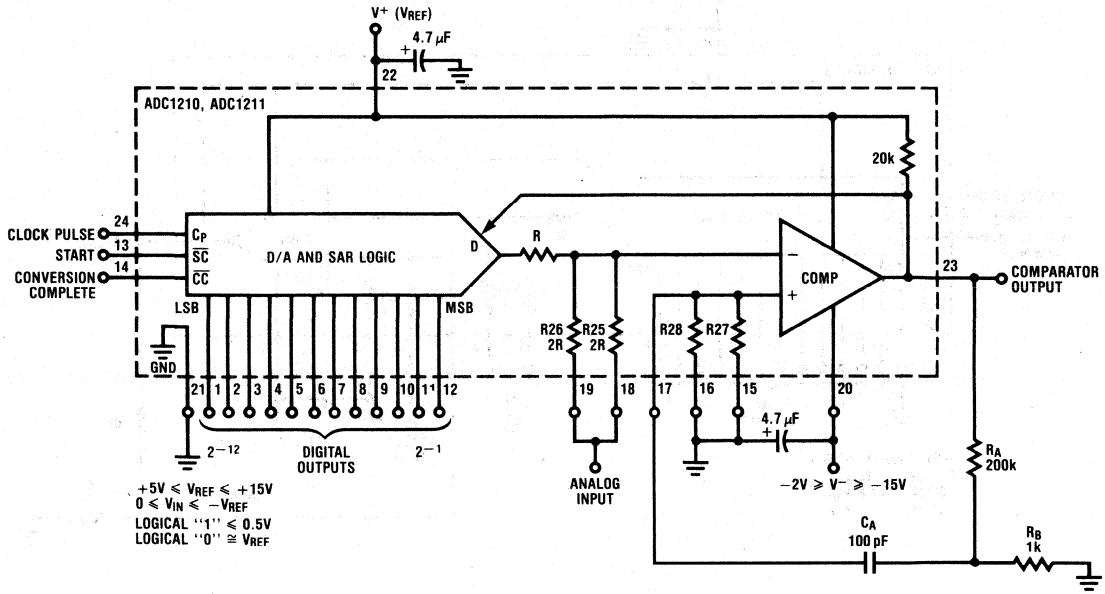


Figure 2. Complementary Logic, 0V to $-V_{REF}$ Input

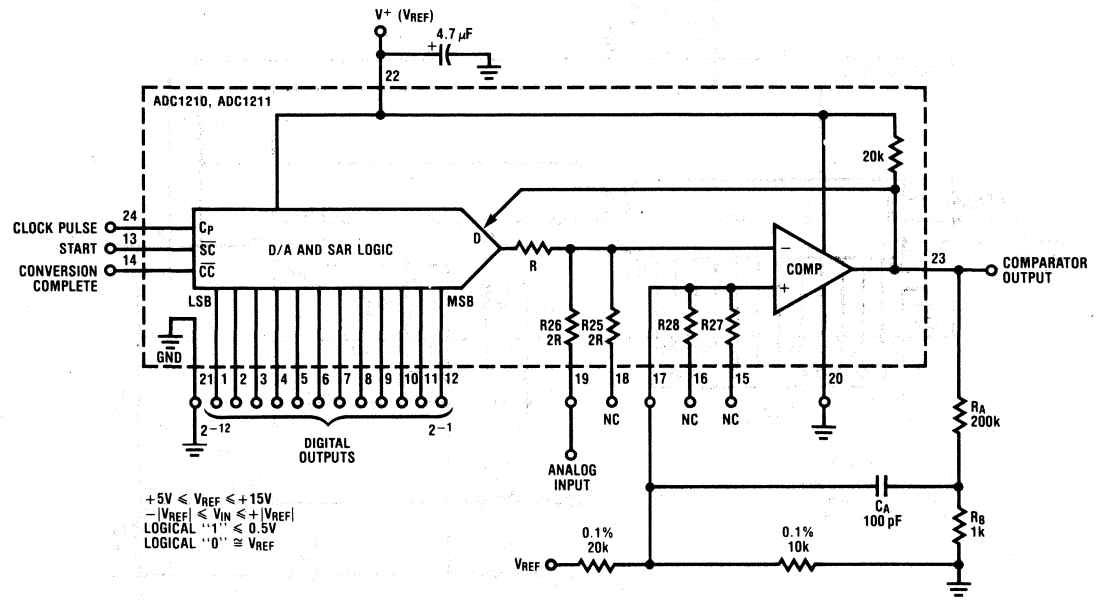


Figure 3. Complementary Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

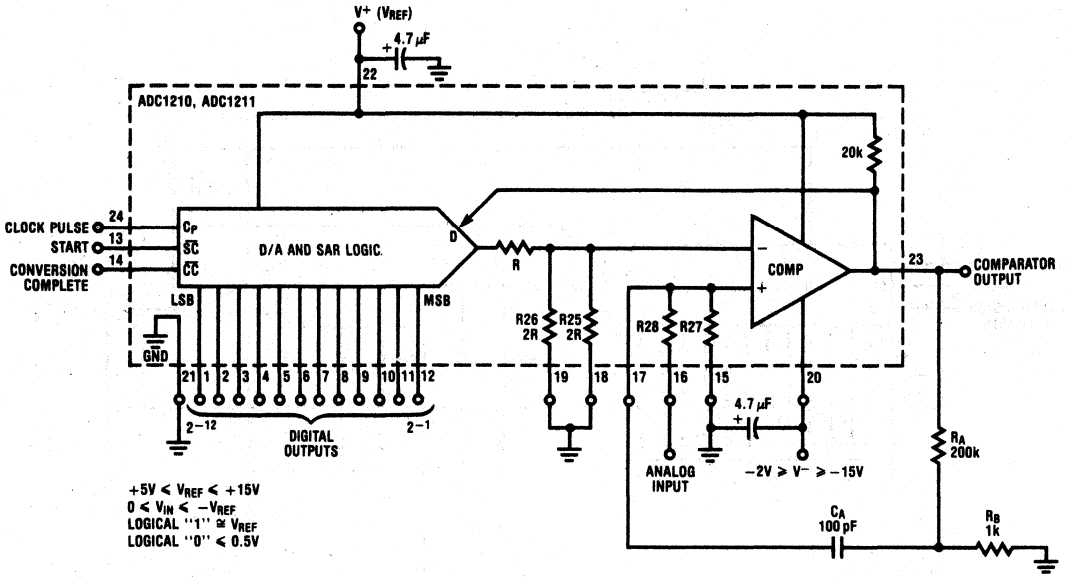


Figure 4. Positive True Logic, 0V to $+V_{REF}$ Input

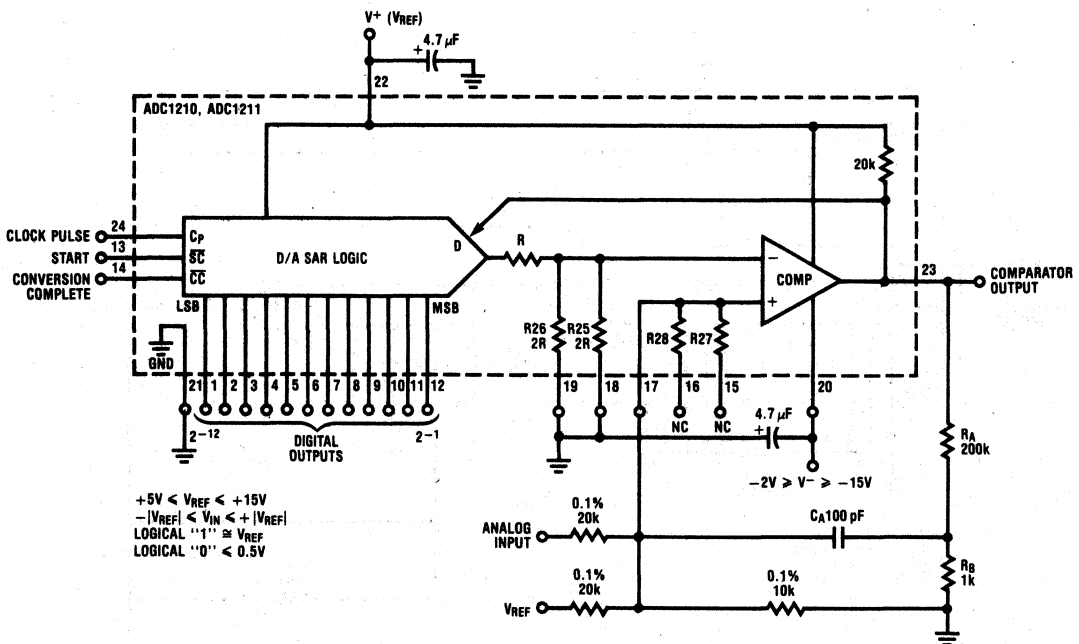


Figure 5. Positive True Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

Design Considerations

To Complement, or Not to Complement

Of the two recommended logic configurations, the complementary version is preferred. It provides greater accuracy than the straight binary version. The reason for that is that with the complementary logic configuration, a reference voltage is fixed at the non-inverting input of the comparator. Consequently, the comparator operates at this fixed threshold independent of the input voltage. For the straight binary configuration, the analog input drives the non-inverting input of the comparator so that the common mode voltage on the comparator input varies with the analog input. This adds a non-linear offset voltage of less than ¼ LSB.

Regardless which configuration is used, the comparator input common mode range must net be exceeded. In fact, the voltage at either comparator input must be no less than 0.5 volts from the negative supply and 2.0 volts from the positive supply. Therefore, for applications requiring common mode range to ground, simply connect a negative supply (−2V to −15V) to pin 20.

Layout Considerations

High resolution D/A and A/D converter circuits may have their entire error budget blown if any digital noise is allowed to enter the analog circuit.

Exercising care in the layout is certain to minimize frustrations. Single point analog grounding is a good place to start. All analog ground connections and supply bypassing should be returned to this point. In fact, in critical applications, the ADC1210 GND pin should be made "the" reference node. Furthermore, one should separate the analog ground from the digital ground. Any excursion of switching spikes generated in the digital circuit is, to some degree, decoupled from the analog circuitries. *Figure 6* illustrates this. Of course, these two points are eventually tied together at the power supply/chassis common.

In addition to a good ground system, it is a good idea to keep digital signal traces as far apart from the analog input as is practical in order to avoid signal cross coupling.

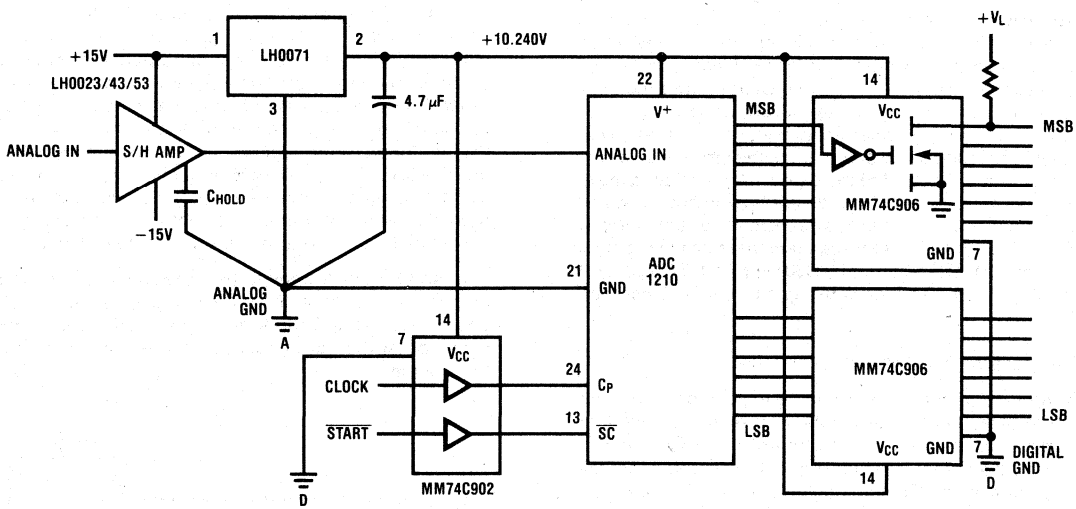


Figure 6. Grounding Considerations of Interface Circuits

Power Supply Bypassing

The supply input not only provides power to the digital logic, it is also a reference voltage to the resistor ladder network of the ADC1210. This voltage must be a very stable source. A precision reference device such as the LH0070 or LH0071 is ideal for the ADC1210. However, the internal CMOS Successive Approximation Register (SAR) invariably generates current spikes (10-20 mA peak) in the supply pin as the logic circuit switches pass the linear region. Consequently, if a reference device such as the LH0070 is used, the current spike tends to cause excursions in the reference voltage, thus threatening conversion accuracy. To preserve the 12-bit accuracy, bypass the supply pin with a 4.7 μF tantalum capacitor. In high noise environments, a 22 μF capacitor shunted by a 0.1 μF ceramic disc capacitor is desirable.

If pin 20 is connected to a negative supply, it too should be bypassed to prevent voltage fluctuations from affecting the comparator operation.

Output Drive Capability

The digital outputs of the ADC1210 and the outputs of the SAR, through which the resistor ladder is referenced, are one and the same. Any excessive load current on the digital outpt lines will degrade conversion accuracy. For this reason, the ADC1210 must interface with CMOS logic. However, the three most significant bits (pins 10, 11, and 12) are buffered from the R-2R ladder and are capable of driving light loads without degrading linearity. This could prove useful in 2's complement applications where an inverter is necessary in the MSB; one might construct this inverter with a discrete NPN transistor and two resistors. The bit most sensitive to output loading is the fourth most significant (pin 9). An error voltage at this pin gets divided down by a factor of 16 before being applied to the comparator, so if we wish to limit the error due to output loading to say, ½ LSB, or 1.25 mV at the comparator, we can tolerate 20 mV at pin 9. If all lower bits will have the same output load, the error must be limited to 10 mV. Since all of the digital outputs have a maximum ON resistance of 350Ω at 10V V_{REF} in both high and low states, the maximum allowable load current is 10 mV/350Ω = 29 μA. This current requirement is easily satisfied with an MM74C914 or MM74C901 thru MM74C902 level translators for interface with logic levels different than V_{REF}.

Comparator Hysteresis

Even an ideal comparator can be expected to oscillate due to stray capacitive feedback if biased in the linar region. It is the normal operation of the SAR feedback loop to do just that . . . at least at or toward the end of the conversion cycle. For most applications, this oscillation is only a minor bother, as the SAR register would have locked out the converted data from further changes at the end of conversion. If that is still undesirable, the Conversion Complete ($\overline{CC}$) Signal may be used to drive an open-collector gate (such as the MM74C906) with the output wire-ORed to the comparator output. In this way, the comparator is always clamped to the low state at the end of conversion. Normal operation resumes upon restart of a new conversion cycle.

In normal operation, however, if we want to preserve 12-bit accurcy, the comparator oscillation should be suppressed. The recommended technique is to apply a slight amount of AC hysteresis (50 mV) at the beginning of the decision cycle, but let it decay away to an acceptable accuracy before the decision is actually recorded in the SAR. The approximate decay time is (5) × (10k + 1k) × (100 pF), or 5.5 microseconds (see *Figure 2*).

For those applications using supply voltage other than 10V, say 5V, and if 50 mV initial hysteresis is to be maintained, the 200 kΩ (R_A) resistor in *Figure 2* should be changed to 100 kΩ based on the relationship:

$$\frac{R_B}{R_A + R_B} V_{REF} = 50\,mV$$

Where: $R_B = 1\,k\Omega$

High Speed Conversion Technique

By using one IC, one discrete NPN transistor, and a resistor, the ADC1210 can be made to run at up to 500 kHz clock frequency, or 12-bit conversion time of 26 μs. The circuit is shown in *Figure 7*. The idea is to clamp the comparator output low until the SAR is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions. This technique eliminates the need for the AC hysteresis circuit.

To implement the idea, a complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The inverted clock, generated from the same clock signal, is inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in working order. During the last half cycle, the comparator output is unclamped. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propagation delay such that the comparator output data is held long enough to resolve any internal logic set-up time requirements.

The 500 kHz clock implies that the absolute minimum amount of time required for the comparator output to be unclamped is 1 μs. Therefore, for applications with clock signal other than 50% duty cycle, this 1 μs period must be observed.

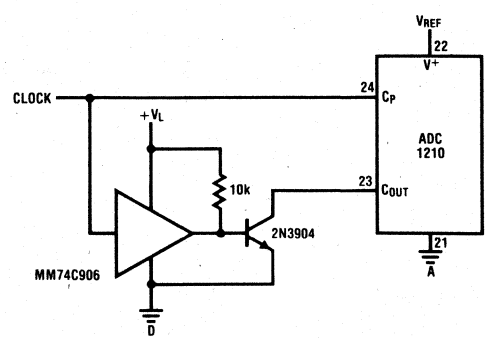


Figure 7. High Speed Conversion Circuit

Testing has demonstrated reliable performance from this circuit beyond the recommended device operating frequency of 65 kHz. However, the AC hysteresis circuit is still a very reliable technique below this clock frequency and, therefore, should be used. Only in applications where the required clock frequency is above 65 kHz should the above-mentioned technique be adopted.

Synchronizing Conversion Start Signal

It is recommended that the $\overline{\text{START CONVERT}}$ input be synchronized to the CLOCK input. This avoids the possibility of the comparator making an error on the first (MSB) decision when the analog input is near ½ scale. There is a chance that energy can be coupled to the comparator from the rising edge of the $\overline{\text{START}}$ signal. If this occurs just before the rising edge of the clock, a wrong MSB decision can be made if time is not allowed for the charge to dissipate. The synchronization circuit in *Figure 8* effectively prevents this from occurring.

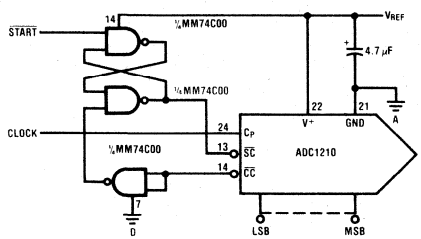


Figure 8. Synchronizing START CONVERT Signal

The circuit operates as follows: initially the latch is in the RESET state and the converter is in the end-of-conversion state ($\overline{\text{CC}}$ output at logic low). The $\overline{\text{START}}$ signal sets the latch and, on the next positive clock transition, initializes all internal registers in the converter. The $\overline{\text{CC}}$ output is set to logic high, presetting the external latch. The latch is held in the "RESET" state during the entire conversion period, effectively preventing a new $\overline{\text{START}}$ signal from interrupting the conversion.

Serial Output

The comparator output does contain the stream of serially converted data with the most significant bit first. However, recognizing the danger of comparator oscillation, there is a potential for the external serial data register to latch a data bit different from that recorded in the SAR due to different logic set-up time requirements. If the ADC1210 accepts an error in any one data bit, the subsequent lower order bits tend to correct for it. On the other hand, an external serial register has no provision for error correction. All subsequent bits following a bit in error will not be valid data.

The 12 bits of information can be shifted out serially by using an MM74C150 digital multiplexer. The circuit is shown in *Figure 9*. This scheme permits valid data to be available at the serial output port as fast as half a clock cycle after the most current decision. The data are thus synchronized to the converter clock (here the serial data are synchronized at the falling edge of the system, CLOCK to avoid clock skew). Obviously, a number of variations can be made to this basic circuit for use with different handshake protocols.

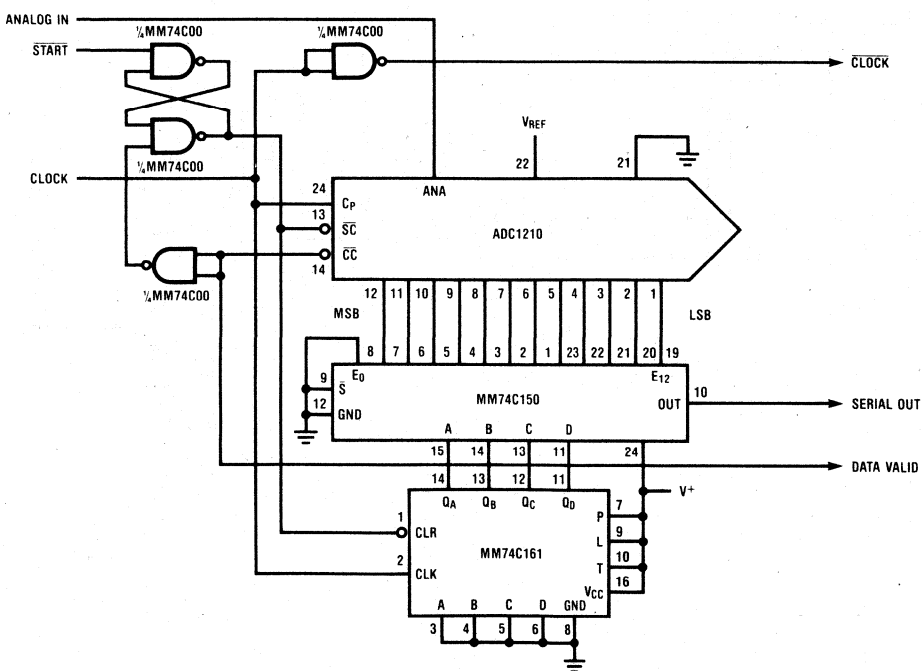


Figure 9. 12-Bit A/D Converter with Serial Output

Applications

Long Time Sample and Hold

The circuit in *Figure 10* is a particularly simple realization of an infinite sample and hold. This scheme requires two low-cost analog sample-and-hold amplifiers to complete the circuit.

The idea is to utilize the digital-loop feedback mechanism of the ADC1210 which, in the normal conversion mode, replicates the analog input voltage at the output of the SAR/D-to-A converter.

The operation of the circuit may be described as follows: During the normal "hold" mode, the replicated analog voltage is buffered straight through the S/H amplifier to the output. Upon an issuance of a $\overline{\text{SAMPLE}}$ signal, this S/H amplifier is placed in the hold mode, holding the voltage until the new analog voltage is valid. The same $\overline{\text{SAMPLE}}$ signal triggers an update to the input sample-and-hold amplifier. The most current analog voltage is captured and held for conversion. This way, the previously determined voltage is held stable at the output during the conversion cycle while the SAR/D-to-A continuously adjust to replicate the new input voltage. At the end of the conversion, the output sample-and-hold amplifier is once again placed in the track mode. The new analog voltage is then regenerated.

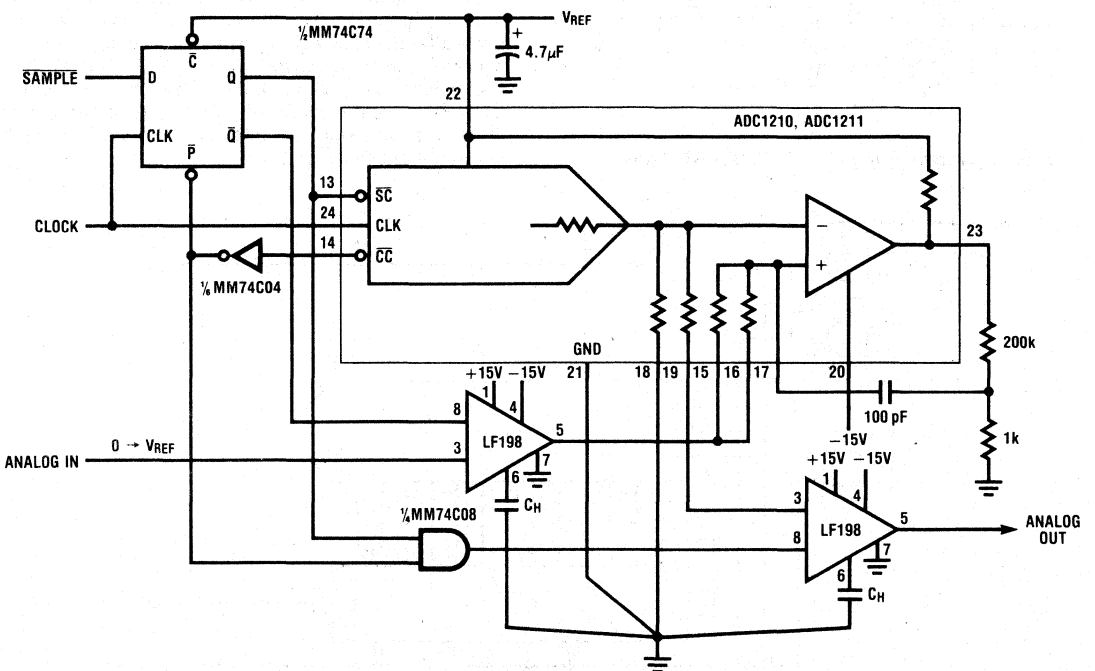


Figure 10. Infinite Sample and Hold Amplifer

An Auto-Ranging Gain-Programmed A/D Converter

The circuit in *Figure 11* shows one possible circuit of an auto-ranging A/D converter. The circuit has a total of 8 gain ranges, with the ranging done in the LH0086 Programmable Gain Amplifier (for differential input, use the LH0084 with ranges of 1, 2, 5, 10 digitally programmed, or pin strap programmed for multiplying factors of 1, 4, and 10). The gain ranges are: 1, 2, 5, 10, 20, 50, 100, and 200. It effectively improves the A/D *resolution* from 12 bits to an equivalent of 19 bits, a dynamic range of better than 100dB.

The circuit has relatively high speed ranging due to the very fast settling time of the LH0086, typically 5μs for 10V swing, well within the 15μs converter clock period. Thus, the ranging circuit is designed to work off the same clock.

The circuit is designed such that the auto-ranging function is transparent to the user. All command signals into and out of the system are identical to those of an ADC1210 operating alone. The only exception is that the system requires one and one-half clock cycle (mandatory auto range cycle), plus however many ranges it has to scale to (each scale requires one clock period, 7 possible range switching in all) in addition to the basic 13 conversion cycle required by the ADC1210. Therefore, in the best case where no ranging is necessary, the circuit adds 22.5μs to the conversion time; and in the worst case, an additional 128μs.

In the quiescent state where the ADC1210 is in the non-conversion mode, the auto-ranging circuit is free to function normally. Upon an issuance of a $\overline{\text{START}}$ signal, the next clock rising edge puts the circuit in the final auto range cycle before conversion begins. If the need for up-range or down-range is detected, the circuit remains in the auto range mode until all necessary scaling is completed. The control circuit then issues a start conversion signal to the ADC1210. Half a clock cycle later, the ADC1210 begins conversion and suspends the auto-ranging operation until the conversion is completed. At which time the 12-bit converter data plus the 3-bit range data are valid for further processing.

This design is suitable for applications in data-acquisition systems or portable instruments, particularly where low power is an important consideration. Other variations from this basic scheme can be realized depending on the user's requirements.

Summary

The ADC1210 is a low-cost, medium-speed CMOS analog-to-digital converter with 12-bit resolution and linearity. It has wide supply range and flexible configuration to allow varied applications such as field instruments and sampled data systems.

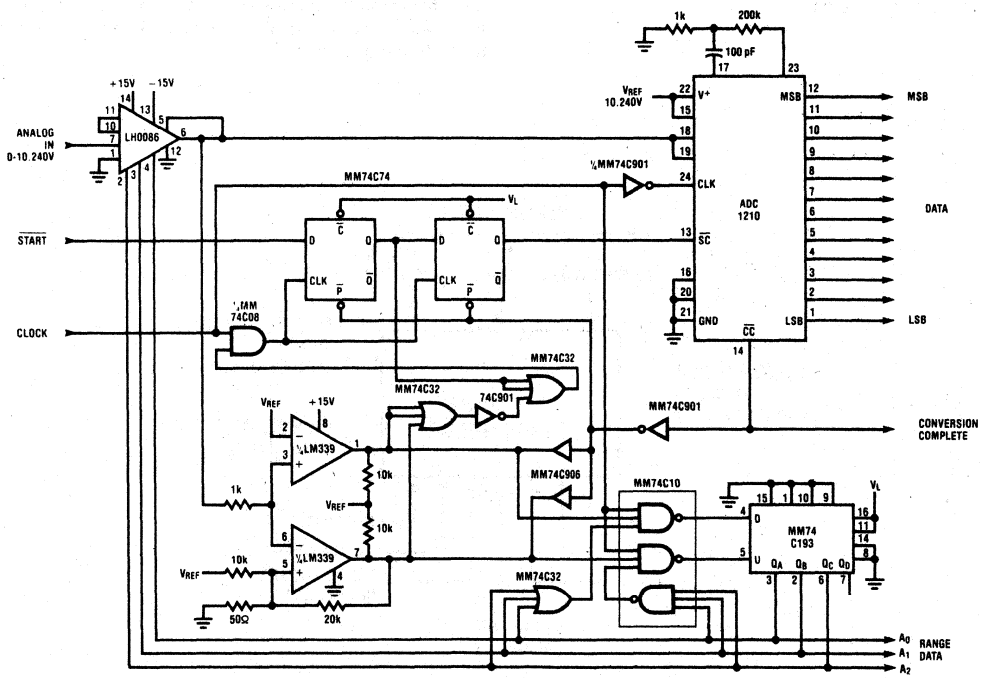


Figure 11. Auto Gain Ranging A/D Converter

Pressure Transducer Accuracy and Specifications

National Semiconductor
Application Note 246
Ray Pitts
Art Zias
May 1980

PRELIMINARY

PRESSURE TRANSDUCER ERROR ANALYSIS

Specified pressure transducer error parameters are measured under well-defined user conditions and related to system performance. With these parameters and a few simple formulas, the user can easily calculate accuracy for any given set of conditions. The formulas and concepts presented herein can also be extended for use with complete pressure systems.

A System Model

To see how transducer performance parameters are related to system accuracy, consider the IC pressure transducer system shown in *Figure 1*. The problem is to determine the magnitude of error for given values of the *major input* (applied pressure) and the *minor inputs* (temperature, time and supply voltage). The *error sources* are inherent to the transducer, but the magnitude of error from each one may depend on the major and minor inputs to the transducer system.

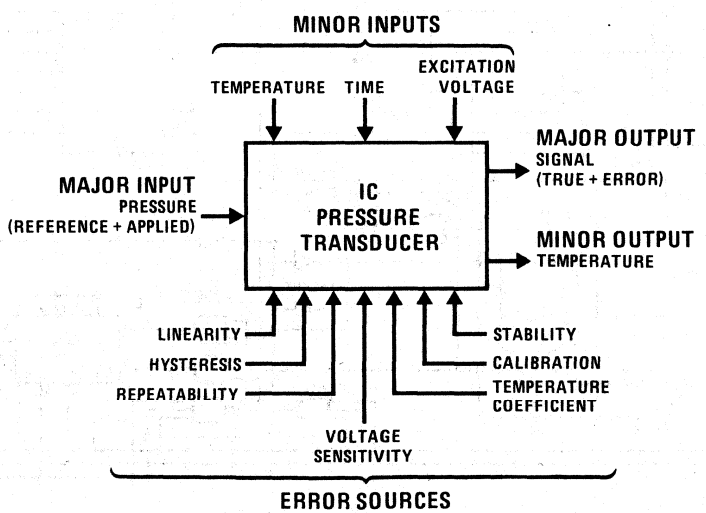


FIGURE 1

To simplify our model, we first divide the error sources into 2 groups: those that are dependent on applied pressure and those that are not. The inherent linearity (and careful design) of National's hybrid IC transducers allows us to do this very simply. As shown in *Figure 2*, the response is fitted to a *best straight line* (BSL) that intersects the true response at the reference pressure. This is called a *BSL with forced reference.* As a result, the output signal V_S is given by:

$$\Delta V_S = V_O + S \bullet P$$

where V_O is the offset voltage (obtained at reference pressure), S is the sensitivity and P is the applied pressure. As a further result, the error in output signal ΔV_S can be expressed as:

$$\Delta V_S = \Delta V_O + s \bullet P$$

where ΔV_O is the *offset* error, which is independent of applied pressure; and s•P is the *span* error, which is proportional to applied pressure, with s as the span error coefficient.

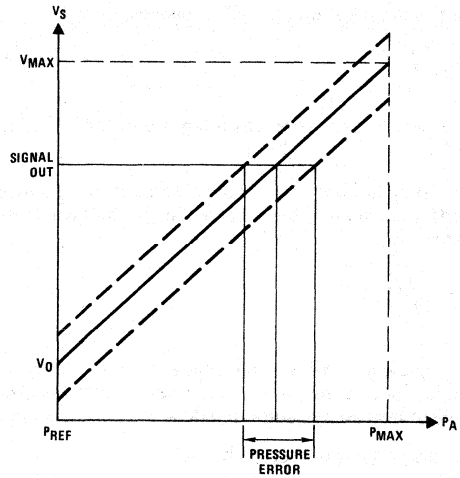


FIGURE 3

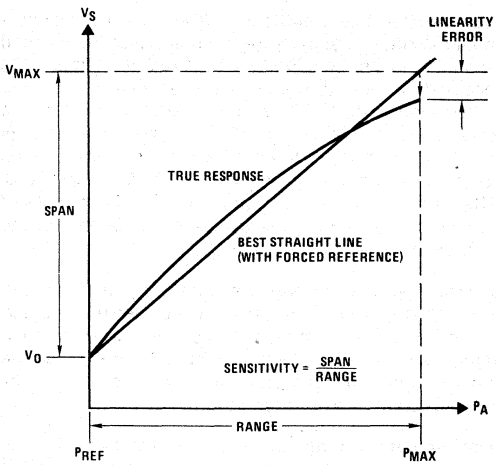


FIGURE 2

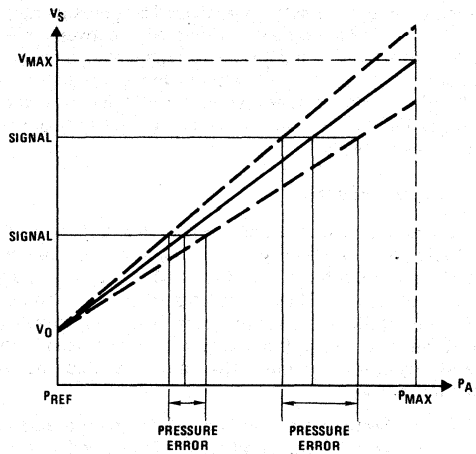


FIGURE 4

The *offset* errors, being independent of the major input variable (applied pressure), are equivalent to system *common-mode* errors, as shown in *Figure 3*. Because the offset error is the same regardless of pressure, it has the effect of translating the response line up or down, while the slope or sensitivity remains constant.

The *span* errors, being proportional to applied pressure, are equivalent to system *normal mode* error, as shown in *Figure 4*. Because the span error increases linearly with applied pressure, it has the effect of rotating the reponse line around the offset-reference pressure point.

While mutually independent, the *offset* and *span* error groups both contain errors that are dependent on the minor input variables. As shown in Table I, each group includes a temperature coefficient, a supply voltage coefficient and 3 time-dependent coefficients. These coefficients are used to specify the errors in National's hybrid IC pressure transducers and to calculate overall accuracy.

TABLE I. OFFSET AND SPAN ERRORS

OFFSET (Common-Mode)	SPAN (Normal Mode)
Calibration	Calibration
Repeatability	Linearity-Hysteresis-Repeatability
Stability	Stability
Temperature Coefficient	Temperature Coefficient
Voltage Coefficient	Voltage Coefficient

System Accuracy

With the errors divided into 2 groups of mutually independent coefficients defined by their dependence (or non-dependence) on the system input variables, we can now compute either the worst-case error or the most probable error for any IC pressure transducer system.

Worst-Case Error: The worst-case overall error $\in_{WC}$ is obtained by simple addition of all applicable errors:

$$\in_{WC} = \sum_{1}^{n} \in_x$$

where $\in_x$ is the error resulting from the x^{th} error coefficient.

Most Probable Error: The most probable error $\in_{MP}$ is obtained by computing the square root of the sum of the squares:

$$\in_{MP} = \sqrt{\sum_{1}^{n} \in_x^2}$$

We can now select the applicable error coefficients and evaluate the error terms $\in_x$ from the specifications given for any individual pressure transducer.

ACCURACY SPECIFICATIONS

By convention, system accuracy is calculated in terms of the major input variable, in this case, applied pressure. In line with this convention, each transducer coefficient is measured in psi or psi/°C then divided by pressure range to express error in percent of range. This convention excludes sensitivity to excitation voltage which is given in percent signal change per applied voltage change; and calibration, which is specified in V or mV/psi and can be converted to %FS or %S by dividing by full span or sensitivity respectively.

Offset Specifications

The offset characteristics are measured at 25°C with 15V excitation and reference pressure applied. The reference pressure is 0 psi for all but the LX0503A, LX1601A and LX1801AN(Z), which have a 15 psia reference. Although measured at the reference pressure, the offset errors are the same regardless of pressure and can be used in the overall accuracy formulas. They are measured and defined as follows.

Offset Calibration: Defines the offset voltage and its maximum deviation from unit to unit, including long-term stability (1 year shelf, 1000 hours operating). The deviation is measured and specified in volts and must be divided by full span (nominally 10V) to express the error band as %FS for accuracy calculations.

Offset Temperature Coefficient (TC_O): Defines the maximum deviation in offset voltage as the temperature is varied from 25°C to any other temperature between 0°C and +85°C. It is specified as %FS/°C and must be multiplied by the temperature difference to obtain the error as %FS. The maximum error is (85°C-25°C)•TC_O = (60°C)•TC_O.

Offset Repeatability: Defines the maximum deviation in offset voltage when applied pressure is cycled through its full range 50 times in a 1 minute period. The measured offset voltage deviation is divided by sensitivity to express the error in units of pressure. That error is divided by (P_{MAX}-P_{MIN}) to be expressed as %FS.

Offset Stability: Defines the maximum deviation in offset voltage after up to 1 year shelf, over a 1000 hour period during which the pressure and temperature are cycled over their specified operating ranges with power applied. The stability is the same whether or not the transducer is operating. The measured offset voltage deviation is divided by sensitivity to express the error in units of pressure. That error is divided by (P_{MAX}-P_{MIN}) to be expressed as %FS.

Span Specifications

The span characteristics are measured at 25°C with 15V excitation and with the applied pressure set first at maximum, then at reference to obtain the span voltage. Since the span errors are proportional to pressure they are specified as percent of applied pressure, or %S. To determine the span error in units of pressure at any intermediate pressure P, multiply %S by |(P-P_{REF})|. The span errors are measured and specified as follows.

Sensitivity Calibration: Defines the slope of the best straight line fitted to the response curve with forced reference at the reference pressure output voltage, with the sensitivity deviation from unit to unit, including long-term stability (1 year shelf, 1000 hours operating). The deviation is measured in mV/psi and must be divided by the sensitivity to express the error as %S.

Span Temperature Coefficient (TC_S): Defines the maximum deviation in span voltage as temperature is varied from 25°C to any temperature from 0°C to +85°C. It is specified for any (P-P_{REF}) in the specified operating pressure range as %S/°C and must be multiplied by the temperature difference, |T-25°C| to obtain the error as %S. The maximum error expressed as %S over the full operating temperature range is (85°C-25°C)•TC_S = (60°C)•TC_S. The maximum span temperature error in units of pressure occurs at P_{MAX} and is determined by multiplying the maximum %S by |(P_{MAX}-P_{REF})|.

Linearity-Hysteresis-Span Repeatability: Defines the deviation in span when the pressure is cycled from P_{REF} to P_{MAX} 50 times in a 1 minute period. The measured span voltage deviation is divided by sensitivity to express the error in units of pressure. That error is divided by (P_{MAX}-P_{REF}) to be expressed as %S.

Span Stability: Defines the maximum deviation in span voltage after up to 1 year shelf, over a 1000 hour period during which the pressure and temperature are cycled over their specified operating ranges with power applied. The span stability is the same whether or not the transducer is operating. The measured span voltage deviation is divided by sensitivity to express the error in units of pressure. That error is divided by (P_{MAX}-P_{REF}) to be expressed as %S.

BASIC ACCURACY CALCULATIONS

Voltage Regulation

In the calculations that follow, we will assume that excitation voltage is sufficiently regulated so as to keep the voltage within the specified allowed limits. For hybrids, the built-in regulation required to satisfy this condition is derived as follows. The voltage error $\in_{VR}$ resulting from output sensitivity to excitation voltage is given by:

$$\in_{VR} = 0.5\% \bullet \Delta V_e$$

where 0.5% is the specified sensitivity to excitation voltage and ΔV_e is the excitation voltage deviation [from nominal (15V)]. For example, to keep the regulation error

below 0.1%FS the required external power supply regulation is given by:

$$\frac{\Delta V_e}{V_e} = \left(\frac{1}{0.5\%}\right) \cdot \left(\frac{\in_{VR}}{V_e}\right) = 200 \cdot \left(\frac{\in_{VR}}{\text{Span}}\right) \cdot \left(\frac{\text{Span}}{V_e}\right)$$

$$\frac{\in_{VR}}{\text{Span}} = 0.1\%$$

$$\frac{\Delta V_e}{V_e} = 20\% \cdot \left(\frac{\text{Span}}{V_e}\right)$$

For Span = 10V and V_e = 15V,

$$\frac{\Delta V_e}{V_e} = 20\% \cdot \left(\frac{2}{3}\right) = \pm 13\% \text{ Regulation}$$

which holds for any hybrid pressure transducer. This degree of voltage regulation essentially eliminates excitation voltage error in all but ultra-high accuracy applications, as long as excitation voltage is kept within allowed limits.

%-to-psi Conversion

Specification in percent error allows easy evaluation of transducer error parameters. But for easy system accuracy computations, percent error is normally converted to psi error.

Span errors are proportional to applied pressure and specified as %S, percent of span. The span error in psi is given by:

$$\text{Span Error} = (\%S) \cdot |P - P_{REF}|$$

where $|P - P_{REF}|$ is the absolute value of applied pressure P relative to the offset reference pressure, P_{REF}. This produces error bands as shown in *Figure 5.* Note that at the reference pressure, span errors are null, and the only errors are in offset.

Offset errors are independent of pressure and given as %FS, where FS is full span voltage or maximum specified operating pressure range. The offset error in psi is given by:

$$\text{Offset Error} = (\%FS) \cdot |P_{MAX} - P_{MIN}|$$

For example, the pressure range of the LX1604G is ± 15 psig, or 30 psig full span, and the specified offset stability is ± 1.7%FS. The error in psi is therefore:

$$\text{Offset Stability} = 1.7\% \cdot 30 \text{ psi} = \pm 0.5 \text{ psi}$$

Since offset errors are independent of applied pressure they can be fully or partially "calibrated out" by manual referencing or autoreferencing at any known pressure, most commonly at the specified offset reference pressure. For a full discussion of autoreferencing, see Section 7 of the 1977 Pressure Transducer Handbook.

SYSTEM ACCURACY CALCULATIONS

To show how the specifications apply for various use conditions, calculations are performed for a typical absolute pressure transducer, the LX1610A, with specifications given in Table II. Analogous procedures will apply to any National IC pressure transducer, and can be extended for use in evaluating errors in a complete pressure system.

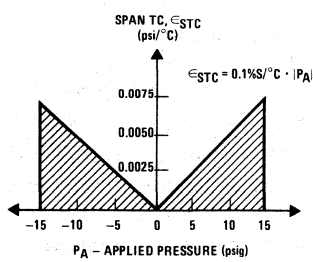
Referring to Table II, the specified % errors are first converted to psi then to *maximum error* (at T_{MAX} or 85°C for offset, at T_{MAX} and P_{MAX} for span); and the calibration tolerances are divided by the sensitivity. This converts the offset calibration error to psi, but the span calibration error must also be multiplied by P_{MAX}. The resulting errors, listed in the third row, are the maximum errors that can occur for each of the listed parameters. The span error at any pressure P can be obtained by multiplying these maximum span errors by P/P_{MAX}. The fourth row lists the maximum errors that can occur at T_{REF} or 25°C. These are the same for all except TC_O and TC_S, which are both zero at T_{REF}. The fifth row under *span* shows the error at P_{REF}, which is zero for all span errors.

Calibrated vs Interchangeable Accuracy

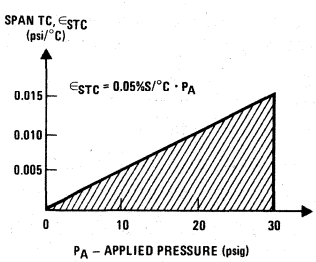
In calculating overall accuracy, the first question is whether each pressure transducer will be field calibrated upon installation or replacement. If so, you will want to use the *calibrated accuracy,* which holds only for one specific transducer. The calibrated overall accuracy excludes National's calibration errors but includes all other applicable specified errors.

Calibrated Accuracy: $\in_C$ includes stability, TC, linearity and hysteresis, and repeatability. But if you're going to just plug it in with no adjustments, you'll need the *interchangeable accuracy,* which allows for unit-to-unit calibration errors. In this case you include National's calibration errors but exclude stability error (the specified calibration error includes both calibration and stability errors).

Interchangeable Accuracy: $\in_I$ includes calibration, TC, linearity and hysteresis, and repeatability; where $\in_I$ is the overall error allowing for direct exchange of transducers of the same type, with the same operating conditions.



a. LX1604G Transducer



b. LX1603G Transducer

FIGURE 5. Span Temperature Coefficients: Error Bands for LX1604G (± 15 psig) and LX1603G (0 to 30 psig) Devices

TABLE II. LX1610A ABSOLUTE PRESSURE TRANSDUCER SPECIFICATIONS

Operating Parameters		General Noise Parameters	
Excitation Voltage	15V	Output Sensitivity to Excitation	0.5% V_e
Output Voltage Span	10V	Electrical Noise ($0 \le f \le 1$ kHz)	0.04%FS
Pressure Range	0 to 60 psia		
Temperature Range	0°C to +85°C		

OFFSET ERRORS

Coefficient	Calibration	Temperature Coefficient (25°C Ref)	Repeatability	Stability
Specified Error	2.5 ±0.30V	±0.04%/°C	0.4%FS	±1.5%FS
Error in psi	±1.8 psia	±0.024 psia/°C	±0.24 psia	±0.9 psia
Maximum Error (at 85°C)	±1.8 psia	±1.44 psia	±0.24 psia	±0.9 psia
Error at 25°C	±1.8 psia	0	±0.24 psia	±0.9 psia

SPAN ERRORS

Coefficient	Sensitivity Calibration	Temperature Coefficient (25°C Ref)	Repeatability	Stability
Specified Error	167 ±3.3 mV/psia	±0.05%/°C	±0.67%S	±0.3%S
Error in psi	+1.2 psia	±0.03 psia/°C	±0.4 psia	±0.24 psia
Maximum Error (85°C, P_{MAX})	±1.2 psia	±1.8 psia	±0.4 psia	±0.24 psia
Error at 25°C	±1.2 psia	0	±0.4 psia	±0.24 psia
Error at P_{REF}	0	0	0	0

Of course, either of these errors can be calculated as worst-case (simple linear addition) or most probable errors. To keep it simple, we will work mainly with worst-case error, remembering that the most probable error is always smaller and easily calculable via the square root of the sum of the squares.

Maximum Error

Referring again to Table II, the maximum possible error occurs at T_{MAX} with P_{MAX} applied. Under these conditions, the *calibrated overall error* $\in_C$ is:

$$\in_C = \underbrace{(1.44 + 0.24 + 0.9)}_{\text{Offset}} + \underbrace{(1.8 + 0.4 + 0.24)}_{\text{Span}}$$

Worst-Case: $\in_{WCC} = 2.58 + 2.44 = \pm 5.02$ psia

Most Probable: $\in_{MPC} = \sqrt{2.94 + 3.46} = \pm 2.53$ psia

which represent, respectively, ±8.4%FS and ±4.2%FS. The corresponding *interchangeable overall error* is:

$$\in_I = \underbrace{(1.8 + 1.44 + 0.24)}_{\text{Offset}} + \underbrace{(1.2 + 1.8 + 0.4)}_{\text{Span}}$$

Worst-Case: $\in_{WCI} = 3.48 + 3.4 = \pm 6.88$ psia

Most Probable: $\in_{MPI} = \sqrt{5.37 + 4.84} = \pm 3.20$ psia

which represent, respectively, ±11.5%FS and ±5.3%FS.

Reducing Temperature Errors

Since the temperature coefficients are two of the main error components, a reduced temperature range or some form of external temperature compensation can greatly reduce overall error. Considering the previous example, a 50% to 80% effective temperature compensation is sufficient to bring TC errors into line with other errors. The TC error is usually monotonic and measured and compensated using the minor output for temperature. For 80% effective temperature compensation (reducing effective range from 60°C to 12°C):

$$\in_C = (\underbrace{0.36}_{\text{Reduced TC Errors}} + 0.24 + 0.9) + (\underbrace{0.36}_{\text{Reduced TC Errors}} + 0.4 + 0.24)$$

Worst-Case: $\in_{WCC} = 0.69 + 1.00 = \pm 1.69$ psia

Most Probable: $\in_{WCI} = \sqrt{0.94 + 0.35} = \pm 1.14$ psia

which results in ±2.8%FS and ±1.9%FS overall errors, reduced from ±8.4%FS and ±4.2%FS by 80%-effective temperature compensation. A corresponding improvement is achieved for the interchangeability accuracy:

$$\in_I = (1.8 + \underbrace{0.29}_{\text{Reduced TC Errors}} + 0.24) + (1.2 + \underbrace{0.36}_{\text{Reduced TC Errors}} + 0.40)$$

Worst-Case: $\in_{WCI} = 2.33 + 1.96 = \pm 4.29$ psia

Most Probable: $\in_{MPI} = \sqrt{3.38 + 1.73} = \pm 2.26$ psia

which results in ±7.2%FS and ±3.8%FS overall errors, reduced from ±11.5%FS and ±5.3%FS, respectively.

Auto-Reference Compensation

A more powerful, easier to use, and generally applicable method, the auto-reference technique can often eliminate all offset errors by periodic sampling of the offset voltage at reference pressure. With this technique, (see Section 7

of the 1977 Pressure Transducer handbook), only the span errors apply. Again, using the LX1610A specifications, the calibrated accuracy is:

$$\epsilon_C = \underbrace{(1.8 + 0.4 + 0.24)}_{\text{Span}}$$

Worst-Case: $\epsilon_{WCC} = \pm 2.44$ psia

Most Probable: $\epsilon_{MPC} = \sqrt{3.46} = \pm 1.86$ psia

which reduces the error to ±4.1%FS or ±3.1%FS, as compared with ±8.4%FS and ±4.2%FS. For interchangeable accuracy it is even more effective:

$$\epsilon_I = \underbrace{(1.2 + 1.8 + 0.4)}_{\text{Span}}$$

Worst-Case: $\epsilon_{WCI} = \pm 3.40$ psia

Most Probable: $\epsilon_{MPI} = \sqrt{4.84} = \pm 2.2$ psia

resulting in ±5.7%FS and ±3.7%FS overall error as compared with ±11.5%FS and ±5.3%FS without auto-reference compensation.

Auto-Reference + Temperature Control

For very high accuracy applications, both auto-reference and effective temperature range reduction may prove valuable. In these cases, the additional temperature compensation may take the form of a temperature-controlled chamber designed to hold temperature within a few degrees of T_{REF} (which may be shifted to a higher temperature to allow use of an oven). In such a case, the only errors included are linearity and hysteresis, span repeatability and span stability. For calibrated accuracy:

$$\epsilon_C = \underbrace{(0.40 + 0.24)}_{\substack{\text{Span} \\ \text{(without TC error)}}}$$

Worst-Case: $\epsilon_{WCC} = \pm 0.64$ psia

Most Probable: $\epsilon_{MPC} = \sqrt{0.22} = \pm 0.47$ psia

which reduces error to ±1.1%FS and ±0.78%FS. For interchangeable accuracy, span calibration error is included:

$$\epsilon_I = \underbrace{(1.2 + 0.40)}_{\substack{\text{Span} \\ \text{(without TC error)}}}$$

Worst-Case: $\epsilon_{WCI} = \pm 1.60$ psia

Most Probable: $\epsilon_{MPI} = \sqrt{1.60} = \pm 1.26$ psia

resulting in ±2.7%FS and ±2.1%FS overall interchangeable errors.

Stability Compensation

With calibrated overall error down to a fraction of a psi, resulting from auto-reference and temperature control, the periodic recalibration of span may become worthwhile. Since the span stability error is a slow aging variation of span voltage and specified for one year, operating or not, a periodic recalibration may well reduce this error by an order of magnitude. Such a recalibration also eliminates the calibration errors so that only calibrated accuracy applies.

$$\epsilon_C = (0.40 + \underbrace{0.04}_{\substack{\text{Reduced} \\ \text{Stability Error}}})$$

Worst-Case: $\epsilon_{WCC} = \pm 0.44$ psia

Most Probable: $\epsilon_{MPC} = \sqrt{0.1616} = \pm 0.40$ psia

resulting in ±0.73%FS and ±0.67%FS overall calibrated accuracy.

Linearity Compensation

For ultra-high accuracy applications, the remaining error, linearity-hysteresis-span repeatability must be reckoned with. The hysteresis and repeatability components of this coefficient are so small as to approach the noise in the operational amplifier included in the hybrid IC pressure transducer this noise is about 0.4%FS for a 1 kHz bandwidth and may require narrow band filter techniques if ultra-high accuracy is to be achieved. We do know, however, that the linearity error is a large fraction of the remaining error, perhaps as high as 90%, and that it can be successfully compensated via curve-fitting techniques to reduce overall calibrated error to about ±0.1%FS, worst-case (see example of Digital Conditioning, Section 8 of 1977 Pressure Transducer handbook).

SUMMING IT UP

As can be seen by these examples, the errors specified for National's transducers are the worst-case errors within the specified operating range. You can obtain higher levels of accuracy by system-error analysis, restriction of operating parameter ranges and error compensation. The main error-causing parameters are time and temperature, and the most dramatic and effective compensation technique is auto-referencing. For higher system-accuracy requirements, a finer degree of error control can be provided by periodic calibration and linearization.

Using the ADC0808/ADC0809 8-Bit μP Compatible A/D Converters with 8-Channel Analog Multiplexer

National Semiconductor
Application Note 247
Larry Wakeman
July 1980

PRELIMINARY

INTRODUCTION

The ADC0808/ADC0809 Data Acquisition Devices (DAD) implement on a single chip most of the elements of the standard data acquisition system. They contain an 8-bit A/D converter, 8-channel multiplexer with an address input latch, and associated control logic. These devices provide most of the logic to interface to a variety of microprocessors with the addition of a minimum number of parts.

These circuits are implemented using a standard metal-gate CMOS process. This process is particularly suitable to applications where both analog and digital functions must be implemented on the same chip.

These two converters, the ADC0808 and ADC0809, are functionally identical except that the ADC0808 has a total unadjusted error of ±1/2 LSB and the ADC0809 has an unadjusted error of ±1 LSB. They are also related to their big brothers, the ADC0816 and ADC0817 expandable 16 channel converters. All four converters will typically do a conversion in ~100 μs when using a 640 kHz clock, but can convert a single input in as little as ~50 μs.

1.0 FUNCTIONAL DESCRIPTION

The ADC0808/ADC0809, shown in *Figure 1*, can be functionally divided into 2 basic subcircuits. These two subcircuits are an analog multiplexer and an A/D converter. The multiplexer uses 8 standard CMOS analog switches to provide for up to 8 analog inputs. The switches are selectively turned on, depending on the data latched into a 3-bit multiplexer address register.

The second function block, the successive approximation A/D converter, transforms the analog output of the multiplexer to an 8-bit digital word. The output of the multiplexer goes to one of two comparator inputs. The other input is derived from a 256R resistor ladder, which is tapped by a MOSFET transistor switch tree. The converter control logic controls the switch tree, funneling a particular tap voltage to the comparator. Based on the result of this comparison, the control logic and the successive approximation register (SAR) will decide whether the next tap to be selected should be higher or lower than the present tap on the resistor ladder. This algorithm is executed 8 times per conversion, once every 8 clock periods, yielding a total conversion time of 64 clock periods.

When the conversion cycle is complete the resulting data is loaded into the TRI-STATE® output latch. The data in the output latch can then be read by the host system any time before the end of the next conversion. The TRI-STATE capability of the latch allows easy interface to bus oriented systems.

The operation of these converters by a microprocessor or some control logic is very simple. The controlling device first selects the desired input channel. To do this, a 3-bit channel address is placed on the A, B, C input pins; and the ALE input is pulsed positively, clocking the address into the multiplexer address register. To begin the conversion, the START pin is pulsed. On the rising edge of this pulse the internal registers are cleared and on the falling edge the start conversion is initiated.

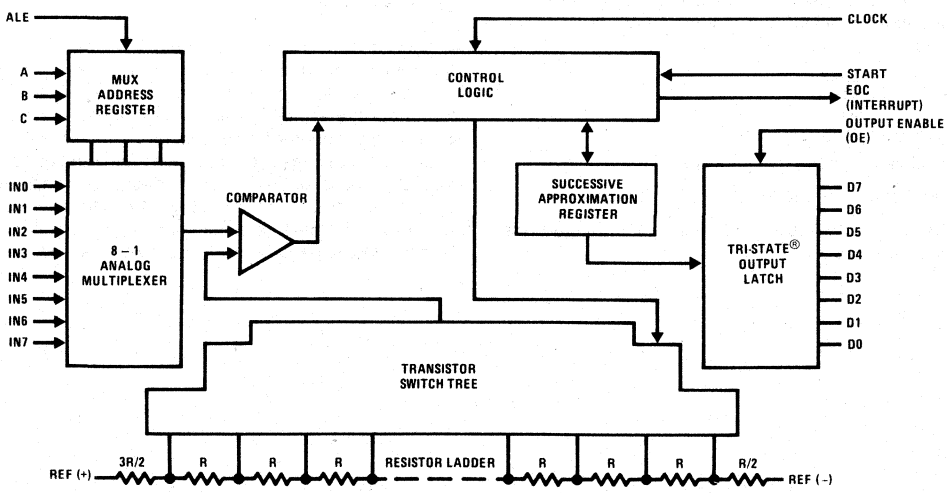


FIGURE 1. ADC0808/ADC0809 Functional Block Diagram

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As mentioned earlier, there are 8 clock periods per approximation. Even though there is no conversion in progress the ADC0808/ADC0809 is still internally cycling through these 8 clock periods. A start pulse can occur any time during this cycle but the conversion will not actually begin until the converter internally cycles to the beginning of the next 8 clock period sequence. As long as the start pin is held high no conversion begins, but when the start pin is taken low the conversion will start within 8 clock periods.

The EOC output is triggered on the rising edge of the start pulse. It, too, is controlled by the 8 clock period cycle, so it will go low within 8 clock periods of the rising edge of the start pulse. One can see that it is entirely possible for EOC to go low before the conversion starts internally, but this is not important, since the positive transition of EOC, which occurs at the end of a conversion, is what the control logic is looking for.

Once EOC does go high this signals the interface logic that the data resulting from the conversion is ready to be read. The output enable (OE) is then raised high. This enables the TRI-STATE outputs, allowing the data to be read. *Figure 2* shows the timing diagram.

2.0 ANALOG INPUTS

2.1 Ratiometric Inputs

The arrangement of the REF(+) and REF(−) inputs is intended to enable easy design of ratiometric converter systems. The REF inputs are located at either end of the 256R resistor ladder and by proper choice of the input voltages several applications can be easily implemented.

Figure 3 shows a typical input connection for ratiometric transducers. A ratiometric transducer is a conversion device whose output is proportional to some arbitrary full-scale value. In other words, the tranducer's absolute output value is of no particular concern but the ratio of the output to the full-scale is of great importance. For example, the potentiometric displacement transducers of *Figure 3* have this feature. When the wiper is at midscale, the output voltage is $V_O = V_F \times$ (Wiper Displacement) $= V_F \times 0.5$. This enables the use of much less accurate and less expensive references. The important consideration for this reference is noise. The reference must be "glitch free" because a voltage spike during a conversion cycle could cause conversion inaccuracies.

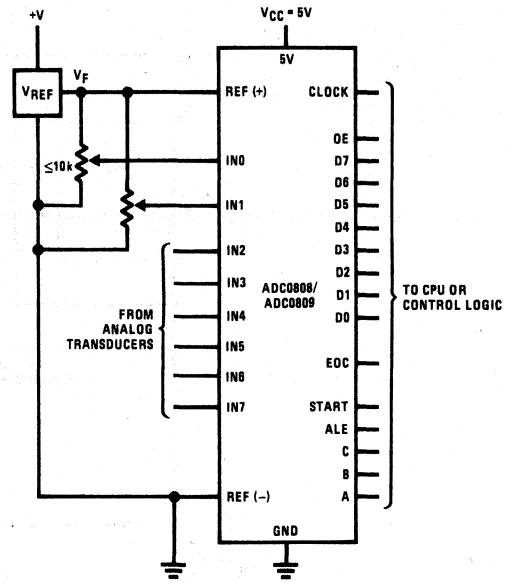


FIGURE 3. Ratiometric Converter with Separate Reference

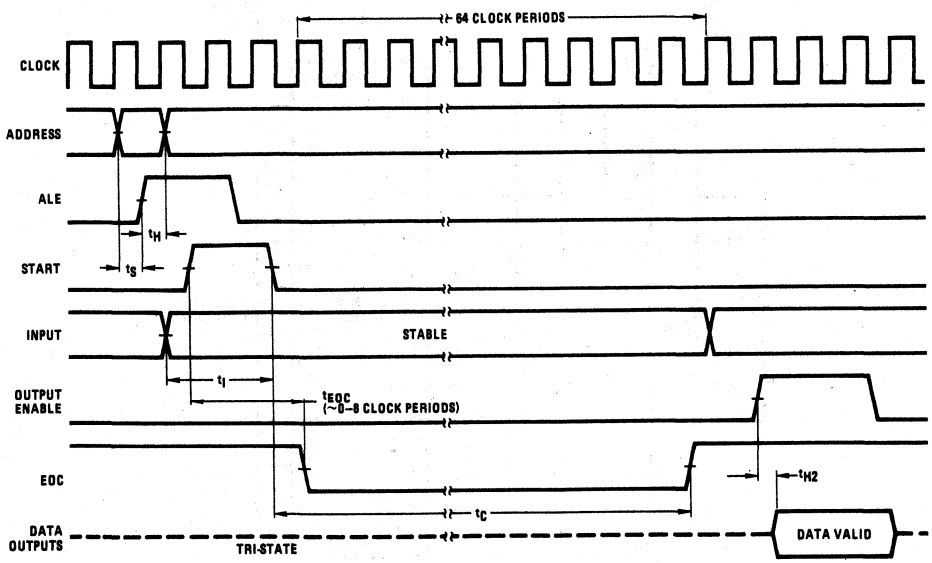


FIGURE 2. ADC0808/ADC0809 Timing Diagram

Since highly accurate references aren't required it is possible to use the system power supply as a reference, as shown in *Figure 4*. If the power supply is to be used in this manner supply noise must be kept to a minimum to preserve conversion accuracy. If possible the supply should be well bypassed and separate reference and supply PC board traces, originating as close as possible to the power supply or regulator, should be used. This is illustrated in *Figure 4*.

External accessibility of both ends of the resistor ladder enables several variations on these basic connections, and are shown in *Figures 5 and 6*. The magnitude of the reference voltage, $V_{REF} = REF(+) - REF(-)$, can be varied from about $-0.5V$ to V_{CC}, but the center voltage must be maintained within $\pm 0.1V$ of $V_{CC}/2$. This constraint is due to the design of the transistor switch tree, which could malfunction if the offset from center scale becomes excessive. Variation of the reference voltage can sometimes eliminate the need for external gain blocks to scale the input voltage to a full-scale range of 5V.

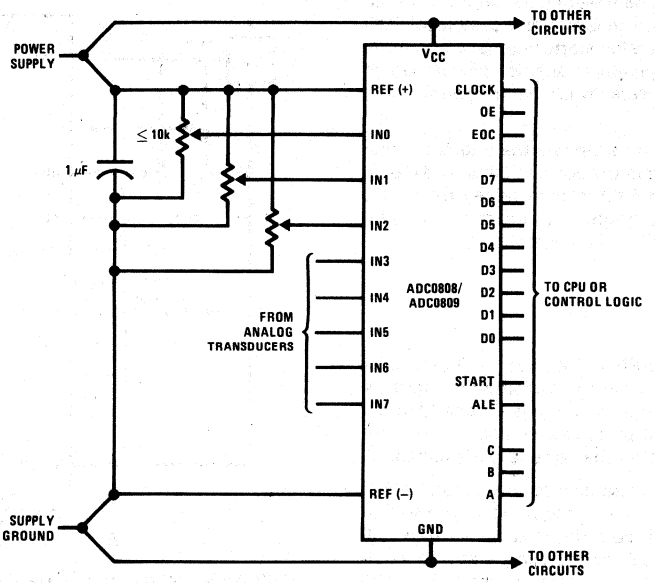


FIGURE 4. Ratiometric Converter with Power Supply Reference

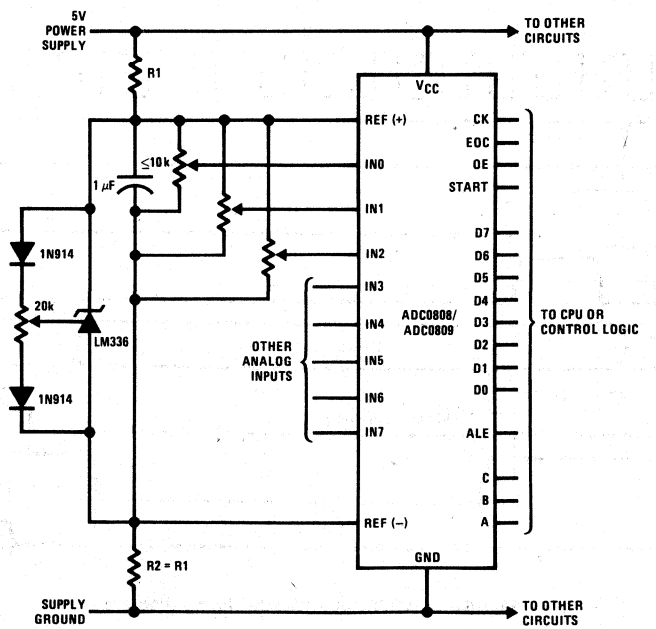


FIGURE 5. Mid-Supply Centered Reference using LM336 2.5V Reference

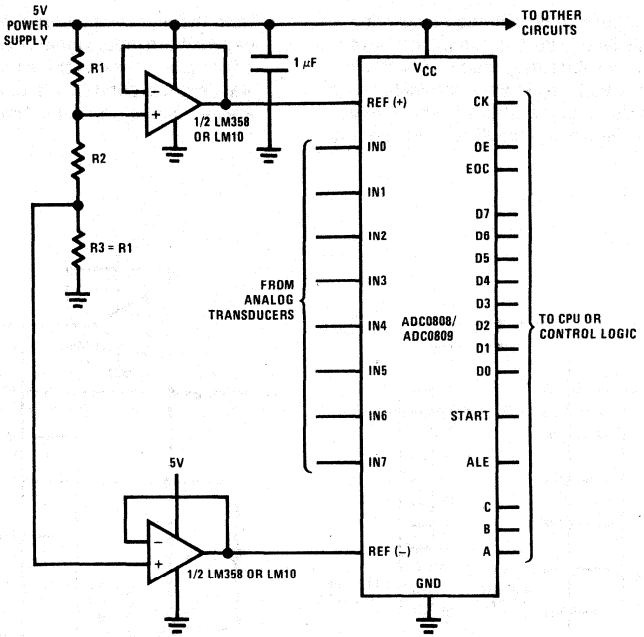


FIGURE 6. Mid-Supply Centered Reference using Buffered Resistors

Figure 5 shows a center referencing technique, using two equal resistors to symmetrically offset an LM336 2.5V reference, from both supplies. The offset from either supply is:

$$V_{OFF} = \frac{V_{CC} - V_{REF}}{2} = 1.25V$$

These resistors should be chosen so that they limit current through the LM336 to a reasonable value, say 5 mA. The total resistor current is:

$$I_R = I_{REF} + I_{LADDER} + I_{TRAN}$$

where I_{LADDER} is the 256R ladder current, I_{TRAN} is the current through all the transducers, and I_{REF} is the current through the reference. R1 and R2 should be well matched and track each other over temperature.

For odd values of reference voltage, the reference could be replaced by a resistor, but due to loading and temperature problems, these resistors should be buffered to the REF(+) and REF(−) inputs, *Figure 6*. The power supply must be well bypassed as supply glitches would otherwise be passed to the reference inputs. The reference voltage magnitude is:

$$V_{REF} = V_{DD}\left(\frac{R2}{2R1 + R2}\right) \quad R3 = R1$$

There are several op amps that can be used for buffering this ladder. Without adding another supply, an LM358 could be used if the REF(+) input is not to be set above 3.5V. The LM10 can swing closer to the positive supply and can be used if a higher, $V_{REF(+)}$ voltage is needed.

As the REF(+) to REF(−) voltage decreases the incremental voltage step size decreases. At 5V one LSB represents ~20 mV, but at 1V, one LSB represents ~4 mV. As the reference voltage decreases, system noise will become more significant so greater precaution should be enforced at lower voltages to compensate for system noise; i.e., adequate supply and reference bypassing, and physical as well as electrical isolation of the inputs.

2.2 Absolute Analog Inputs

The ADC0808/ADC0809 may have been designed to easily utilize ratiometric transducers, but this does not preclude the use of non-ratiometric inputs. A second type of input is the absolute input. This is one which is independent of the reference. This implies that its *absolute* numerical voltage value is very critical, and to accurately measure this voltage the accuracy of the reference voltage becomes equally critical. The previous designs can be modified to accommodate absolute input signals by using a more accurate reference. In *Figure 4* the power supply reference could be replaced by an LM336-5.0 reference. R1 and R2 of *Figure 6*, and R1 and R3 of *Figure 7* may have to be made more accurately equal.

In some small systems it is possible to use the precision reference as the power supply as shown in *Figure 7*. An unregulated supply voltage >5V is required, but the LM336-5.0 functions as both a regulator and reference. The dropping resistor R must be chosen so that, for the whole range of supply currents needed by the system, the LM336-5.0 will stay in regulation. As in *Figure 4* separate supply and reference traces should be used to maintain a noiseless supply.

If the system requires more power, an op amp can be used as shown in *Figure 8* to isolate the reference and boost the supply current capabilities. Here again, a single unregulated supply is required.

2.3 Differential Inputs

Differential measurements can be obtained by playing a little software trick. This simply involves sequentially converting two channels then subtracting the two results. For example, if the difference voltage between channel 1 and 2 is required, merely convert channel 1 and read the result. Then convert channel 2, input the result, and subtract it from the first result. *(See Figure 9.)* When using this procedure, both input signals must be stable throughout both conversion times or the end result will be incorrect. One way to get around this is to use two sample/holds which are sampled at the same time.

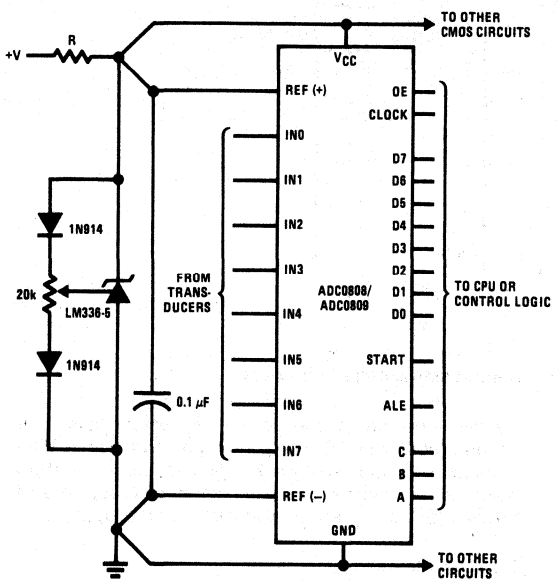


FIGURE 7. Precision Reference used as a Power Supply

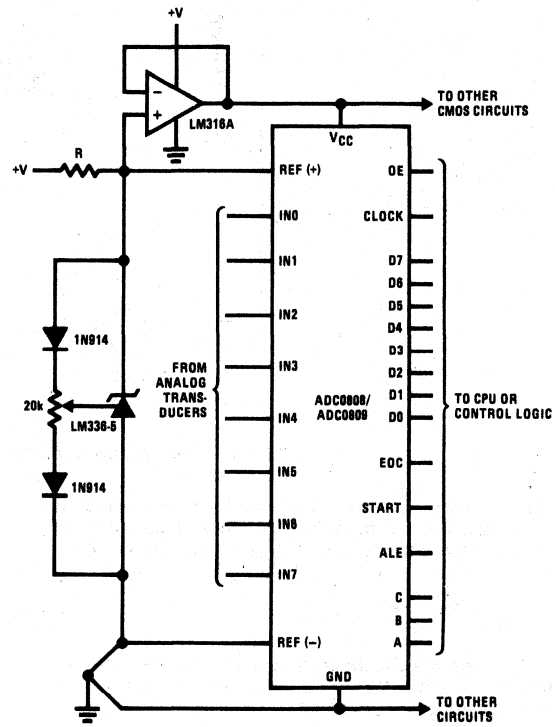


FIGURE 8. Precision Reference Buffered for Power Supply

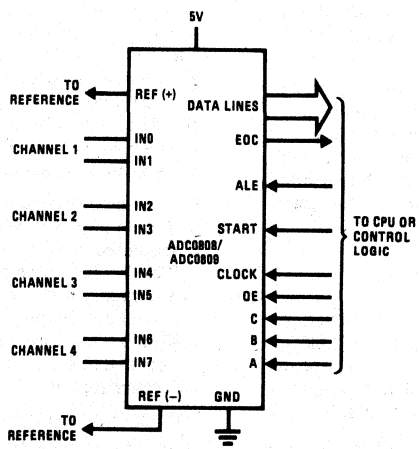


FIGURE 9. Software Controlled Differential Converter

A second method is to use two chips to convert a differential channel, *Figure 10*. Typically each channel 1 would be connected to opposite sides of the differential input. Both converters are started simultaneously. When both converters' EOC outputs go high the output of the AND gate will go high indicating that the data is ready to be read.

The circuit in *Figure 10* can be slightly modified to provide increased data throughput by using two converters in a parallel data acquisition scheme. *Figure 11* shows this circuit in which all the input channels are connected in pairs through LF398 monolithic sample/holds. Under normal operation a sample/hold is accessed through an MM74C42 which will pulse an MM74C221, generating a sample pulse. After a sample/hold is done sampling the signal, the appropriate channel is started. If this process is alternated between two converters the sample rate can be doubled.

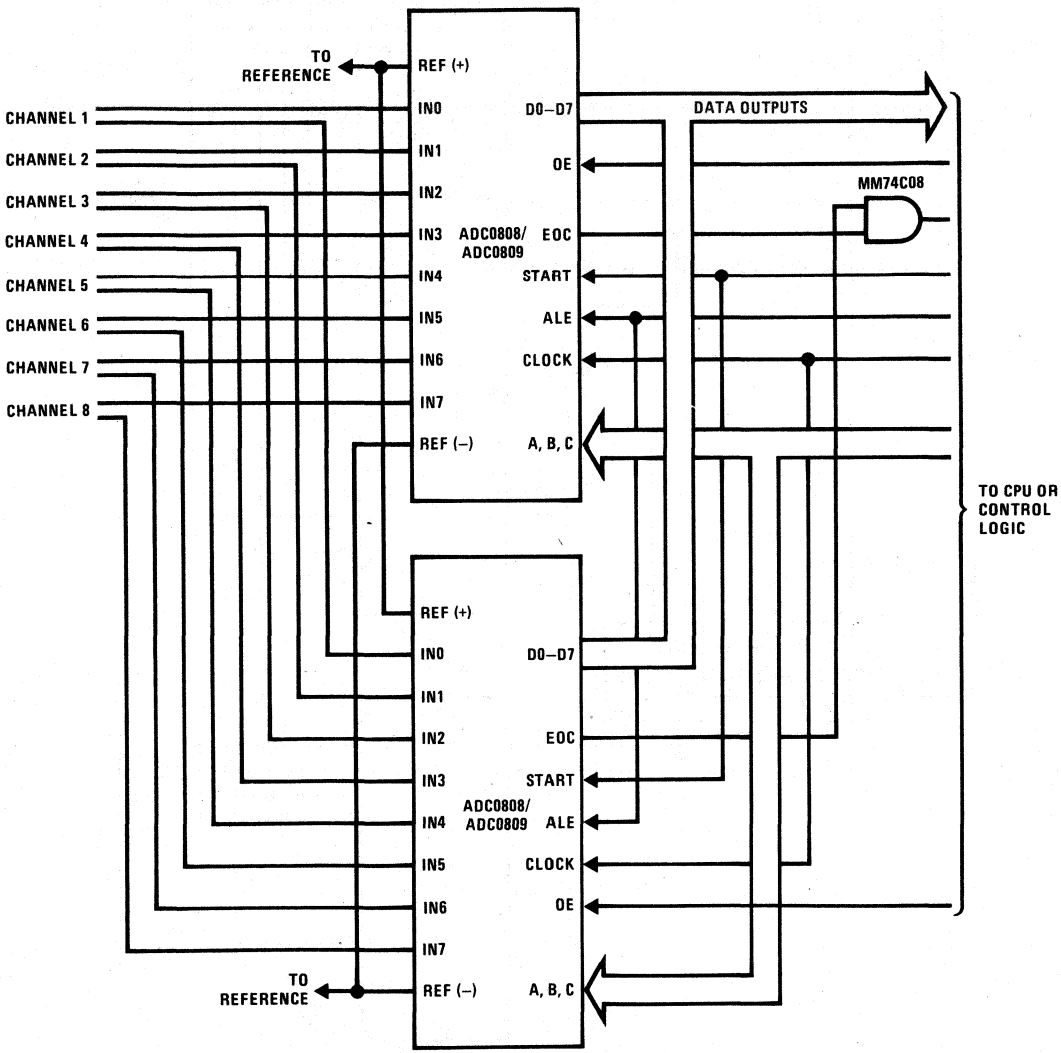


FIGURE 10. Dual Converter Differential Circuit

2.4 Analog Input Considerations

Analog inputs into the ADC0808/ADC0809 can handle any input signal that is maintained within the supply limits, but some careful consideration must be given to the output impedance of the transducer or buffer. Using transducers with large source impedances can cause errors due to comparator input currents.

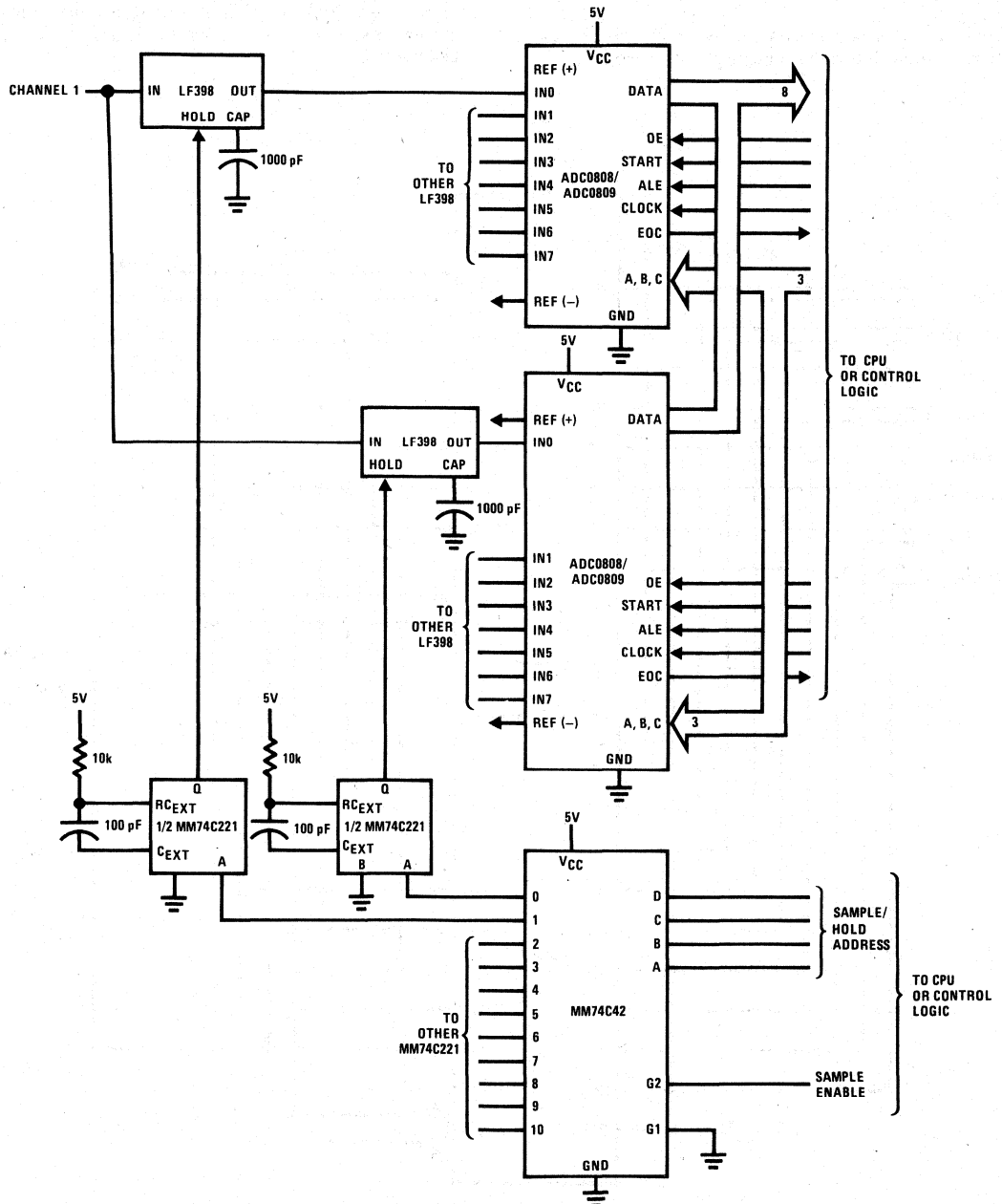


FIGURE 11. Parallel Data Acquisition with Sample/Holds

To understand the nature of these currents a short discussion of comparator operation is required. *Figure 12* shows a simplified model of the comparator and multiplexer. This comparator alternately samples the input voltage and the ladder voltage. As it samples the input, C_C and C_P are charged up to the input voltage. It then samples the ladder and discharges the capacitor. The net charge difference is determined by a modified inverter chain and results in a 1 or 0 state at the output.

Eight samples are made per conversion, resulting in eight spikes of varying magnitude on the input.

If the source resistance is large, it adds to the RC time constant of the switched capacitor which will inhibit the input from settling properly, causing errors. As one might expect, the maximum source resistance allowable for accurate conversions is inversely proportional to clock frequency. This resistance should be ≤ 1 kΩ at 1.2 MHz and ≤ 2 kΩ at 640 kHz. If a potentiometer-type ratiometric transducer is used it should be ≤ 5 kΩ at 1.2 MHz and ≤ 10 kΩ at 640 kHz.

If large source impedances are unavoidable (≥ 2 kΩ at 640 kHz), the transient errors can be reduced by placing a bypass capacitor ≥ 0.1 μF from the analog inputs to ground. This will reduce the spikes to a small average current which will cause some error as well, but this can be much less than the error otherwise incurred. The maximum voltage error for a potentiometer input with a bypass capacitor added is:

$$V_{ERR} \approx \left[\frac{R_{POT}}{5}(I_{IN})\frac{Ck}{640\text{ kHz}}\right] V$$

where R_{POT} = total potentiometer resistance; I_{IN} = maximum input current at 640 kHz, 2 μA; and Ck = clock frequency.

For standard buffer source impedance the maximum error is:

$$V_{ERR} = \left[I_{IN} R_S \left(\frac{Ck}{640\text{ kHz}}\right)\right] V$$

where R_S = buffer source resistance; I_{IN} = the maximum input current at 640 kHz, 2 μA; and Ck = clock frequency.

3.0 MICROPROCESSOR INTERFACING

The ADC0808/ADC0809 converters were designed to interface to most standard microprocessors with very little external logic, but there are a few general requirements which must be considered to ensure proper converter operation.

Most microprocessors are designed to be TTL compatible and, due to speed and drive requirements, incorporate many TTL circuits. The data outputs of the ADC0808/ADC0809 are capable of driving one standard TTL load which is adequate for most small systems, but for larger systems extra buffering may be necessary. The EOC output is not quite as powerful as the data outputs, but normally it is not bussed like the data outputs.

The converter inputs are standard CMOS compatible inputs. When TTL outputs are connected to any of the digital inputs a pull-up resistor should be tied from the TTL output to V_{CC}, ~ 5 kΩ. This will ensure that the TTL will pull-up above 3.5V.

Usually the converter clock will be derived from the microprocessor system clock. Some slower microprocessor clocks can be used directly, but at worst a few divider stages may be necessary to divide microprocessor clock frequencies above 1.2 MHz to a usable value.

The timing of the START and ALE pulses relative to channel selection and signal stability can be critical. The simplest approach to microprocessor interfaces usually ties START and ALE together. When these lines are strobed the address is strobed into the address register and the conversion is started. The propagation delay from ALE to the comparator input of the selected input signal is about ~3.0 μs (input source resistance $\ll 1$ kΩ). If the start pulse is very short the comparator can sample the analog input before it is stable. When using a slow clock ≤ 500 kHz the sample period of the comparator input is long enough to allow this delay to settle out.

If the ADC0808/ADC0809 clock is >500 kHz, a delay between the START and ALE pulses is required. There are three basic methods to accomplish this. The first possibility is to design the microprocessor interface so that the START and ALE inputs are separately accessible. This is simple if some extra address decoding is available. Separate accessibility of the START and ALE pins allows the microprocessor, via software, to set the delay time between the START and ALE pulses.

If extra decoding is not available, then START and ALE could be tied together. To obtain the proper delay, the microprocessor would cause START/ALE to be strobed twice by executing the load and start instruction twice. The first time this instruction is executed, the new channel address is loaded and the conversion is started. The second execution of this instruction will reload the same channel address and restart the conversion. But since the multiplexer address register contents are unchanged the selected analog input will have already settled by the time the second instruction is issued. Actual implementations of these ideas are shown in following sections.

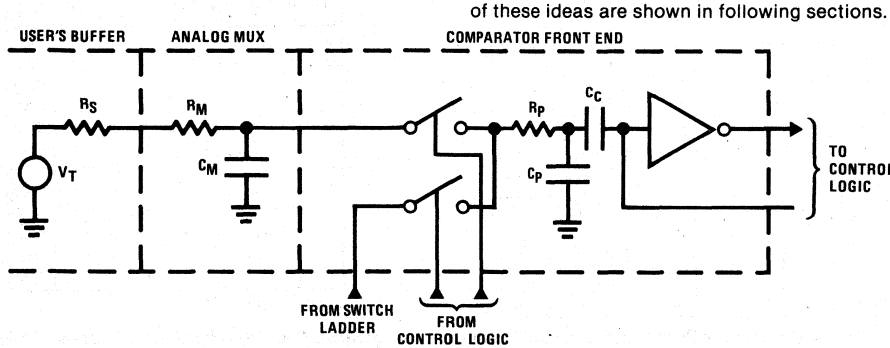


FIGURE 12. Analog Multiplexer and Comparator Input Model

A third possibility when ALE and START are tied together is to stretch the microprocessor derived ALE/START pulse by inserting a one-shot at these inputs and creating a positive pulse >3 μs. Since ALE loads the multiplexer register on the positive going edge of the pulse and START begins the conversion on the falling edge, the width of the pulse sets the ALE to START delay time.

Most microprocessor interfaces would be designed such that a START pulse is issued by a memory or I/O write instruction, although a memory or I/O read can be used. The ALE strobe on the other hand, requires a write by the CPU when A, B, and C are connected to the data bus, and could use a read instruction if A, B, and C are connected to the address bus, but the software could get confusing. The logic to derive the OE strobe must be connected to the microprocessor so that a memory or I/O read instruction will cause OE to be pulsed. A read is required since the ADC0808/ADC0809 data must be read.

3.1 Interfacing to the INS8080

The simplest interface would contain no address decoding, which may seem unreasonable; but if the system ports are I/O mapped, up to 8 of them can be connected to the CPU with no decoding. Each of the 8 I/O address lines would serve as a simple port enable line which would be gated with read and write strobes to select a particular port. This scheme is shown in *Figure 13*. A7 is the address line used and, whenever it is zero and an I/O read or write is low, the port is accessed. This implementation shows A, B, C connected to D0, D1, D2 causing the information on the data bus to select the channel, but A, B, and C could be connected to the address bus, with a loss of only 3 ports. Both decoding schemes are tabulated in *Figure 14*. (Remember A, B, C inputs are only valid when selecting a channel to convert, and are not used to read data.)

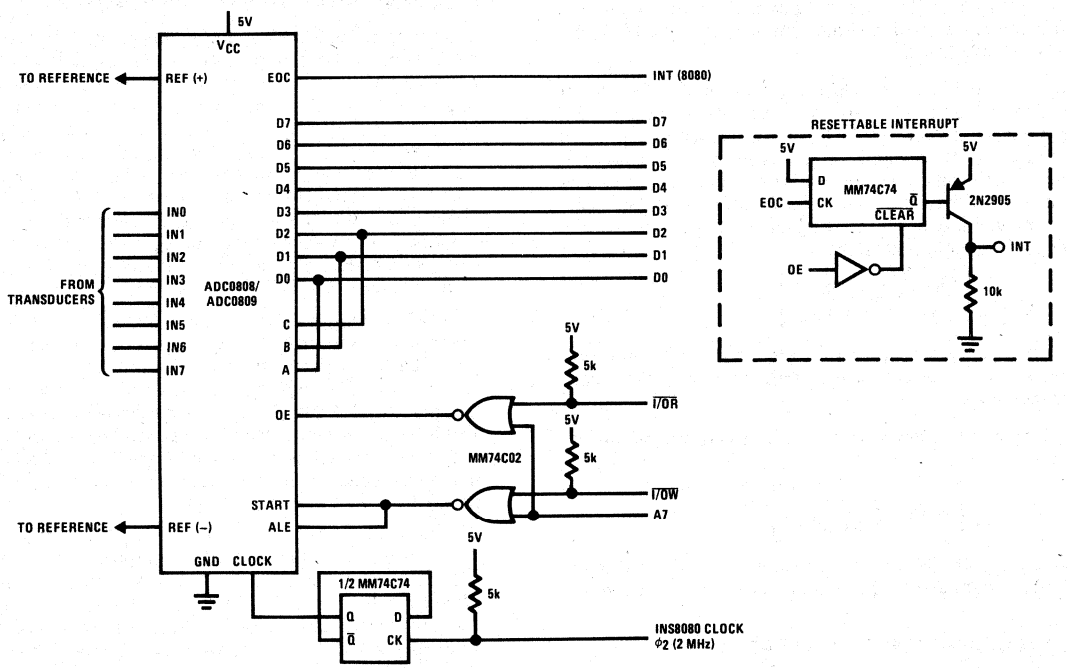


FIGURE 13. Minimum INS8080/INS8224/INS8238 Interface

A7	A6	A5	A4	A3	A2	A1	A0	D2	D1	D0	Output Port Description
1	1	1	1	1	1	1	0	X	X	X	Spare Port
1	1	1	1	1	1	0	1	X	X	X	Spare Port
1	1	1	1	1	0	1	1	X	X	X	Spare Port
1	1	1	1	0	1	1	1	X	X	X	Spare Port
1	1	1	0	1	1	1	1	X	X	X	Spare Port
1	1	0	1	1	1	1	1	X	X	X	Spare Port
1	0	1	1	1	1	1	1	X	X	X	Spare Port
0	1	1	1	1	1	1	1	0	0	0	Channel 0 Port
0	1	1	1	1	1	1	1	0	0	1	Channel 1 Port
0	1	1	1	1	1	1	1	0	1	0	Channel 2 Port
0	1	1	1	1	1	1	1	0	1	1	Channel 3 Port
0	1	1	1	1	1	1	1	1	0	0	Channel 4 Port
0	1	1	1	1	1	1	1	1	0	1	Channel 5 Port
0	1	1	1	1	1	1	1	1	1	0	Channel 6 Port
0	1	1	1	1	1	1	1	1	1	1	Channel 7 Port

FIGURE 14a. Write Address Decoding for INS8080 Output Ports (A, B, C Connected to D0, D1, D2)

A7	A6	A5	A4	A3	A2	A1	A0	Output Port Description
0	1	1	1	1	0	0	0	Channel 0 Port
0	1	1	1	1	0	0	1	Channel 1 Port
0	1	1	1	1	0	1	0	Channel 2 Port
0	1	1	1	1	0	1	1	Channel 3 Port
0	1	1	1	1	1	0	0	Channel 4 Port
0	1	1	1	1	1	0	1	Channel 5 Port
0	1	1	1	1	1	1	0	Channel 6 Port
0	1	1	1	1	1	1	1	Channel 7 Port
1	1	1	1	0	X	X	X	Spare Port
1	1	1	0	1	X	X	X	Spare Port
1	1	0	1	1	X	X	X	Spare Port
1	0	1	1	1	X	X	X	Spare Port

X = don't care

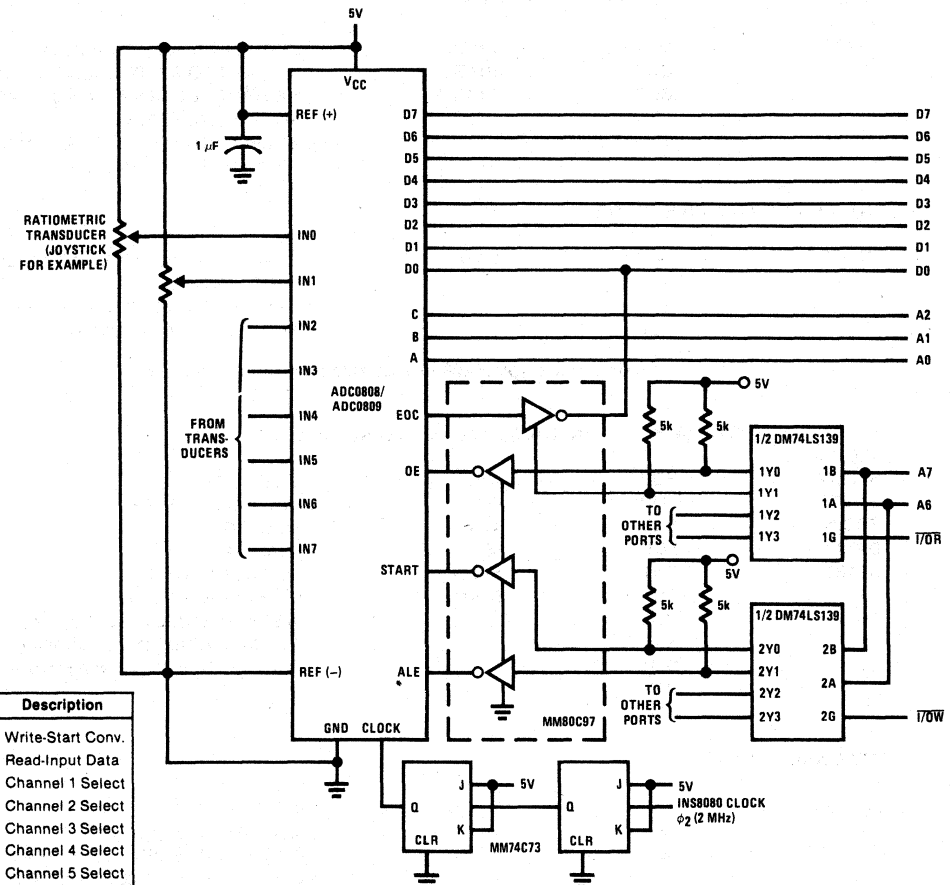
FIGURE 14b. Modified Write Address Decoding for INS8080 Output Ports (A, B, C Connected to A0, A1, A2)

Two LSTTL NOR gates are used to generate to the ADC0808/ADC0809 read/write strobes. When the INS8080 writes to the ADC0808/ADC0809 the ALE and START inputs are strobed, loading and starting the conversion. When the CPU reads the ADC0808/ADC0809 the OE input is taken high, and the data outputs are enabled.

Figure 13 implements a simple interrupt concept where EOC is tied directly to the INS8080 interrupt input. When the INS8238 is used and the INTA pin is tied high through a 1 kΩ resistor, the interrupt will cause a restart, RST, instruction to be executed, which will then cause a jump to a restart vector and execution of the interrupt routine. If a very simple multi-interrupt system is desired, a wire OR'ed configuration employing resettable latches as shown in *Figure 13's* inset can be used. In this simple design the MM74C74 is reset when the ADC0808/ADC0809 data is read. If more complicated interrupt structures are required, then an interrupt controller is usually the best solution.

The I/O port address structure for *Figure 13's* implementation is shown in *Figure 14a*. If the A, B, C inputs are tied to A0, A1, A2 inputs the port structure is as shown in *Figure 14b*. The later method makes each channel look like a separate port address whereas, if A, B, C are tied to the data bus the ADC0808/ADC0809 looks like one start conversion port address, whose channel is selected by the 3-bit status word written to it on the data bus.

Figure 15 shows a slightly more complex interface, where the address is partially decoded by a DM74LS139, dual 2-4 line decoder which creates the read and write strobes to operate the converter. This design interfaces to the processor in a polled type of interface. An MM80C97 TRI-STATE® buffer is used to buffer the EOC line to the data bus, as well as provide the correct level for the START, ALE, and OE pulses. The converter clock is a divided INS8080 system clock.



Address A7-A0	Description
00XXXXXX	Write-Start Conv.
00XXXXXX	Read-Input Data
01XXX000	Channel 1 Select
01XXX001	Channel 2 Select
01XXX010	Channel 3 Select
01XXX011	Channel 4 Select
01XXX100	Channel 5 Select
01XXX101	Channel 6 Select
01XXX110	Channel 7 Select
01XXX111	Channel 8 Select
01XXXXXX	Read-Input $\overline{EOC}$

FIGURE 15. INS8080/INS8224/INS8238 Interface using Partial Decoding

Typically, the software to use *Figure 15* would first select the desired channel by writing the channel address to the ALE port address, 01XXXCBA, where X = don't care, and CBA is the channel address. Next the conversion is started by writing to the START address, 00XXXXXX. Now the processor must wait a few instruction cycles to allow EOC to fall. Once EOC falls, its status can be checked by reading the EOC line, address 01XXXXXX. When the EOC line is detected high again (a low on DO), the data can be read by accessing the OE port, address 00XXXXXX. As in the previous example the A, B, C inputs can be tied to D0, D1, D2 rather than A0, A1, A2, so that the information on the data bus selects the channel to be converted. *Figure 15* can be connected in an interrupt mode by incorporating the interrupt flip-flop of *Figure 13.*

A few typical utility routines to operate the ADC0808/ADC0809 application in *Figure 13* are shown in *Figure 16a.* These routines assume that the resettable interrupt flip-flop is used. *Figure 16b* illustrates some typical polled I/O routines for *Figure 15.* Notice that in *Figure 16a* the OUT START1 instruction is executed twice to allow the analog input signal to settle as discussed earlier.

```
;
;
; START CONVERSION (A, B, C CONNECTED TO D0, D1, D2)
;
  CHANN1          EQU         7
  START1          EQU         7FH
  DATA            EQU         7FH
;
  START:          LDA         CHANN1      ; LOAD CHANNEL ADDRESS INTO ACE
                  OUT         START1      ; STORE IT TO ADC0808/ADC0809 AND START
                  OUT         START1      ; RESTART ADC0808/ADC0809 TO ACCOUNT FOR
;                                         ; MULTIPLEXER DELAY
                  EI                      ; ENABLE INTERRUPTS IF NOT ALREADY
                  —           —           ; PROCESS PROGRAM
;
; INTERRUPT HANDLER ROUTINE
;
  INTRP:          IN          DATA        ; READ DATA AND RESET INTERRUPT
                  —           —           ; PROCESS DATA
                  EI                      ; ENABLE INTERRUPTS IF DESIRED
                  RET                     ; RETURN TO MAIN PROGRAM
```

FIGURE 16a. Typical 8080 Resettable Interrupt I/O Routines

```
;
; START CONVERSION (A, B, C CONNECTED TO A0, A2, A3) AND POLL EOC
; (FIGURE 15)
  SELECT          EQU         40H         ; SELECT CHANNEL 0
  START           EQU         00H         ; START CONVERTER
  EOCIN           EQU         40H         ; READ EOC
  DATA            EQU         00H         ; READ DATA
  START:          OUT         SELECT      ; SELECT CHANNEL
                  OUT         START       ; START CONVERSION
                  N0P                     ; INSERT INSTRUCTIONS TO WAIT 0-8
                  N0P                     ; CLOCK PERIODS OF ADC0808/ADC0809 CLOCK
                  N0P                     ; FOR EOC TO DROP (8 N0Ps MINIMUM)
                  N0P
                  N0P
;
; READ AND TEST EOC
;
  STATUS:         IN          EOCIN       ; INPUT EOC BIT
                  ANI         01H         ; MASK OUT OTHER BITS
                  JZ          READY       ; IF INPUT BIT IS ZERO JUMP READY
                  —           —           ; ELSE CONTINUE EXECUTING PROGRAM
; OR
; CONTINUOUS POLLING ROUTINE
;
  STAT 2:         IN          EOCIN       ; INPUT EOC STATUS BIT
                  ANI         01H         ; MASK OUT ALL BITS BUT D0
                  JNZ         STAT 2      ; JUMP TO TRY AGAIN IF NOT READY
  READY:          IN          DATA        ; IF READY INPUT DATA
                  —           —           ; CONTINUE EXECUTING PROGRAM
```

FIGURE 16b. Typical 8080 Polled I/O Routines for ADC0808/ADC0809

The application in *Figure 17* uses a 6-bit bus comparator and a few gates to decode a read and write strobe. Viewed from the CPU this interface looks like a bidirectional data port whose address is set by the logic levels on the T_n inputs of the DM8131 comparator. When data is written to the ADC0808/ADC0809 the 3 least significant bits on the address bus define the channel to be converted. The rest of the bits are decoded to provide the START and ALE strobes. When the conversion is completed EOC sets the interrupt flip-flop, and when the data is read the interrupt is reset.

Both the decoder and the bus comparator methods of address decoding have their own advantages. Bus comparators will more completely decode addresses but are capable of only a limited number of port strobes. Decoders, on the other hand, provide less decoding but more port strobes. There is a trade off for minimum parts systems as far as which route to go, and it will depend on the CPU and type of system.

3.2 Interfacing to the 6800

The ADC0808/ADC0809 easily interface to more than one microprocessor. The 6800 can also be used to control the converter. The 6800 has no separate I/O address space so all I/O transfers must be memory mapped. In general more address decoding logic is required to ensure that the I/O ports don't overlap existing memory. For small systems a partial address decoding scheme is shown in *Figure 18.* Generally, if several ports are desired, a small block of memory would be set aside, as is accomplished by the DM8131. *Figure 18* also illustrates a typical 6800 interrupt scheme using a flip-flop and open collector transistor. The interrupt is reset when the data is read. If more ports are needed, a decoder could be added as shown in *Figure 19. Figure 19* also illustrates a polled I/O mode using TRI-STATE® buffer to gate EOC onto the data bus. As with the INS8080 the A, B, C inputs of the ADC0808/ADC0809 can be connected to the address bus or the data bus.

The 6800 differs from the INS8080 in that the 6800 has a single read/write (R/$\overline{W}$) strobe and a valid memory address (VMA), whereas the INS8080 has separate read and write strobes ($\overline{I/OR}$ and $\overline{I/OW}$). Normally, to obtain a read pulse, VMA, R/$\overline{W}$ and ϕ_2 are gated together and, for a write, R/$\overline{W}$ is inverted. ϕ_2 is the 6800 phase 2 system clock. Also notice that the 6800 $\overline{INT}$ interrupt input is active low. This enables a standard wired-OR open collector design to be implemented.

Figure 20 illustrates some typical 6800 software utility routines for either polled or interrupt interfaces. Again notice double start instructions.

3.3 Z80 Interface

Interfacing the Z80 to the ADC0808 is much the same as interfacing to an INS8080/INS8224/INS8238 CPU group. CPU instruction timing is very similar, except the read/write control stgnals are slightly different. Instead of the $\overline{I/OW}$ write strobe there is the $\overline{IOREQ}$ and $\overline{WR}$ and instead of $\overline{I/OR}$, $\overline{IOREQ}$ and $\overline{RD}$ are supplied.

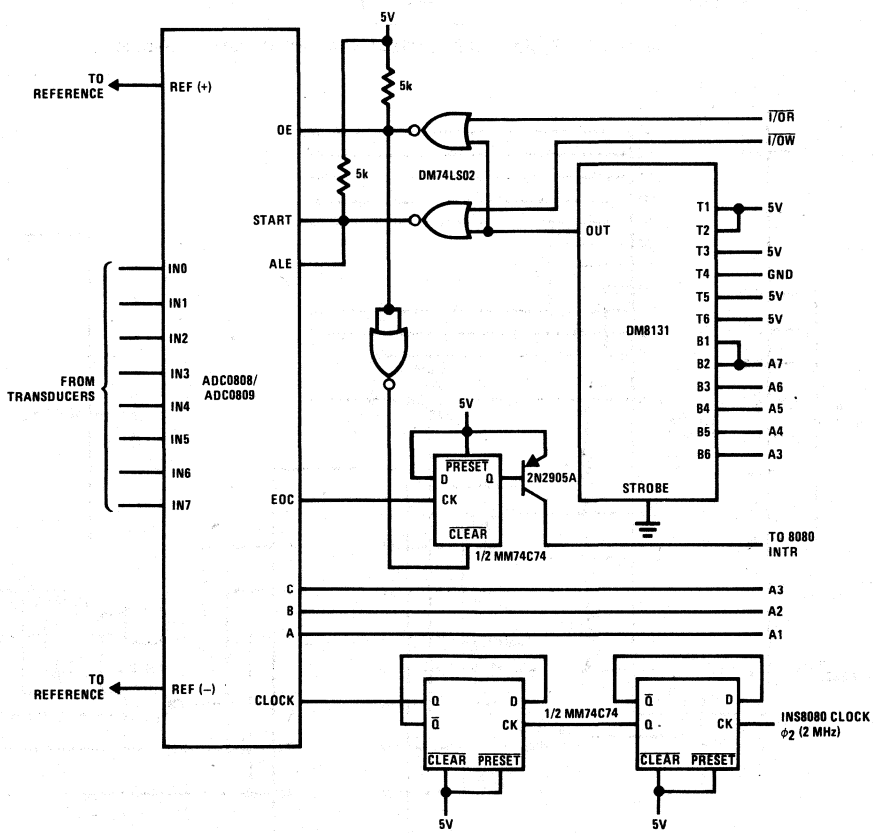


FIGURE 17. Interrupt-Type INS8080/INS8224/INS8238 Interface using 6-Bit Bus Comparator

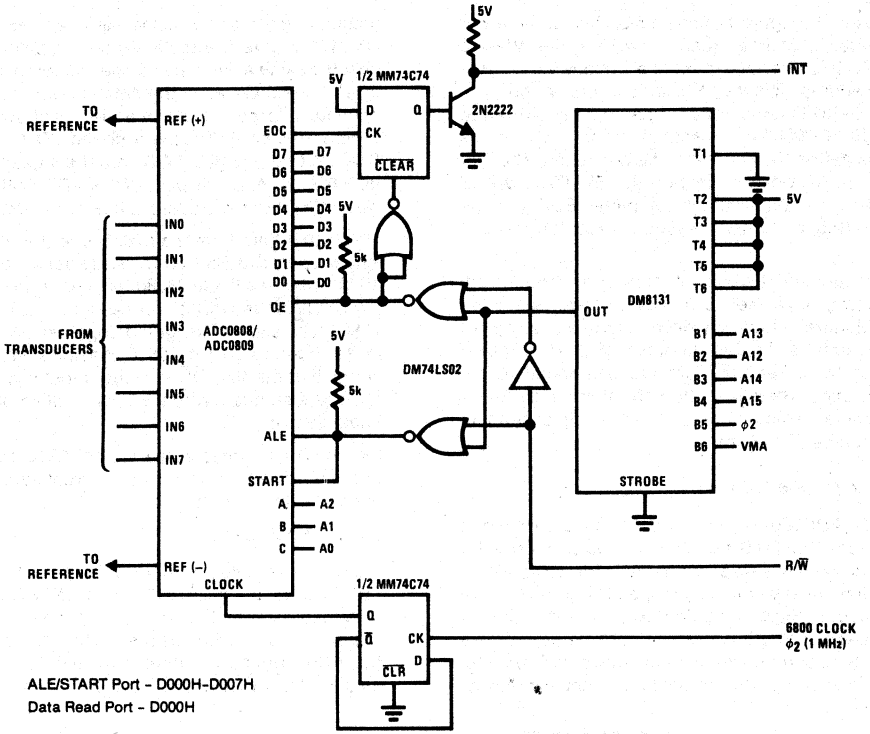


FIGURE 18. Typical 6800 Interface with Partial Address Decoding

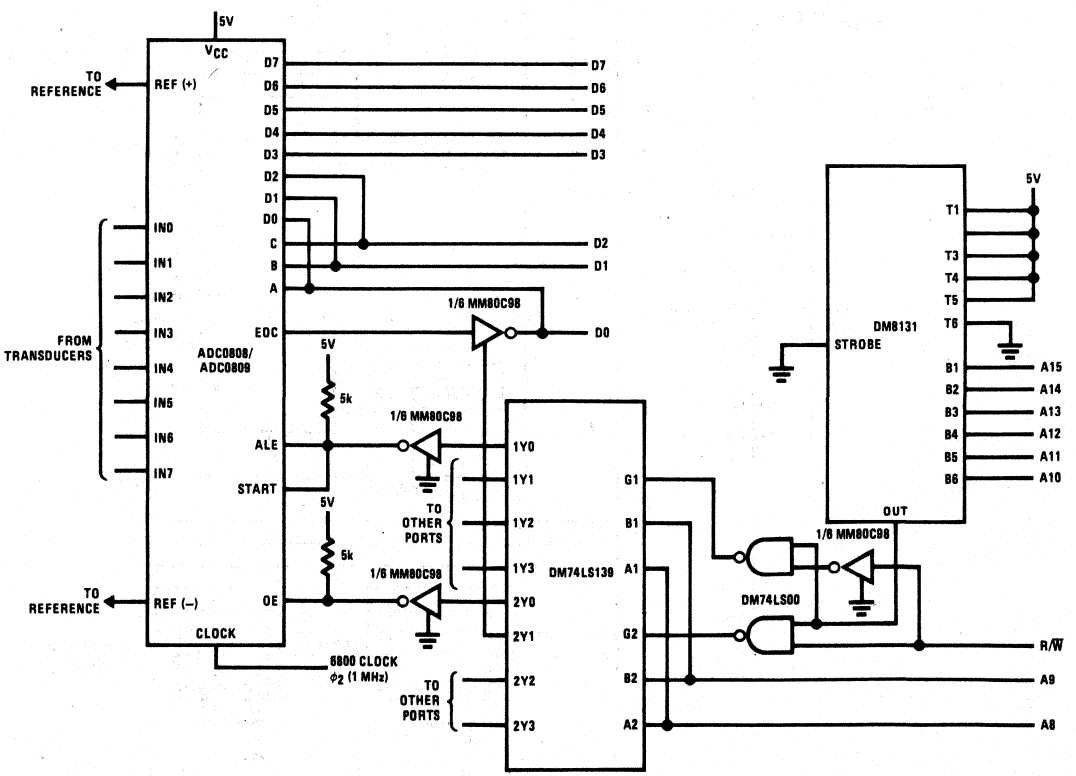


FIGURE 19. Fully Decoded 6800 Interface Address

```
*
*UTILITY ROUTINES FOR ADC0808/ADC0809 INTERFACE
*
*
*LOAD AND START CONVERSION (FIGURE 18)
*
 STATUS          EQU         $D800          START ADDRESS FOR CHANNEL 0
 DATA            EQU         $D800          CONVERTER DATA ADDRESS
*                                           .
*
*
 START           STA         STATUS         SELECT CHANNEL 0 AND START
                 STA         STATUS         DO AGAIN TO LET INPUTS SETTLE
                 LDX         #VECTOR        LOAD INTERRUPT VECTOR ADDRESS
                 STX         $FFF8          STORE IT
                 — —                        EXECUTE MISC PROGRAM
                 — —
                 — —
                 CLI                        ENABLE INTERRUPT IF NOT ALREADY
                 — —                        EXECUTE MISC PROGRAM
                 WAI                        WAIT FOR INTERRUPT
*
*INTERRUPT HANDLER (FIGURE 18)
*
 VECTOR          LDAA        DATA           LOAD DATA RESET INTERRUPT
                 CLI                        ENABLE INTERRUPTS (OPTION)
                 — —                        EXECUTE PROGRAM
                 RTI                        RETURN TO MAIN PROGRAM
*
*START AND TEST CONVERSION POLLED MODE (FIGURE 19)
*
 DATA2           EQU         $F800          CONVERTER DATA ADDRESS
 CHANN2          EQU         02             CHANNEL 2 ADDRESS
 EOCIN           EQU         $F900          EOC INPUT PORT
 START 2         LDAA        CH. 2          LOAD A ACCUMULATOR
                 STAA        STATUS         LOAD ADDRESS AND START
                 N0P                        WAIT
                 STAA        STATUS         RESTART TO LET MUX SETTLE
                 N0P                        8 N0PS TO WAIT FOR EOC
                 — —                        TO GO LOW
                 LDAA        EOCIN          LOAD EOC STATUS BIT
                 ANDA        01             MASK BITS 1-7
                 BEQ         READY          IF A = 0 THEN CONVERTER DONE
*
*
                 — —                        EXECUTE MISC PROGRAM

*
*CONTINUOUS POLLING OF EOC (FIGURE 19)
*
*
 POLLIT          LDAA        EOCIN          LOAD EOC STATUS
                 ANDA        CH. 2          MASK MSBs
                 BNE         POLL IT        IT ACC ≠ 0 NOT READY, LOOP
 READY           LDAA        DATA           ELSE READ DATA
                 — —                        CONTINUE PROGRAM
                 — —
```

FIGURE 20. Typical I/O Routines for ADC0808/ADC0809 and 6800 Interface

Figure 21 shows a very simple Z80 interface, which is similar to the INS8080 interface of *Figure 13*, except that the interrupt flip-flop design is closer to the 6800 designs. This is because the Z80 $\overline{INT}$ is active low as is the 6800, but the INS8080 INT is active high.

Figure 22 shows a fully decoded bus comparator design where the DM8131 decodes 5 address bits and the $\overline{IOREQ}$ I/O request strobe. Two NOR gates gate the $\overline{RD}$ and $\overline{WR}$ strobes for ALE, START and OE inputs.

4.0 CONCLUSION

Both the ADC0808 and the ADC0809 can be easily used in microprocessor controlled environments. Many sophisticated medium throughput applications can be handled with a minimum of extra hardware, but additional hardware can increase flexibility and simplify software. Putting both the multiplexer and A/D on the same chip frees the designer from matching multiplexers and A/Ds to implement a 7 or 8-bit accurate system. Design time and overall system cost can be reduced by using these low cost converters.

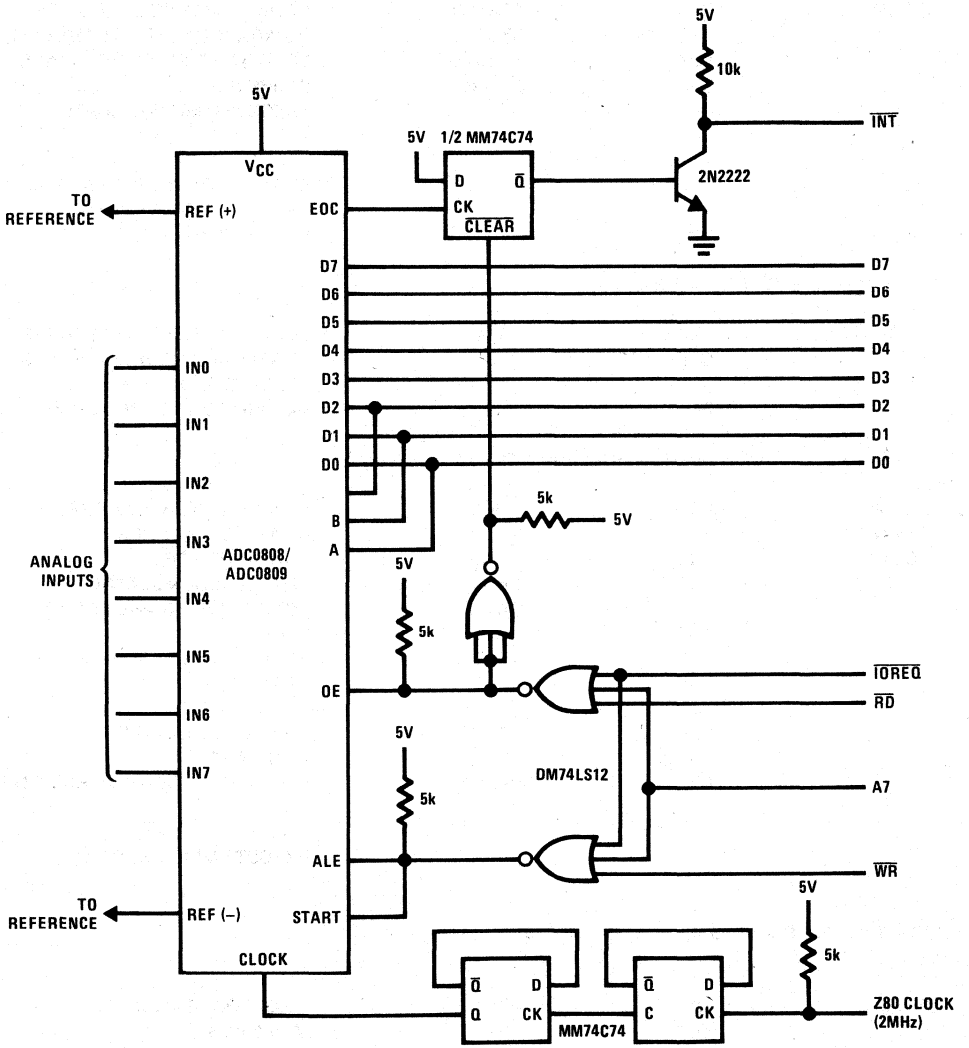


FIGURE 21. Simple Z80 Interface

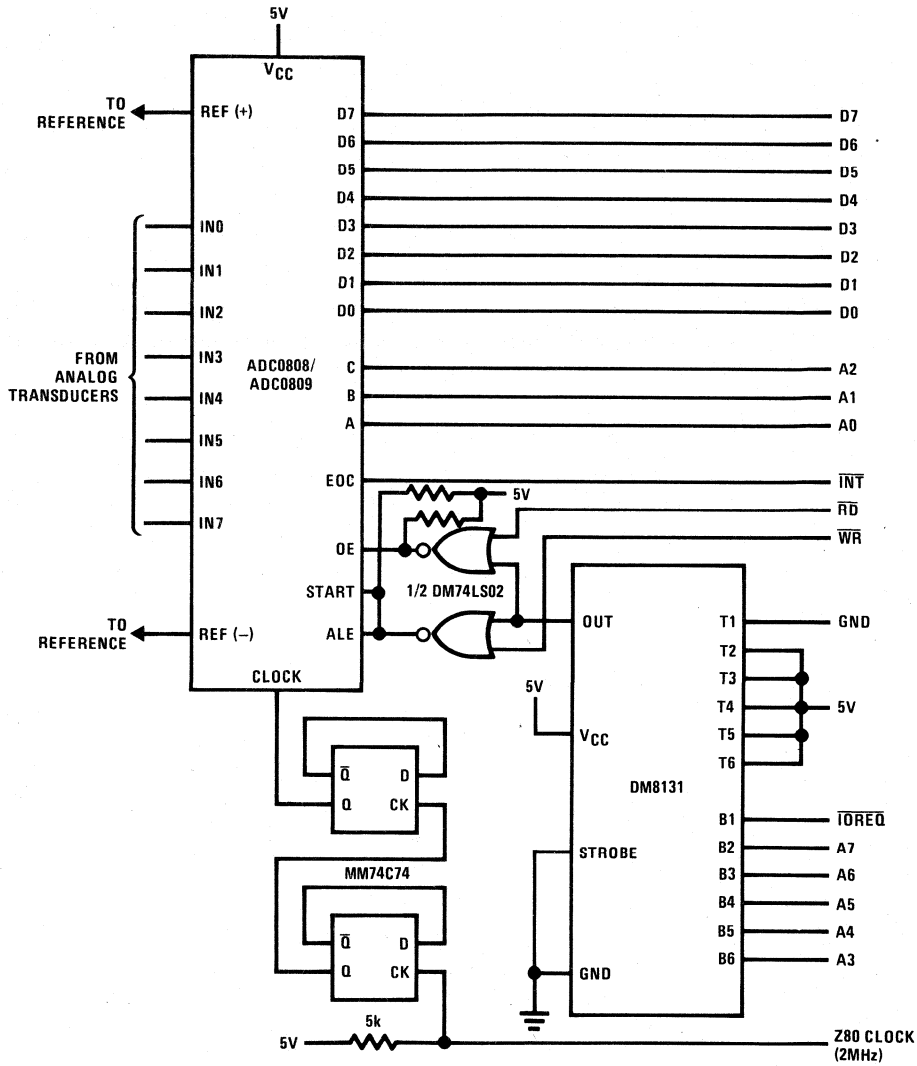


FIGURE 22. Z80 Partial Decoding Interface

Section 16

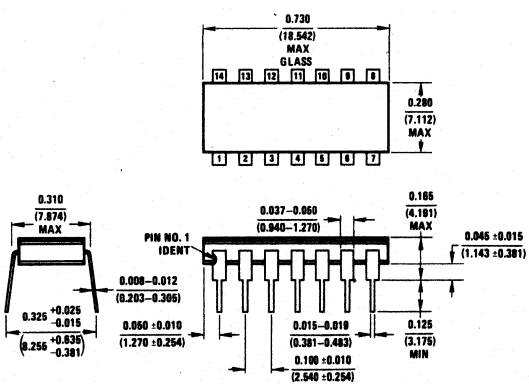
Physical Dimensions

16

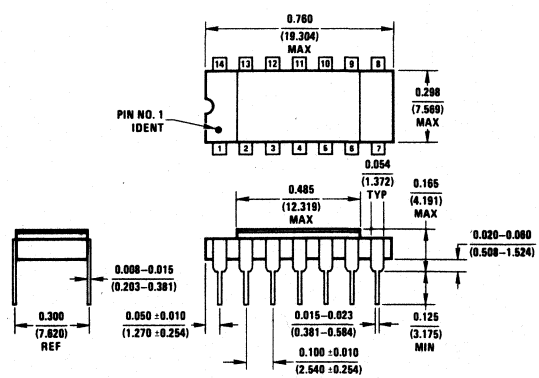
Physical Dimensions

Section Contents

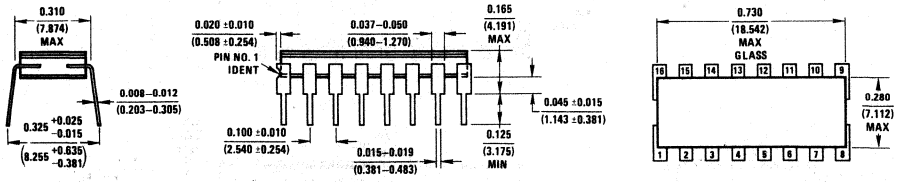
All dimensions in inches(millimeters).



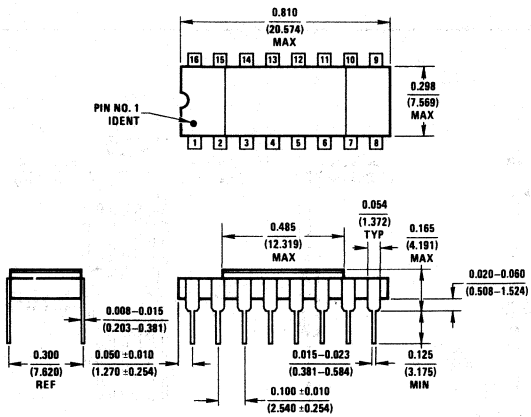
NS Package D14A
14-Lead Cavity DIP (D)



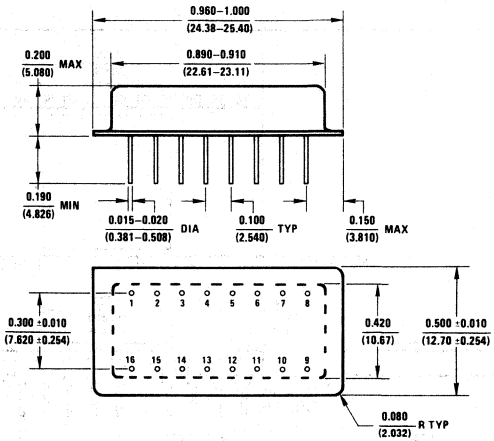
NS Package D14E
14-Lead Cavity DIP (D)



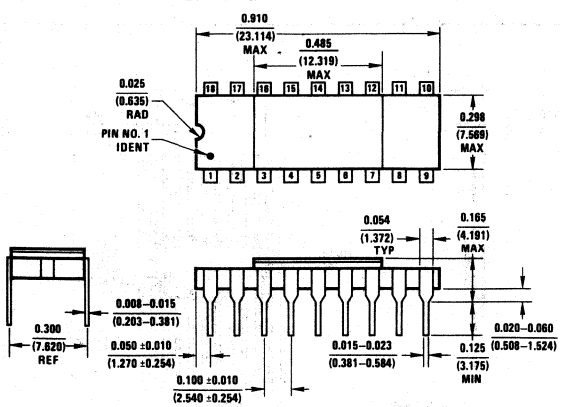
NS Package D16A
16-Lead Cavity DIP (D)



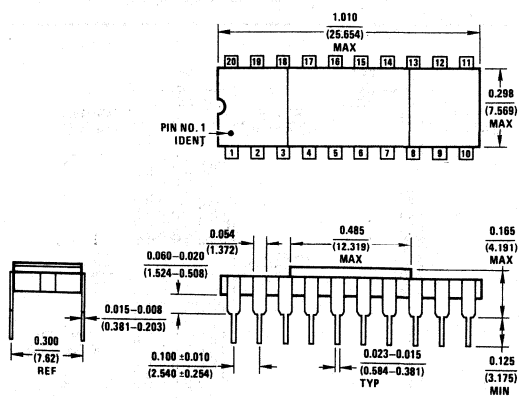
NS Package D16C
16-Lead Cavity DIP (D)
(Side Brazed)



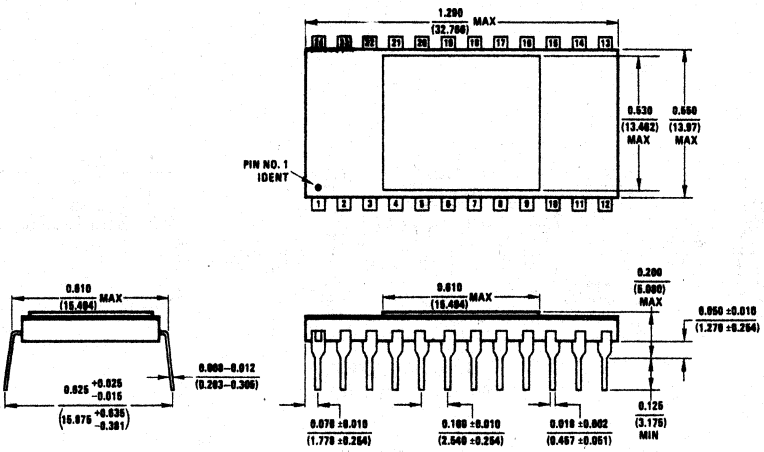
NS Package D16D
16-Lead Cavity DIP (D)



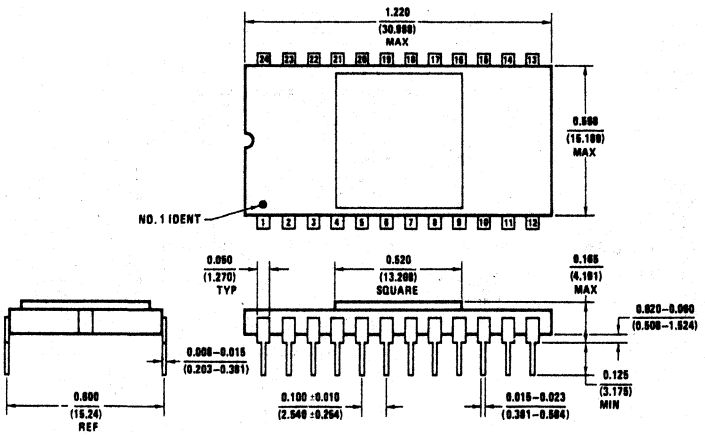
NS Package D18A
18-Lead Cavity DIP (D)
(Side Brazed)



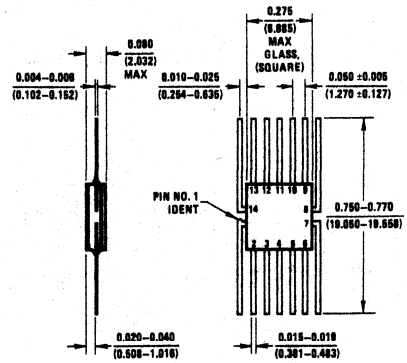
NS Package D20A
20-Lead Cavity DIP (D)
(Side Brazed)



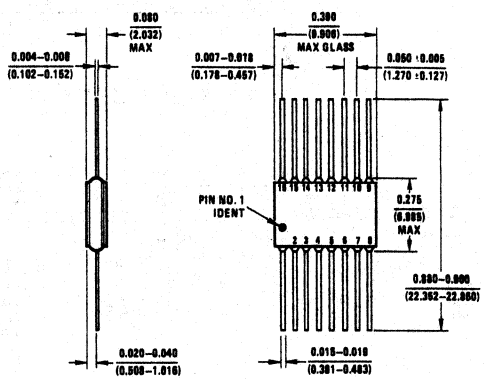
NS Package D24A
24-Lead Cavity DIP (D)



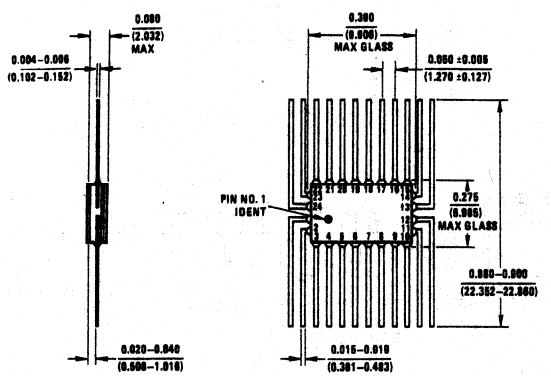
NS Package D24C
24-Lead Cavity DIP (D)



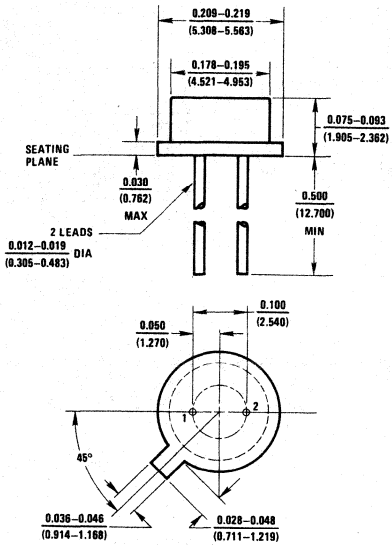
NS Package F14A
14-Lead Flat Package (F)



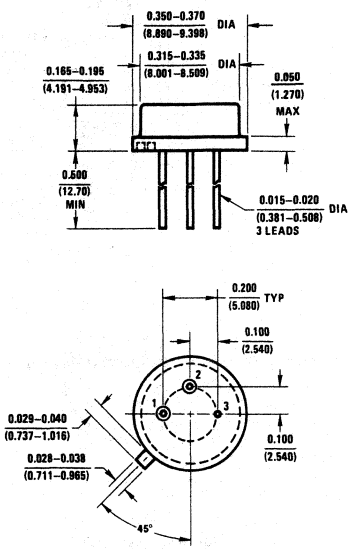
NS Package F16A
16-Lead Flat Package (F)



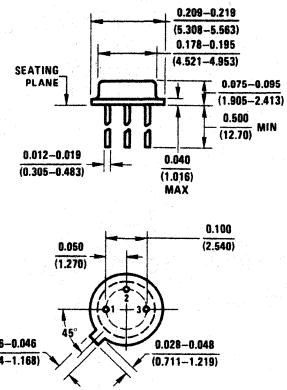
NS Package F24A
24-Lead Flat Package (F)



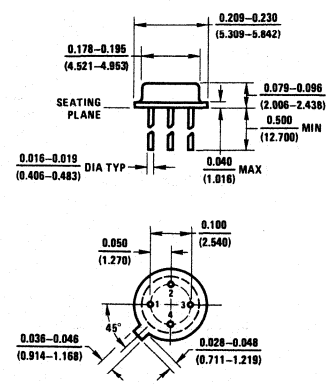
NS Package H02A
2-Lead TO-46 Metal Can Package (H)



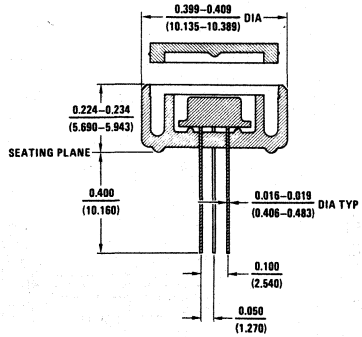
NS Package H03A
3-Lead TO-39 Metal Can Package (H)



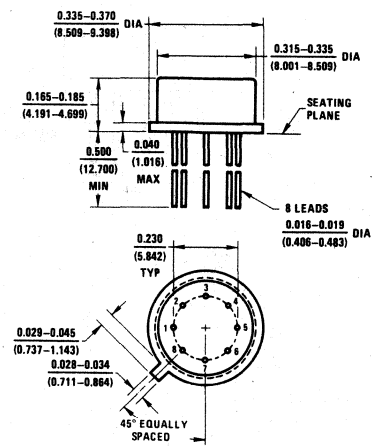
NS Package H03H
3-Lead TO-46 Metal Can Package (H)



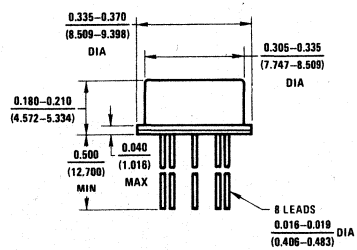
NS Package H04A
4-Lead TO-46 Metal Can Package (H)

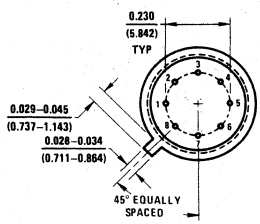


NS Package H04D
Thermal Shield for H04A

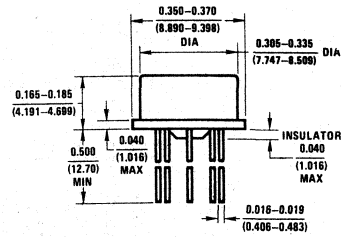


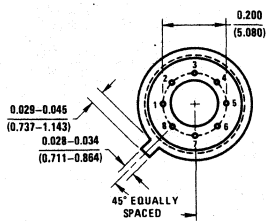
NS Package H08A
8-Lead TO-5 Metal Can Package (H)



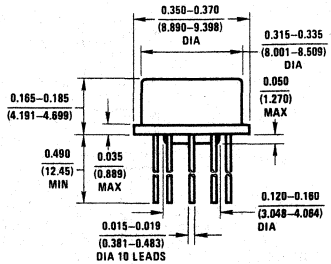


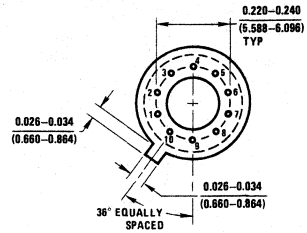
NS Package H08B
8-Lead TO-5 Metal Can Package (H)



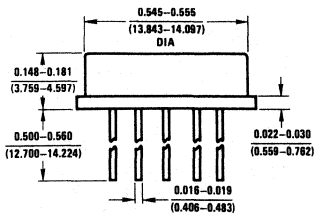


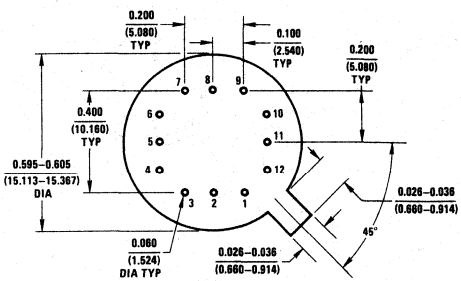
NS Package H08C
8-Lead TO-5 Metal Can Package (H)



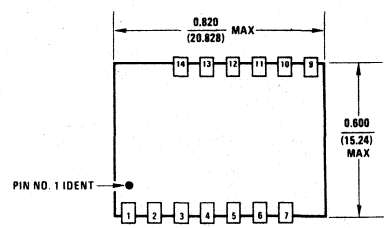


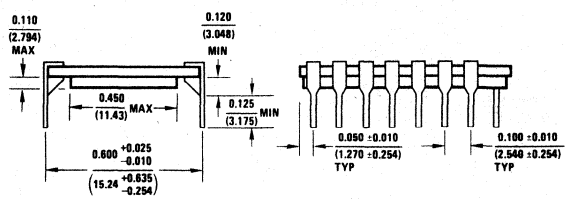
NS Package H10C
10-Lead TO-5 Metal Can Package (H)
(Low Profile)



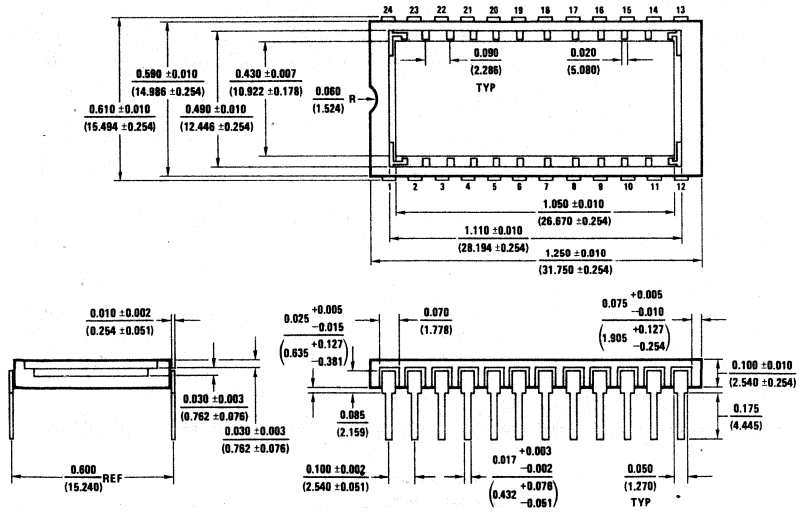


NS Package H12B
12-Lead TO-8 Metal Can Package (H)

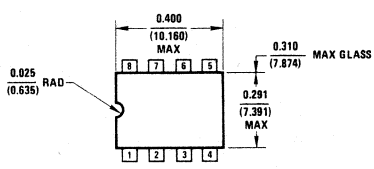


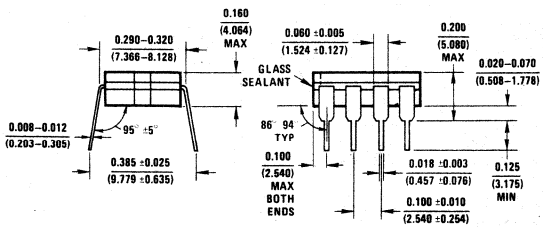


NS Package HY13A
13-Lead Epoxy/Ceramic Package (J) (Hybrid)

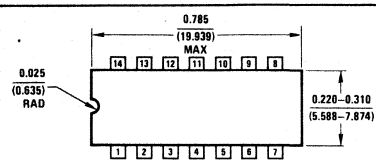


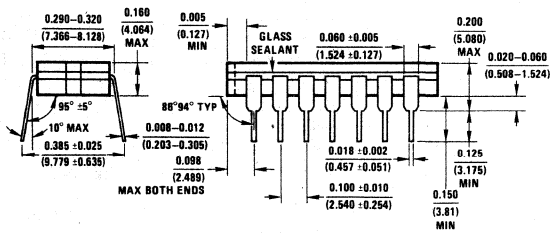
NS Package D24D
24-Lead Epoxy/Ceramic Package (D) (Hybrid)



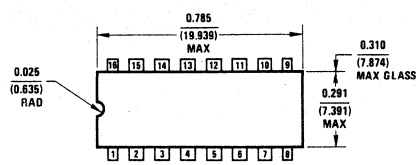


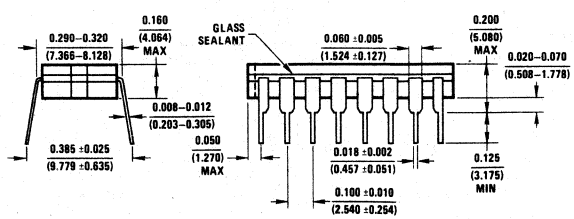
NS Package J08A
8-Lead Cavity DIP (J)



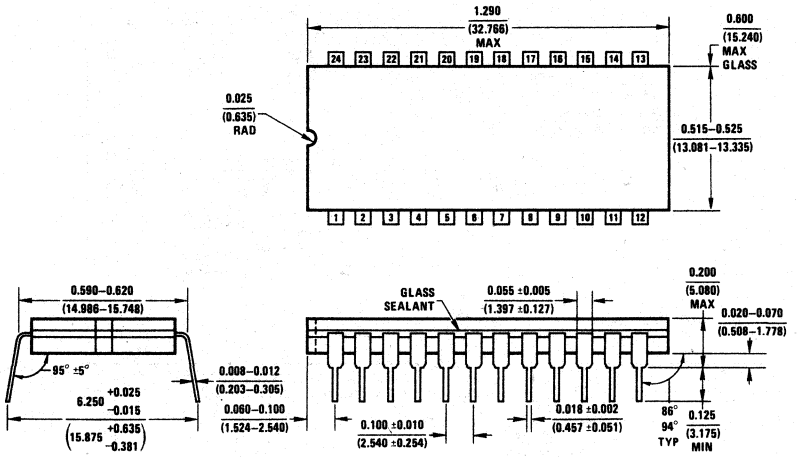


NS Package J14A
14-Lead Cavity DIP (J)

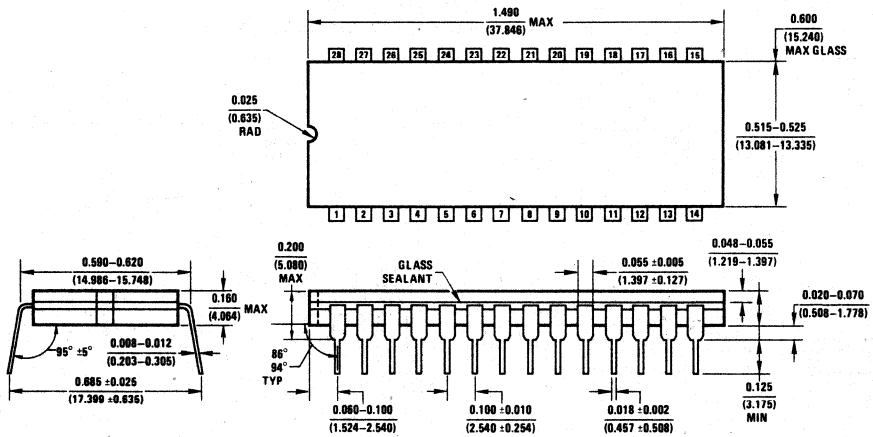




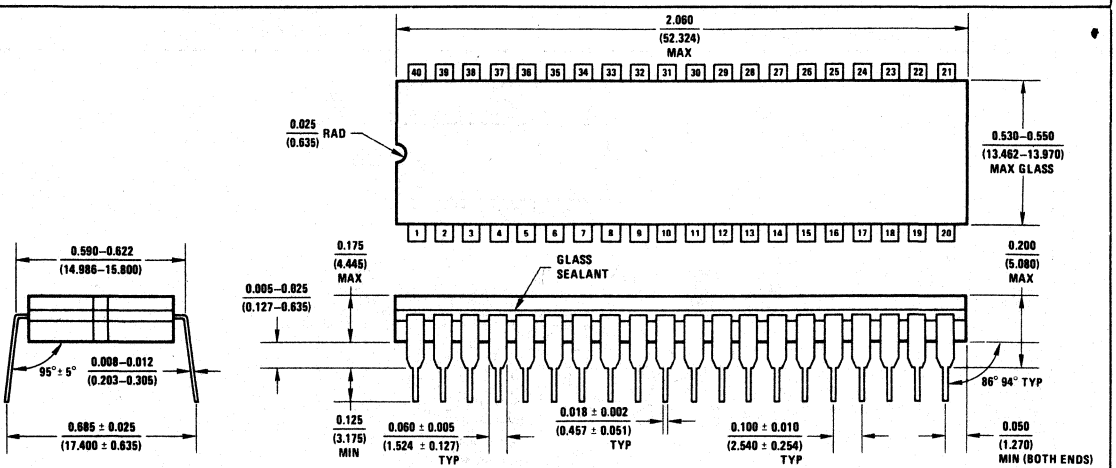
NS Package J16A
16-Lead Cavity DIP (J)



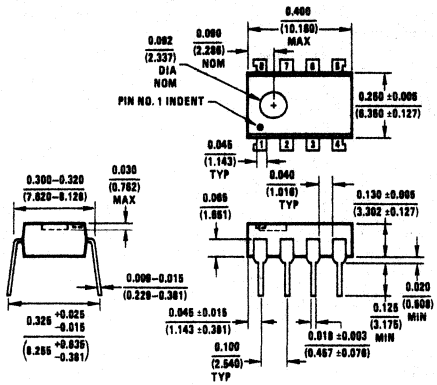
NS Package J24A
24-Lead Cavity DIP (J)



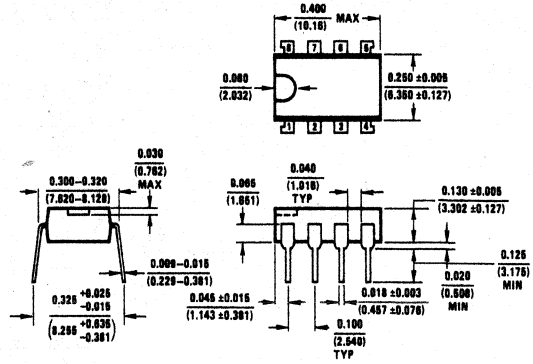
NS Package J28A
28-Lead Cavity DIP (J)



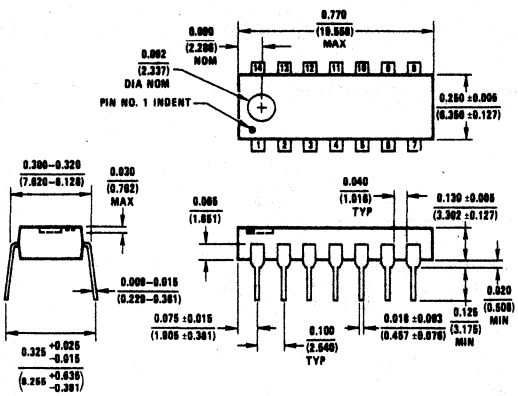
NS Package J40A
40-Lead Cavity DIP (J)



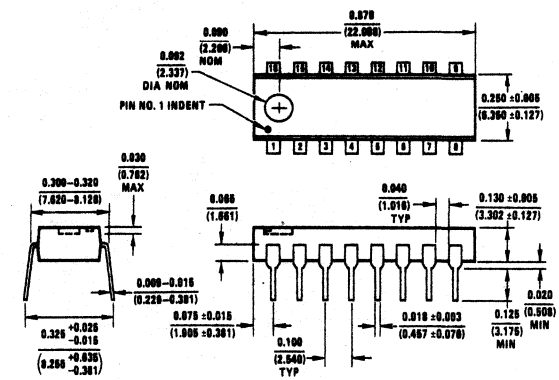
NS Package N08A
8-Lead Molded Mini-DIP (N)



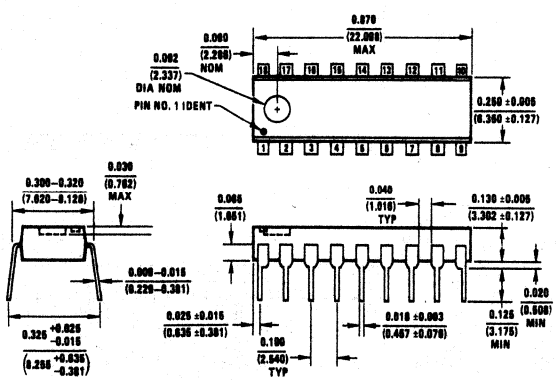
NS Package N08B
8-Lead Molded Mini-DIP (N)



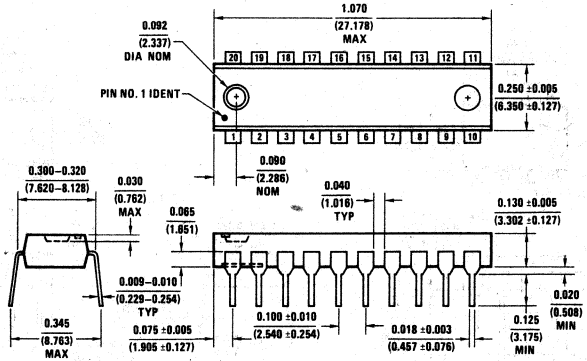
NS Package N14A
14-Lead Molded DIP (N)



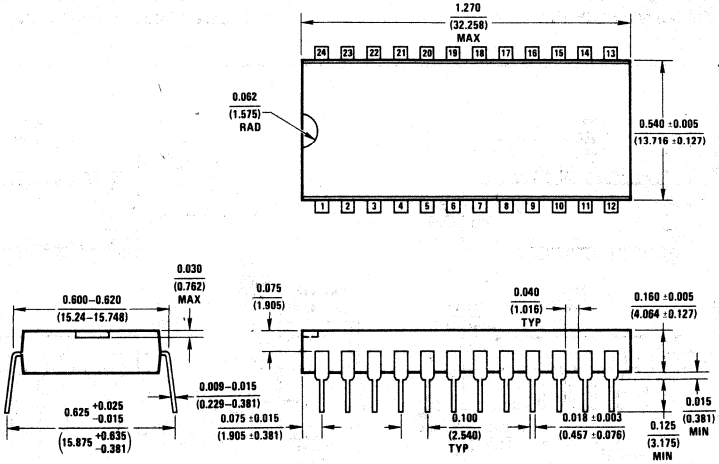
NS Package N16A
16-Lead Molded DIP (N)



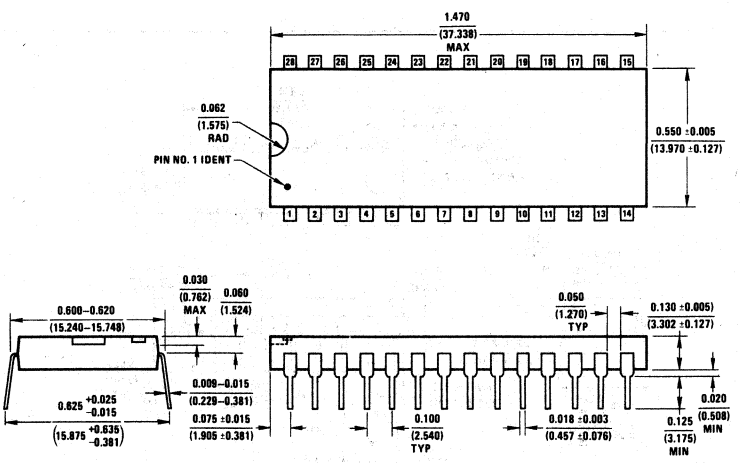
NS Package N18A
18-Lead Molded DIP (N)



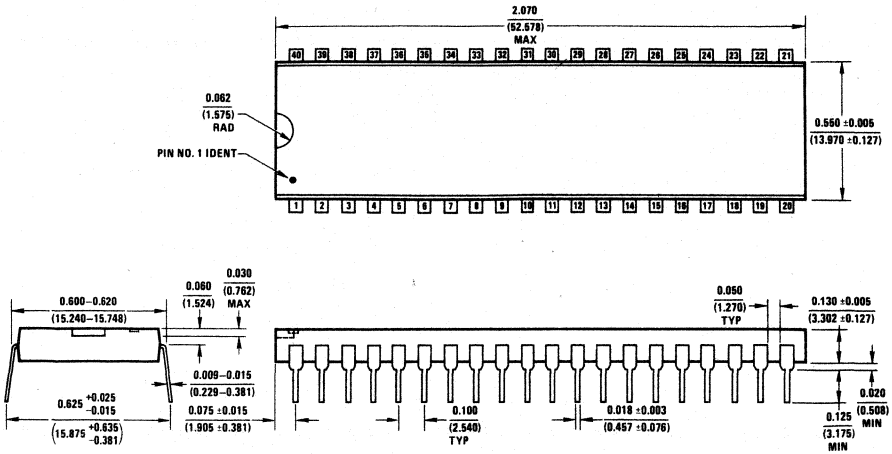
NS Package N20A
20-Lead Molded DIP (N)



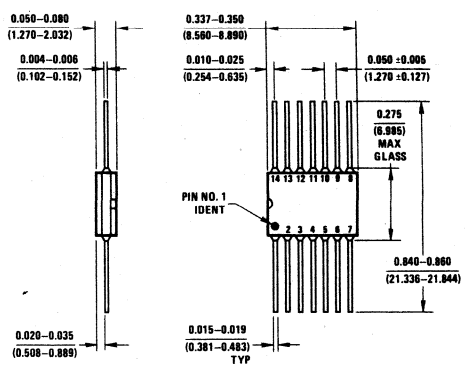
NS Package N24A
24-Lead Molded DIP (N)



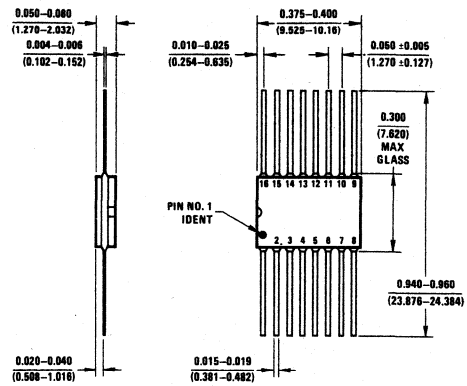
NS Package N28A
28-Lead Molded DIP (N)



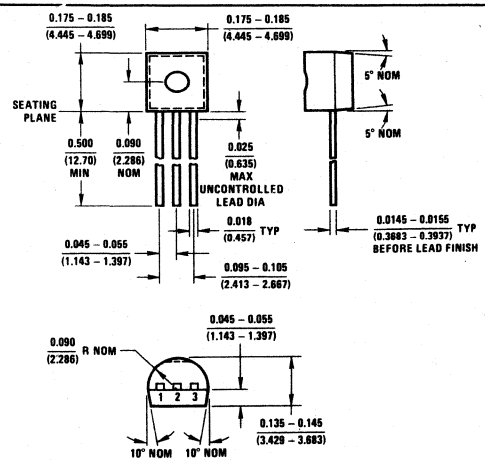
NS Package N40A
40-Lead Molded DIP (N)



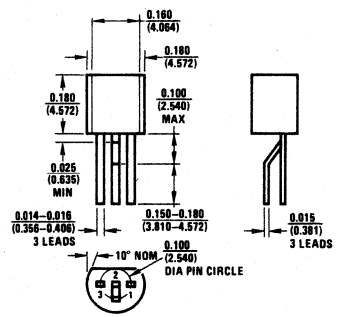
NS Package W14A
14-Lead Flat Package (W)



NS Package W16A
16-Lead Flat Package (W)



NS Package Z03A
3-Lead TO-92 Plastic Package (Z)



NS Package Z03D
3-Lead TO-92 Plastic Package (Z)

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